

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operate With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for n-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Push-Down Registers
  - Buffer Storage
  - Accumulator Registers
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

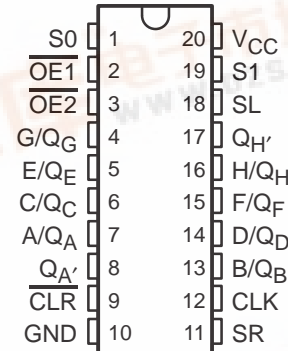
## description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0$ ,  $S_1$ ) inputs and two output-enable ( $\overline{OE}1$ ,  $\overline{OE}2$ ) inputs can be used to choose the modes of operation listed in the function table.

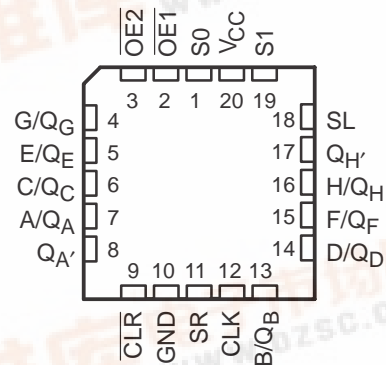
Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE}1$  or  $\overline{OE}2$  high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS299 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS299 . . . J PACKAGE  
SN74ALS299 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS299 . . . FK PACKAGE  
(TOP VIEW)



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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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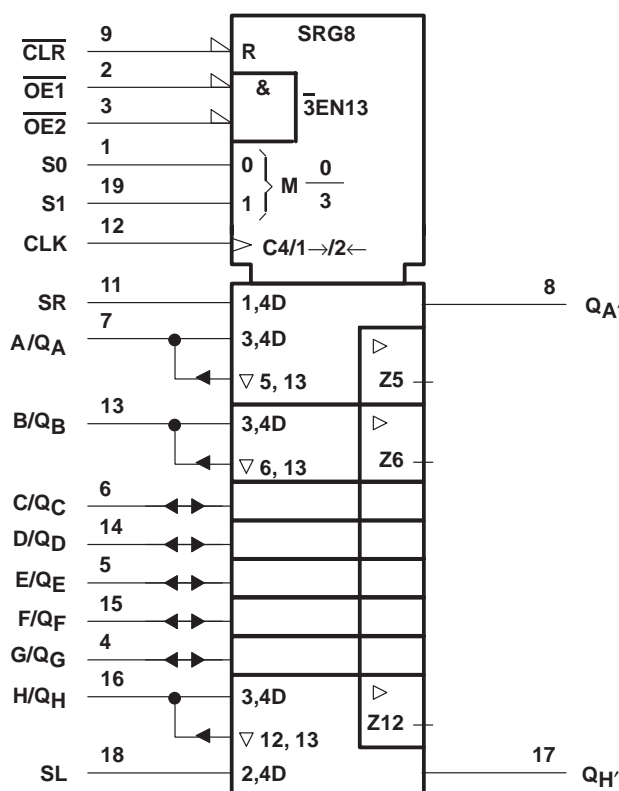
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

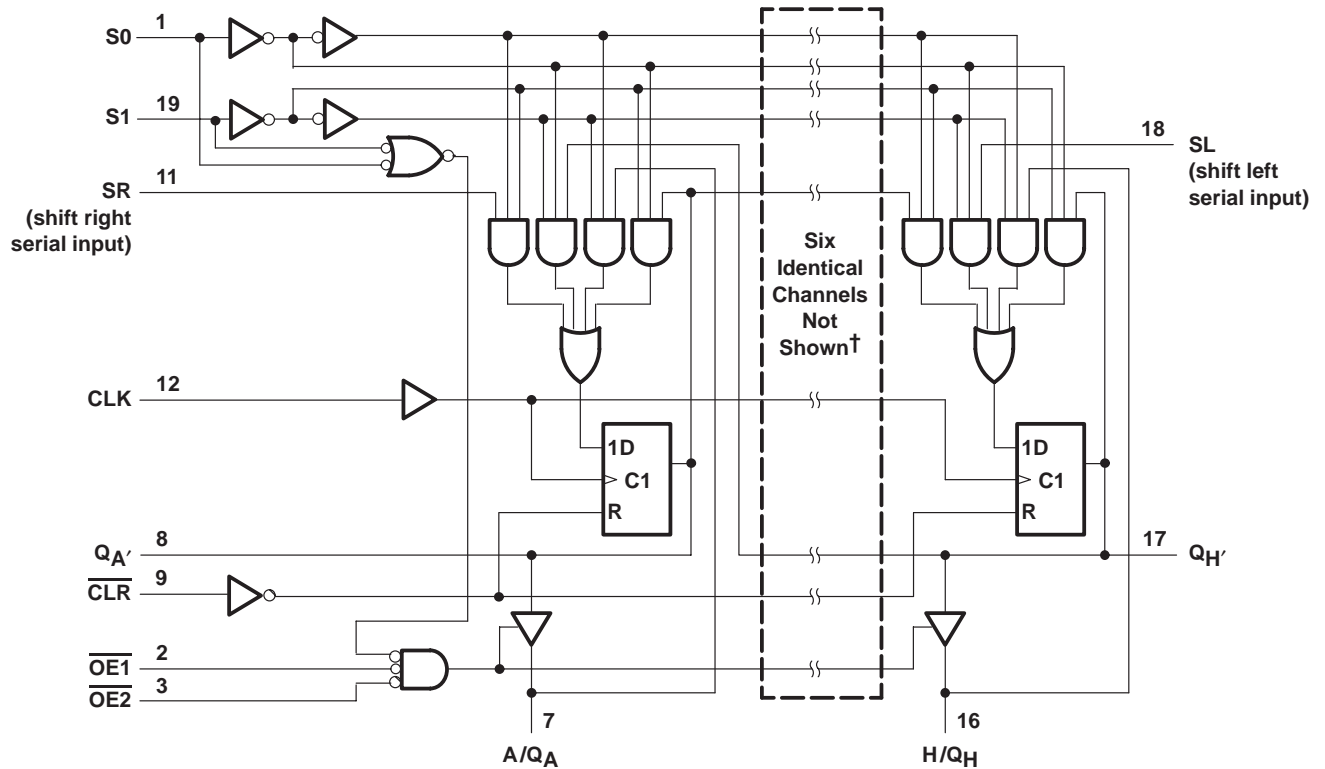
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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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#### logic diagram (positive logic)



† I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS299	–55°C to 125°C
SN74ALS299	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions

			SN54ALS299			SN74ALS299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
I <sub>OH</sub>	High-level output current	Q <sub>A</sub> ' or Q <sub>H</sub> '	−0.4			−0.4			mA
		Q <sub>A</sub> − Q <sub>H</sub>	−1			−2.6			
I <sub>OL</sub>	Low-level output current	Q <sub>A</sub> ' or Q <sub>H</sub> '	4			8			mA
		Q <sub>A</sub> − Q <sub>H</sub>	12			24			
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299			SN74ALS299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA				–1.5			–1.5	V
V <sub>OH</sub>	All outputs	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = –0.4 mA		V <sub>CC</sub> – 2			V <sub>CC</sub> – 2			V
	Q <sub>A</sub> – Q <sub>H</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = –1 mA	2.4	3.3					
			I <sub>OH</sub> = –2.6 mA				2.4	3.2		
V <sub>OL</sub>	Q <sub>A'</sub> or Q <sub>H'</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
			I <sub>OL</sub> = 8 mA				0.35	0.5		
	Q <sub>A</sub> – Q <sub>H</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4		0.25	0.4		
			I <sub>OL</sub> = 24 mA				0.35	0.5		
I <sub>I</sub>	A – H	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V			0.1			0.1	mA
	Any others		V <sub>I</sub> = 7 V			0.1			0.1	
I <sub>IH</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V				20			20	μA
I <sub>IL</sub> ‡	S0, S1, SR, SL	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V				–0.2			–0.2	mA
	Any others					–0.1			–0.1	
I <sub>OS</sub> §	Q <sub>A'</sub> or Q <sub>H'</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		–15		–70	–15		–70	mA
	Q <sub>A</sub> – Q <sub>H</sub>			–20		–112	–30		–112	
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V	Outputs high	15		28	15		28	mA
			Outputs low	22		38	22		38	
			Outputs disabled	23		40	23		40	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports (Q<sub>A</sub> – Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ALS299	SN74ALS299	UNIT
				MIN	MAX	
$f_{\text{clock}}$	Clock frequency (at 50% duty cycle)			0	17	MHz
$t_w$	Pulse duration	CLK high or low		22	16.5	ns
		CLR low		12	10	
$t_{\text{su}}$	Setup time before CLK $\uparrow$	S0 or S1		25	20	ns
		Serial or parallel data	High	18	16	
			Low	15	6	
	Inactive-state setup time before CLK $\uparrow\uparrow$	CLR		15	15	
$t_h$	Hold time after CLK $\uparrow$	S0 or S1		0	0	ns
		Serial or parallel data		0	0	

$\uparrow$  Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX‡				UNIT
			SN54ALS299		SN74ALS299		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			17		30		MHz
t <sub>PLH</sub>	CLK	Q <sub>A</sub> –Q <sub>H</sub>	2	19	4	13	ns
t <sub>PHL</sub>			4	25	7	19	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	2	21	5	15	ns
t <sub>PHL</sub>			4	25	8	18	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q <sub>A</sub> –Q <sub>H</sub>	6	29	6	22	ns
		Q <sub>A</sub> ' or Q <sub>H</sub> '	6	29	6	22	
t <sub>PZH</sub>	$\overline{\text{OE1}}, \overline{\text{OE2}}$	Q <sub>A</sub> –Q <sub>H</sub>	5	22	6	16	ns
t <sub>PZL</sub>			6	27	8	22	
t <sub>PZH</sub>	S0, S1	Q <sub>A</sub> –Q <sub>H</sub>	5	27	7	17	ns
t <sub>PZL</sub>			6	26	8	22	
t <sub>PHZ</sub>	$\overline{\text{OE1}}, \overline{\text{OE2}}$	Q <sub>A</sub> –Q <sub>H</sub>	1	15	1	8	ns
t <sub>PLZ</sub>			4	38	5	15	
t <sub>PHZ</sub>	S0, S1	Q <sub>A</sub> –Q <sub>H</sub>	1	16	1	12	ns
t <sub>PLZ</sub>			4	34	8	25	

$\ddagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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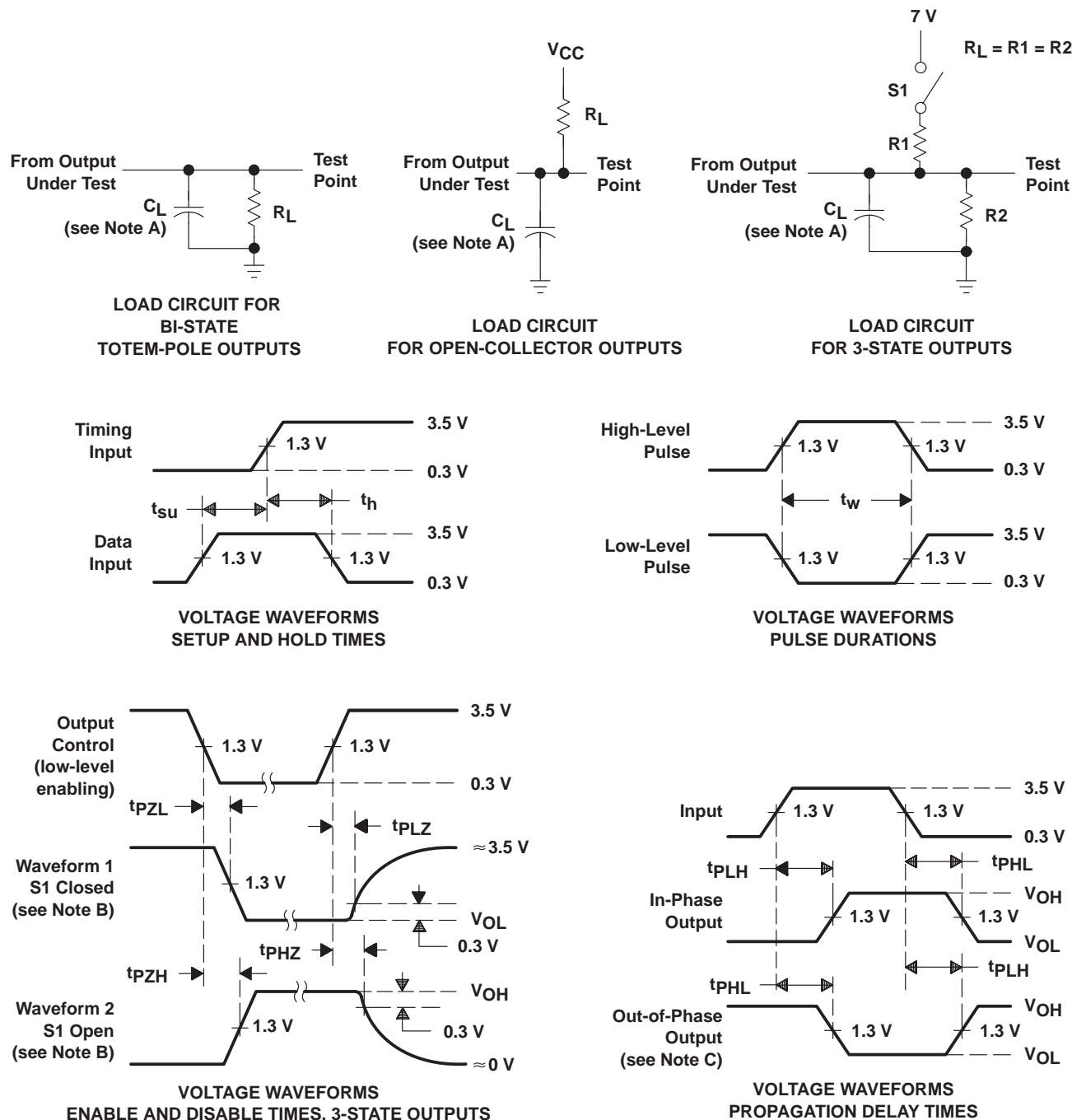
## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION

#### SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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