FAIRCHILD SEMICONDUCTOR®

July 1988
Revised March 2005

# 74AC299 • 74ACT299
# 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

## General Description

The AC/ACT299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops $Q_0$, $Q_7$ to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

## Features

- $I_{CC}$ and $I_{OZ}$ reduced by 50%
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- ACT299 has TTL-compatible inputs

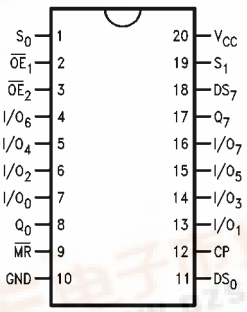
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC299SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC299SCX_NL (Note 1) | M20B | Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC299SJ | M20D | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC299MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC299PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT299SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT299MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT299PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| CP | Clock Pulse Input |
| $DS_0$ | Serial Data Input for Right Shift |
| $DS_7$ | Serial Data Input for Left Shift |
| $S_0$, $S_1$ | Mode Select Inputs |
| $\overline{MR}$ | Asynchronous Master Reset |
| $\overline{OE}_1$, $\overline{OE}_2$ | 3-STATE Output Enable Inputs |
| $I/O_0$–$I/O_7$ | Parallel Data Inputs or 3-STATE Parallel Outputs |
| $Q_0$, $Q_7$ | Serial Outputs |

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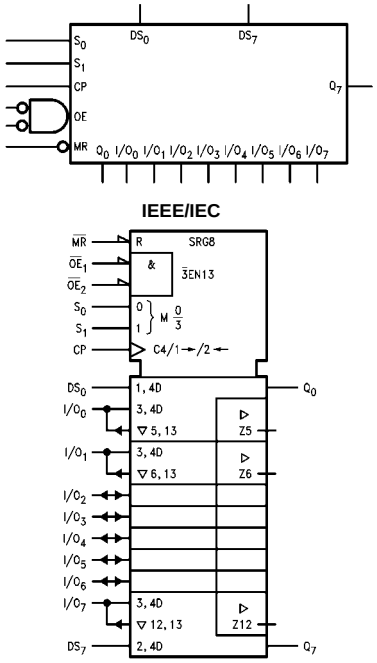
## Logic Symbols




## Truth Table

| Inputs | | | | Response |
|---|---|---|---|---|
| $\overline{MR}$ | $S_1$ | $S_0$ | CP | |
| L | X | X | X | Asynchronous Reset; $Q_0$–$Q_7$ = LOW |
| H | H | H | ⌐ | Parallel Load; $I/O_n \rightarrow Q_n$ |
| H | L | H | ⌐ | Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc. |
| H | H | L | ⌐ | Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc. |
| H | L | L | X | Hold |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

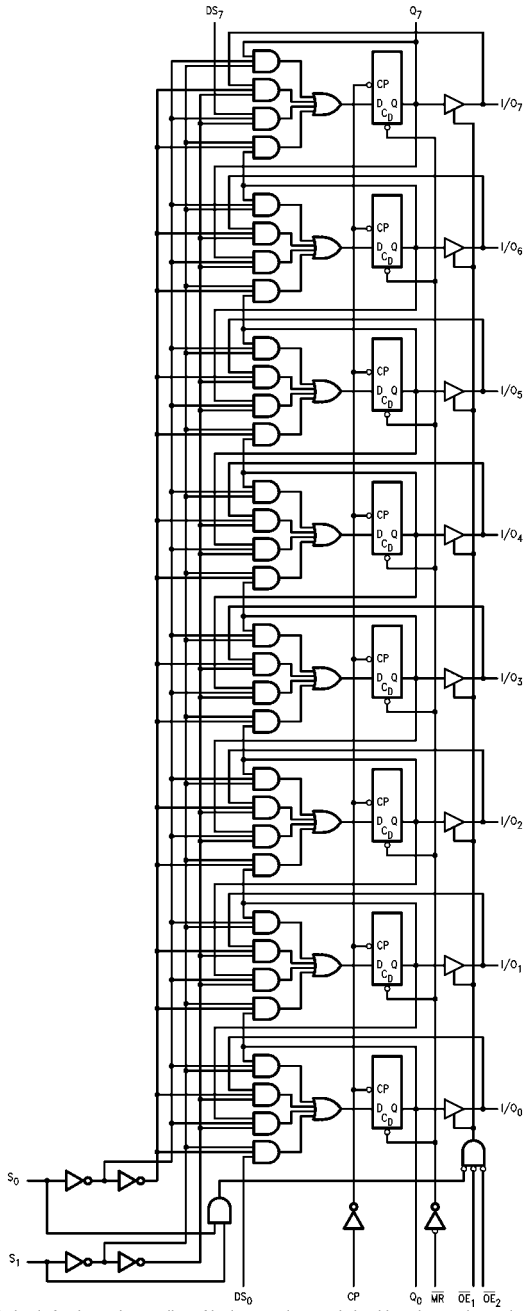
## Functional Description

The AC/ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by $S_0$ and $S_1$, as shown in the Truth Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. $Q_0$ and $Q_7$ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both $S_0$ and $S_1$ in preparation for a parallel load operation.

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ +0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ +0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Source or Sink Current ($I_O$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current | |
| Per Output Pin ($I_{CC}$ or $I_{GND}$) | ± 50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| (PDIP) | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| (Unless Otherwise Specified) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.0V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| AC Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | (V) | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level | 3.0 | 1.5 | 2.1 | 2.1 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.9 | 0.9 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level | 3.0 | 2.99 | 2.9 | 2.9 | | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | V | $I_{OH}$ = −12 mA |
| | | 4.5 | | 3.86 | 3.76 | | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 3) |
| $V_{OL}$ | Maximum LOW Level | 3.0 | 0.002 | 0.1 | 0.1 | | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OH}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OH}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OH}$ = 24 mA (Note 3) |
| $I_{IN}$ (Note 5) | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 86 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 4) | | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 5) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

## DC Electrical Characteristics for AC (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = 25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{OZT}$ | Maximum I/O Leakage Current | 5.5 | | ± 0.3 | ± 3.0 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |

**Note 3:** All outputs loaded; threshold on input associated with output under test.

**Note 4:** Maximum test duration 20 ms, one output loaded at a time.

**Note 5:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = 25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V |
| | Input Voltage | 5.5 | 1.5 | 2.0 | 2.0 | | or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | | or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum HIGH Level | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | 0.0001 | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 6) |
| $V_{OL}$ | Maximum LOW Level | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | Output Voltage | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$= 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$= 24 mA (Note 6) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1V |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 7) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{OZT}$ | Maximum I/O | | | | | | $V_I$ (OE) = $V_{IL}$, $V_{IH}$ |
| | Leakage Current | 5.5 | | ±0.3 | ±3.0 | μA | $V_I$ = $V_{CC}$, GND |
| | | | | | | | $V_O$ = $V_{CC}$, GND |

**Note 6:** All outputs loaded; thresholds on input associated with output under test.

**Note 7:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Input | 3.3 | 90 | 124 | | 80 | | MHz |
| | Frequency | 5.0 | 130 | 173 | | 105 | | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 8.5 | 14.0 | 20.5 | 7.0 | 22.0 | ns |
| | CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 5.5 | 9.5 | 14.0 | 4.5 | 15.0 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 8.5 | 14.5 | 21.5 | 7.0 | 23.0 | ns |
| | CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 5.5 | 10.0 | 14.5 | 5.0 | 16.0 | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 9.0 | 14.5 | 20.5 | 7.5 | 22.5 | ns |
| | $\overline{CP}$ to $I/O_n$ | 5.0 | 6.0 | 10.0 | 14.5 | 5.0 | 16.0 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 10.0 | 16.0 | 23.0 | 8.5 | 24.5 | ns |
| | $\overline{CP}$ to $I/O_n$ | 5.0 | 6.5 | 11.0 | 16.0 | 6.0 | 17.5 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 9.0 | 15.5 | 22.5 | 7.5 | 25.0 | ns |
| | $\overline{MR}$ to $Q_0$ or $Q_7$ | 5.0 | 5.5 | 10.5 | 15.5 | 5.0 | 17.0 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 9.0 | 15.0 | 21.5 | 7.5 | 24.0 | ns |
| | $\overline{MR}$ to $I/O_n$ | 5.0 | 5.5 | 10.0 | 15.0 | 5.0 | 16.5 | |
| $t_{PZH}$ | Output Enable Time | 3.3 | 7.0 | 12.0 | 18.0 | 6.0 | 19.5 | ns |
| | $\overline{OE}$ to $I/O_n$ | 5.0 | 4.5 | 8.5 | 12.5 | 4.0 | 13.5 | |
| $t_{PZL}$ | Output Enable Time | 3.3 | 7.0 | 12.5 | 18.0 | 6.0 | 20.5 | ns |
| | $\overline{OE}$ to $I/O_n$ | 5.0 | 5.0 | 8.0 | 12.5 | 4.0 | 14.0 | |
| $t_{PHZ}$ | Output Disable Time | 3.3 | 6.5 | 13.0 | 18.5 | 5.5 | 19.5 | ns |
| | $\overline{OE}$ to $I/O_n$ | 5.0 | 3.5 | 9.5 | 14.0 | 3.0 | 15.0 | |
| $t_{PLZ}$ | Output Disable Time | 3.3 | 5.5 | 11.5 | 17.0 | 4.5 | 19.0 | ns |
| | $\overline{OE}$ to $I/O_n$ | 5.0 | 3.5 | 8.0 | 12.5 | 2.0 | 13.5 | |

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V.
Voltage Range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW | 3.3 | 3.0 | 8.0 | 8.5 | ns |
| | $S_0$ or $S_1$ to CP | 5.0 | 2.0 | 5.0 | 5.5 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | −3.0 | 0.5 | 0.5 | ns |
| | $S_0$ or $S_1$ to CP | 5.0 | −1.5 | 1.0 | 1.0 | |
| $t_S$ | Setup Time, HIGH or LOW | 3.3 | 2.0 | 5.5 | 6.0 | ns |
| | $I/O_n$ to CP | 5.0 | 1.0 | 3.5 | 4.0 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | −2.0 | 0 | 0 | ns |
| | $I/O_n$ to CP | 5.0 | −1.0 | 1.0 | 1.0 | |
| $t_S$ | Setup Time, HIGH or LOW | 3.3 | 2.5 | 6.5 | 7.0 | ns |
| | $DS_0$ or $DS_7$ to CP | 5.0 | 1.5 | 4.0 | 4.5 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | −2.0 | 0 | 0.5 | ns |
| | $DS_0$ or $DS_7$ to CP | 5.0 | −1.0 | 1.0 | 1.0 | |
| $t_W$ | CP Pulse Width, LOW | 3.3 | 3.5 | 4.5 | 5.0 | ns |
| | | 5.0 | 2.0 | 3.5 | 3.5 | |
| $t_W$ | $\overline{MR}$ Pulse Width, LOW | 3.3 | 4.0 | 4.5 | 5.0 | ns |
| | | 5.0 | 2.0 | 3.5 | 3.5 | |
| $t_{REC}$ | Recovery Time | 3.3 | 0 | 1.5 | 1.5 | ns |
| | $\overline{MR}$ to CP | 5.0 | 0.5 | 1.5 | 1.5 | |

**Note 9:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) (Note 10) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Input Frequency | 5.0 | 120 | 170 | | 110 | | MHz |
| $t_{PLH}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 4.0 | 8.5 | 12.5 | 3.0 | 14.0 | ns |
| $t_{PHL}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 4.0 | 9.0 | 13.5 | 3.5 | 15.0 | ns |
| $t_{PLH}$ | Propagation Delay CP to $I/O_n$ | 5.0 | 4.5 | 8.5 | 12.5 | 4.5 | 13.5 | ns |
| $t_{PHL}$ | Propagation Delay CP to $I/O_n$ | 5.0 | 5.0 | 9.5 | 15.0 | 4.5 | 16.5 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $Q_0$ or $Q_7$ | 5.0 | 4.0 | 14.0 | 15.0 | 4.0 | 18.0 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $I/O_n$ | 5.0 | 4.0 | 13.0 | 14.5 | 3.5 | 17.5 | ns |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $I/O_n$ | 5.0 | 2.5 | 8.0 | 12.0 | 1.5 | 13.0 | ns |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $I/O_n$ | 5.0 | 2.0 | 8.0 | 12.0 | 1.5 | 13.5 | ns |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $I/O_n$ | 5.0 | 2.0 | 8.5 | 12.5 | 2.0 | 13.5 | ns |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $I/O_n$ | 5.0 | 2.5 | 8.0 | 11.5 | 2.0 | 12.5 | ns |

**Note 10:** Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for ACT

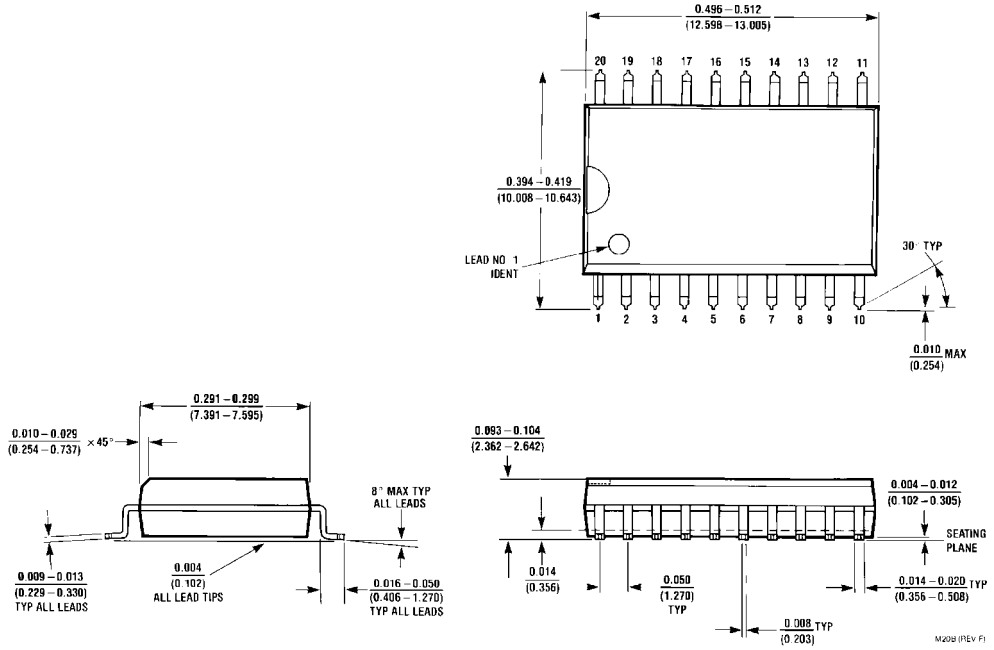
| Symbol | Parameter | $V_{CC}$ (V) (Note 11) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW $S_0$ or $S_1$ to CP | 5.0 | 2.0 | 5.0 | 5.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW $S_0$ or $S_1$ to CP | 5.0 | −2.0 | 1.0 | 1.0 | ns |
| $t_S$ | Setup Time, HIGH or LOW $I/O_n$ to CP | 5.0 | 1.5 | 4.0 | 4.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW $I/O_n$ to CP | 5.0 | −1.0 | 1.0 | 1.0 | ns |
| $t_S$ | Setup Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 5.0 | 1.5 | 4.5 | 5.0 | ns |
| $t_H$ | Hold Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 5.0 | −1.0 | 1.0 | 1.0 | ns |
| $t_W$ | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 4.0 | 4.5 | ns |
| $t_W$ | $\overline{MR}$ Pulse Width, LOW | 5.0 | 2.0 | 3.5 | 3.5 | ns |
| $t_{REC}$ | Recovery Time, $\overline{MR}$ to CP | 5.0 | 0 | 1.5 | 1.5 | ns |

**Note 11:** Voltage Range 5.0 is 5.0V ± 0.5V.

## Capacitance

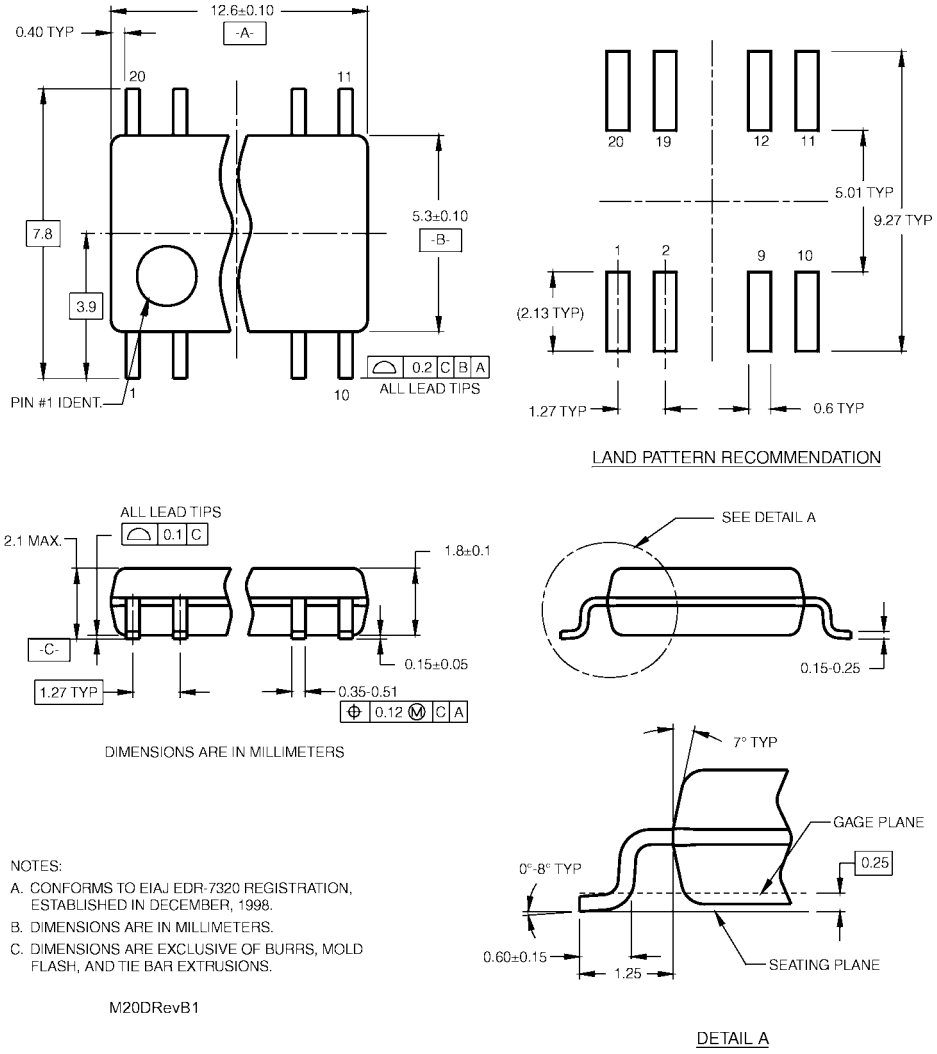
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| $C_{PD}$ | Power Dissipation Capacitance | 170 | pF | $V_{CC} = 5.5V$ |

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

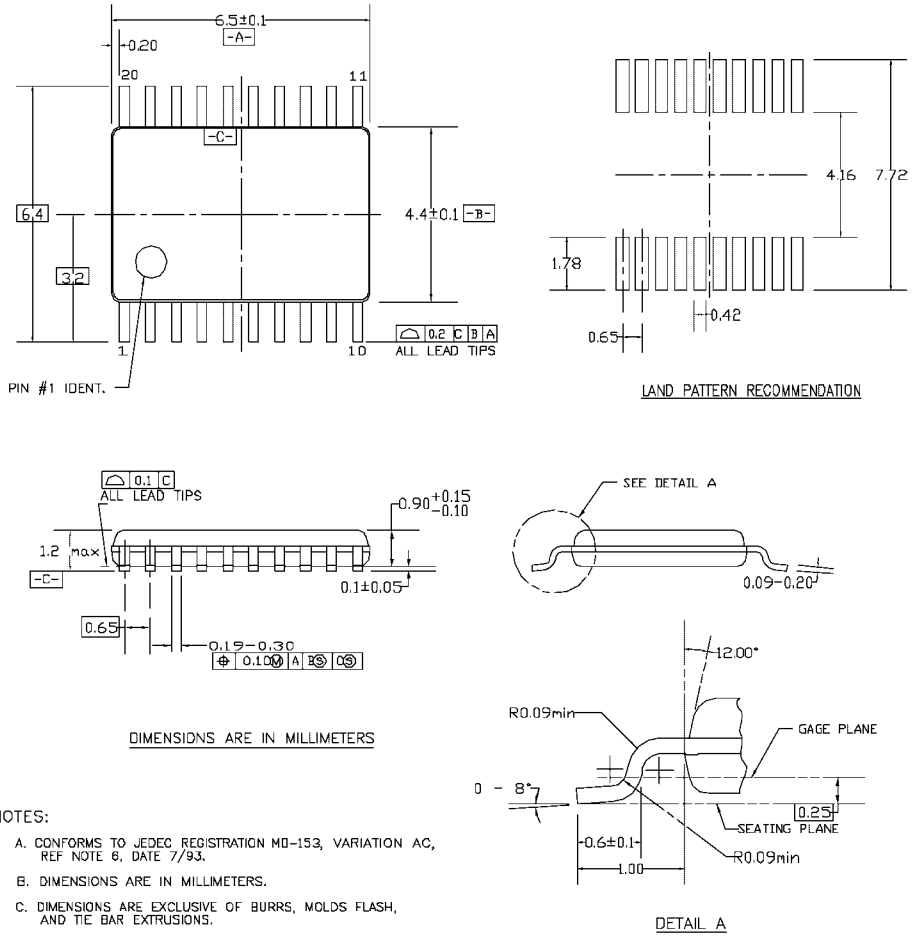
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M20D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

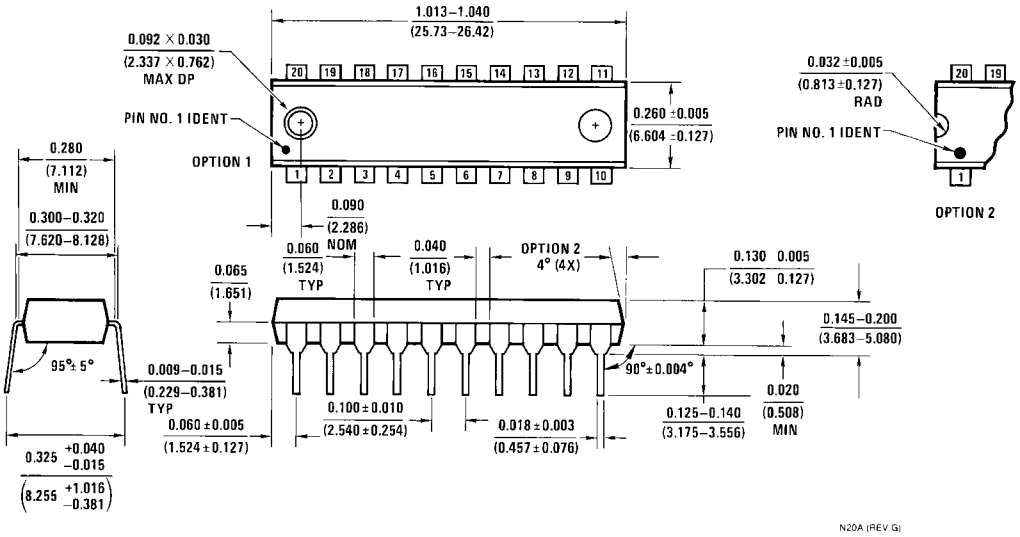
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC20**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N20A**