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Dual 260 MHz Gain = +2.0 & +2.2 Buffer

AD8079

FEATURES

Factory Set Gain
- AD8079A: Gain = +2.0 (Also +1.0 & –1.0)
- AD8079B: Gain = +2.2 (Also +1 & –1.2)
- Gain of 2.2 Compensates for System Gain Loss
- Minimizes External Components
- Tight Control of Gain and Gain Matching (0.1%)

Optimum Dual Pinout
- Simplifies PCB Layout
- Low Crosstalk of –70 dB @ 5 MHz

Excellent Video Specifications (R_L = 150 Ω)
- Gain Flatness 0.1 dB to 50 MHz
- 0.01% Differential Gain Error
- 0.02° Differential Phase Error

Low Power of 50 mW/Amplifier (5 mA)

High Speed and Fast Settling
- 260 MHz, –3 dB Bandwidth
- 750 V/μs Slew Rate (2 V Step), 800 V/μs (4 V Step)
- 40 ns Settling Time to 0.1% (2 V Step)

Low Distortion of –65 dBc THD, f_C = 5 MHz

High Output Drive of Over 70 mA
- Drives Up to 8 Back-Terminated 75 Ω Loads (4 Loads/Side) While Maintaining Good Differential Gain/Phase Performance (0.01%/0.17°)

High ESD Tolerance (5 kV)

Available in Small 8-Pin SOIC

APPLICATIONS

Differential A-to-D Driver
Video Line Driver
Differential Line Driver
Professional Cameras
Video Switchers
Special Effects
RF Receivers

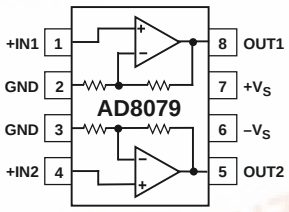
PRODUCT DESCRIPTION

The AD8079 is a dual, low power, high speed buffer designed to operate on ±5 V supplies. The AD8079's pinout offers excellent input and output isolation compared to the traditional dual amplifier pin configuration. With two ac ground pins separating both the inputs and outputs, the AD8079 achieves very low crosstalk of less than –70 dB at 5 MHz.

Additionally, the AD8079 contains gain setting resistors factory set at G = +2.0 (A grade) or Gain = +2.2 (B grade) allowing circuit configurations with minimal external components. The B grade gain of +2.2 compensates for gain loss through a system by providing a single-point trim. Using active laser trimming of these resistors, the AD8079 guarantees tight control of gain and channel-channel gain matching. With its performance and configuration, the AD8079 is well suited for driving differential

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic SOIC



cables and transformers. Its low distortion and fast settling are ideal for buffering high speed dual or differential A-to-D converters.

The AD8079 features a unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance of 0.01% and 0.02° on only 50 mW of power per amplifier. It features gain flatness of 0.1 dB to 50 MHz. This makes the AD8079 ideal for professional video electronics such as cameras and video switchers.

The AD8079 offers low power of 5 mA/amplifier (V_S = ±5 V) and can run on a single +12 V power supply while delivering over 70 mA of load current. All of this is offered in a small 8-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power are critical.

The outstanding bandwidth of 260 MHz along with 800 V/μs of slew rate make the AD8079 useful in many general purpose high speed applications where dual power supplies of ±3 V to ±6 V are required.

The AD8079 is available in the industrial temperature range of –40°C to +85°C.

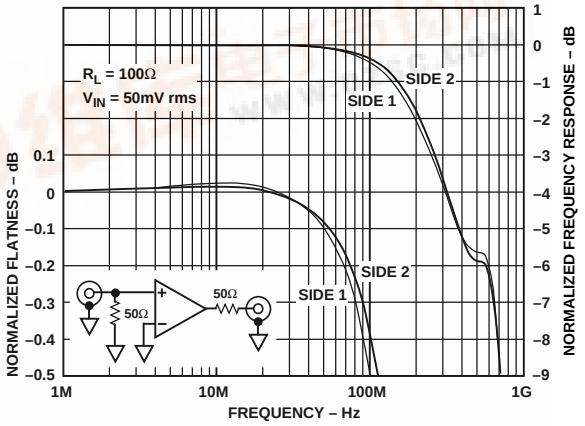


Figure 1. Frequency Response and Flatness

REV. A

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AD8079—SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted)

Parameter	Conditions	AD8079A/AD8079B Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{IN} = 50 mV rms		260		MHz
Bandwidth for 0.1 dB Flatness	V_{IN} = 50 mV rms		50		MHz
Large Signal Bandwidth	V_{IN} = 1 V rms		100		MHz
Slew Rate	V_O = 2 V Step		750		V/µs
	V_O = 4 V Step		800		V/µs
Settling Time to 0.1%	V_O = 2 V Step		40		ns
Rise & Fall Time	V_O = 2 V Step		2.5		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p		–65		dBc
Crosstalk, Output to Output	f = 5 MHz		–70		dB
Input Voltage Noise	f = 10 kHz		2.0		nV/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
Differential Gain Error	NTSC, R_L = 150 Ω		0.01		%
	R_L = 75 Ω		0.01		%
Differential Phase Error	NTSC, R_L = 150 Ω		0.02		Degree
	R_L = 75 Ω		0.07		Degree
DC PERFORMANCE					
Offset Voltage, RTO			10	15	mV
	T_{MIN}–T_{MAX}		10	20	mV
Offset Drift, RTO			20		µV/°C
+Input Bias Current			3.0	6.0	±µA
	T_{MIN}–T_{MAX}			10	±µA
Gain	No Load	1.998/2.198	2.0/2.2	2.002/2.202	V/V
	R_L = 150 Ω	1.995/2.195	2.0/2.2	2.005/2.205	V/V
Gain Matching	Channel-to-Channel, No Load		0.1		%
	Channel-to-Channel, R_L = 150 Ω		0.5		%
INPUT CHARACTERISTICS					
+Input Resistance	+Input		10		MΩ
+Input Capacitance	+Input		1.5		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.7	3.1		±V
	R_L = 75 Ω		2.8		±V
Output Current[1]			70		mA
Short Circuit Current[1]		85	110		mA
POWER SUPPLY					
Operating Range		±3.0		±6.0	V
Quiescent Current/Both Amplifiers	T_{MIN}–T_{MAX}		10.0	11.5	mA
Power Supply Rejection Ratio, RTO	$+V_S$ = +4 V to +6 V, $–V_S$ = –5 V	49	69		dB
	$–V_S$ = – 4 V to –6 V, $+V_S$ = +5 V	40	50		dB
+Input Current	T_{MIN}–T_{MAX}		0.1	0.5	µA/V

NOTES

[1]Output current is limited by the maximum power dissipation in the package. See the power derating curves.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . . . 0.9 Watts
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin SOIC Package: θ_{JA} = 160°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8079 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8079 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

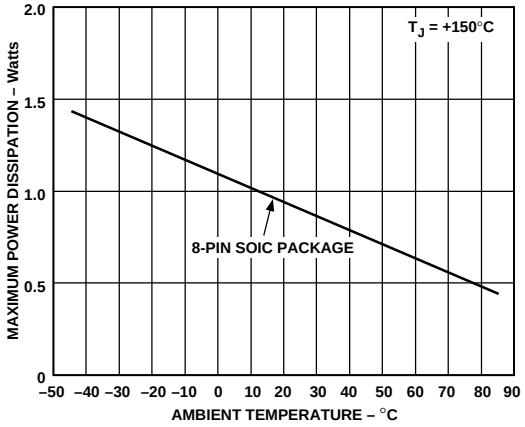


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Gain	Temperature Range	Package Description	Package Option
AD8079AR	G = +2.0	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD8079AR-REEL	G = +2.0	–40°C to +85°C	REEL SOIC	SO-8
AD8079AR-REEL7	G = +2.0	–40°C to +85°C	REEL 7 SOIC	SO-8
AD8079BR	G = +2.2	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD8079BR-REEL	G = +2.2	–40°C to +85°C	REEL SOIC	SO-8
AD8079BR-REEL7	G = +2.2	–40°C to +85°C	REEL 7 SOIC	SO-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8079 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

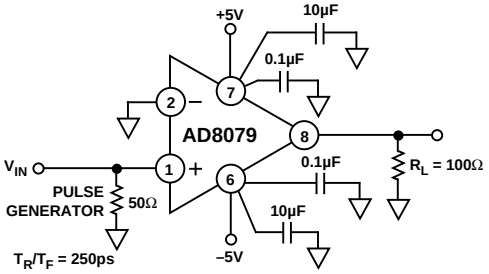


Figure 3. Test Circuit

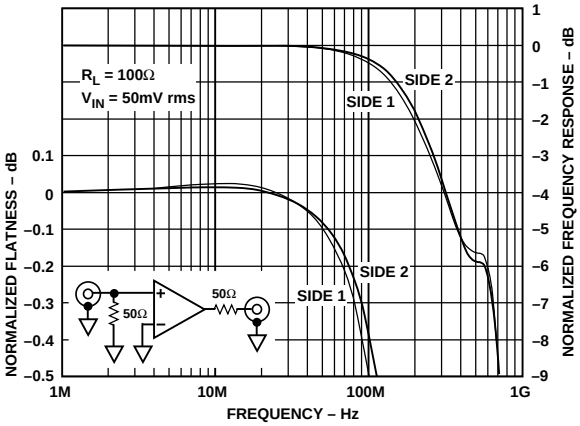


Figure 6. Frequency Response and Flatness

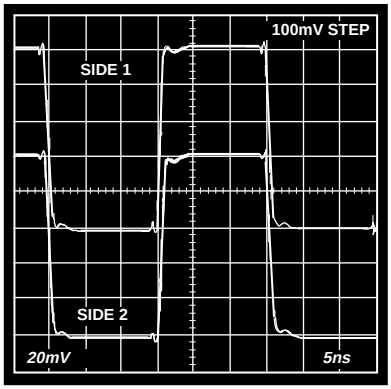


Figure 4. 100 mV Step Response

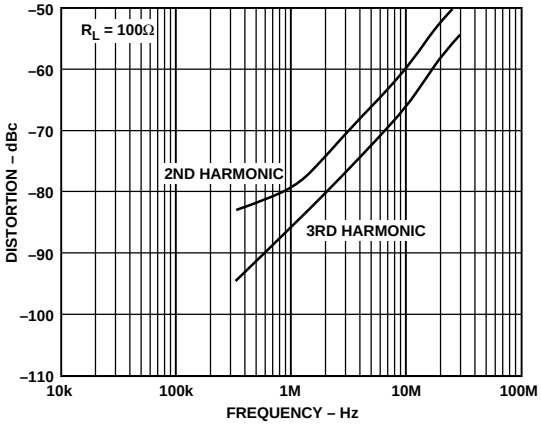


Figure 7. Distortion vs. Frequency, R_L = 100 Ω

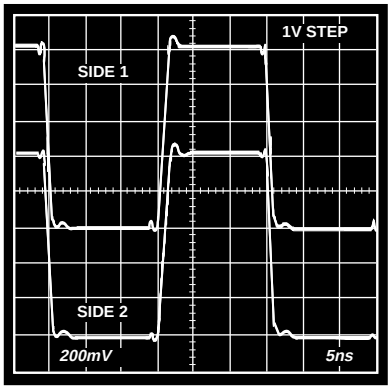


Figure 5. 1 V Step Response

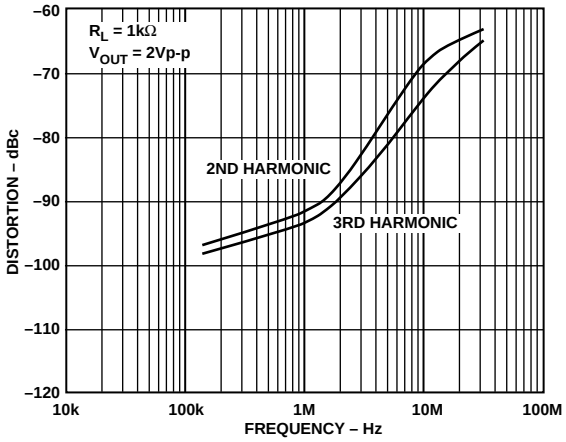


Figure 8. Distortion vs. Frequency, R_L = 1 kΩ

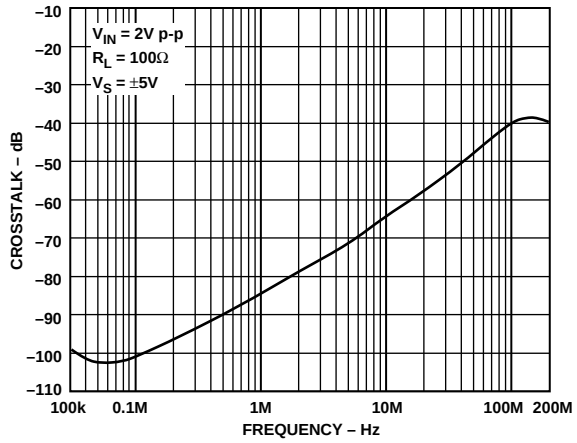


Figure 9. Crosstalk (Output-to-Output) vs. Frequency

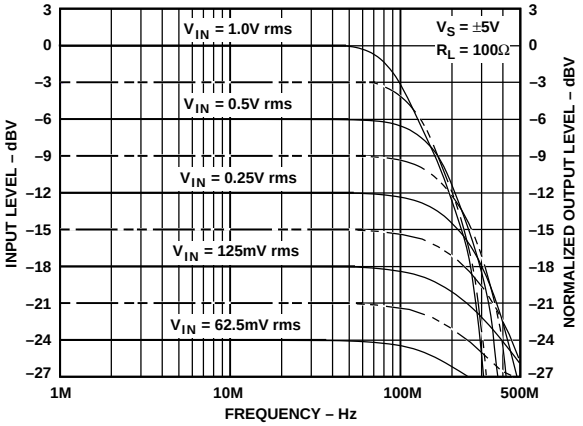


Figure 12. Large Signal Frequency Response

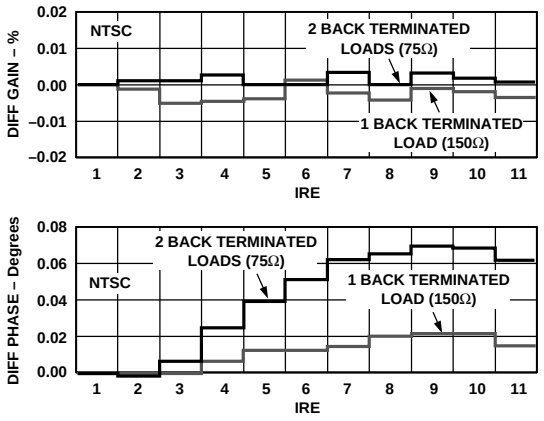


Figure 10. Differential Gain and Differential Phase (per Amplifier)

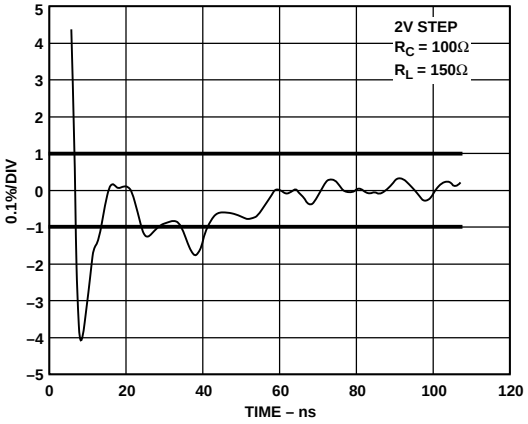
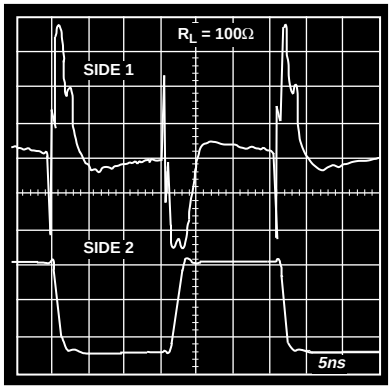


Figure 13. Short-Term Settling Time



NOTES: SIDE 1: V_{IN} = 0V; 8mV/div RTO
SIDE 2: 1V STEP RTO; 400mV/div

Figure 11. Pulse Crosstalk, Worst Case, 1 V Step

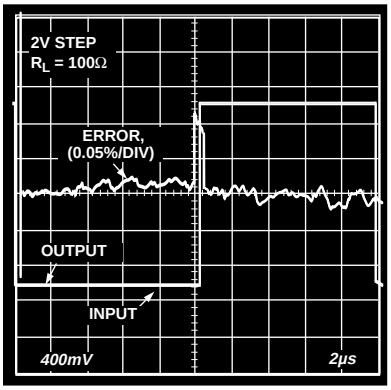


Figure 14. Long-Term Settling Time

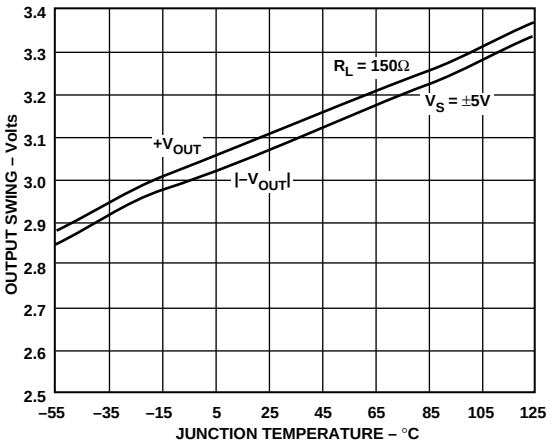


Figure 15. Output Swing vs. Temperature

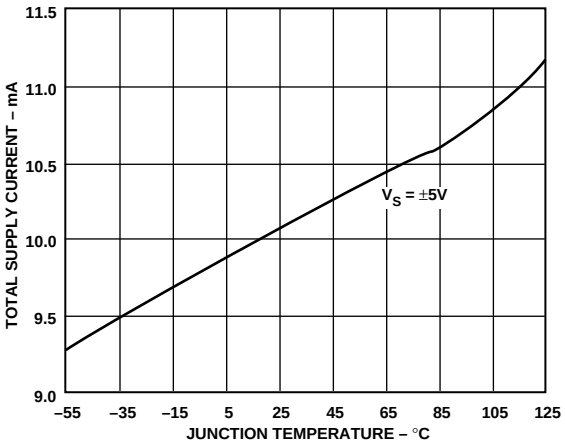


Figure 18. Total Supply Current vs. Temperature

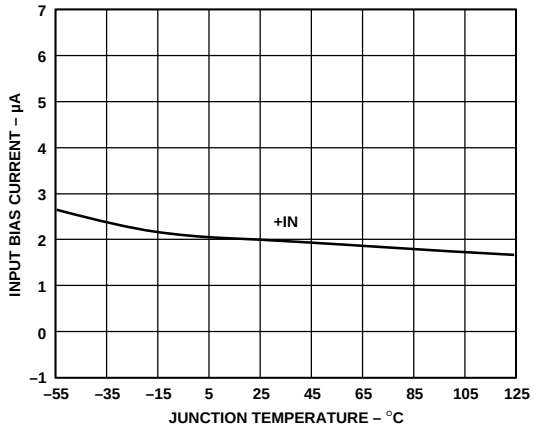


Figure 16. Input Bias Current vs. Temperature

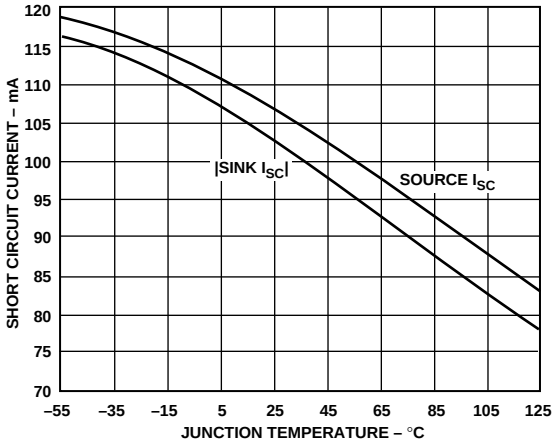


Figure 19. Short Circuit Current vs. Temperature

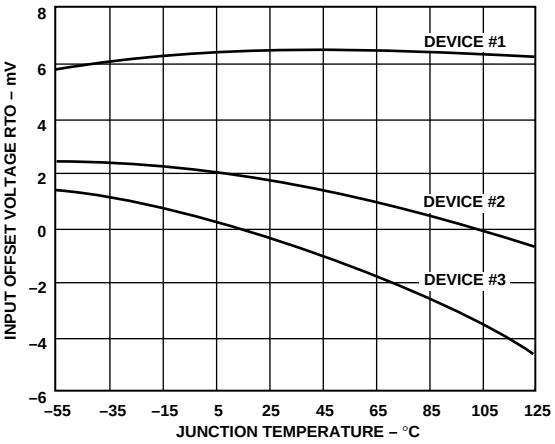


Figure 17. Input Offset Voltage vs. Temperature

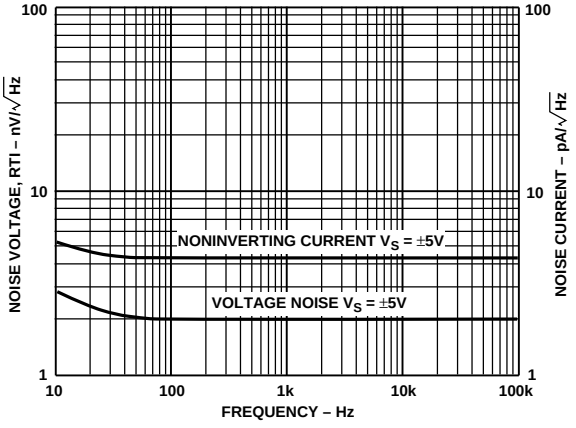


Figure 20. Noise vs. Frequency

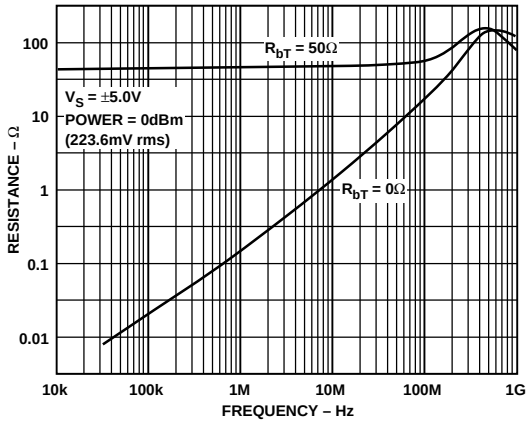


Figure 21. Output Resistance vs. Frequency

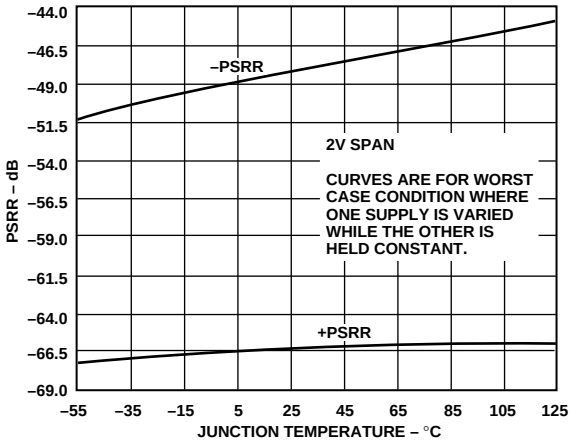


Figure 22. PSRR vs. Temperature

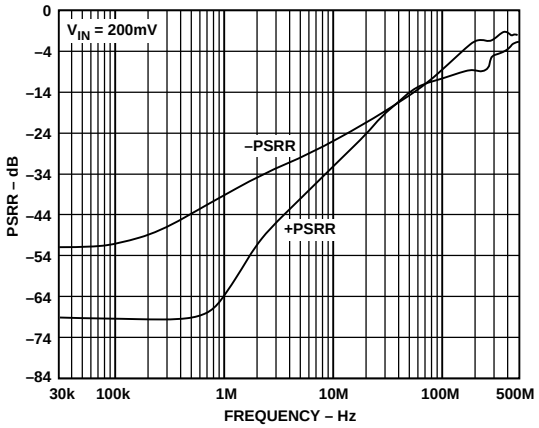


Figure 23. PSRR vs. Frequency

THEORY OF OPERATION

The AD8079, a dual current feedback amplifier, is internally configured for a gain of either +2 (AD8079A) or +2.2 (AD8079B). The internal gain-setting resistors effectively eliminate any parasitic capacitance associated with the inverting input pin, accounting for the AD8079's excellent gain flatness response. The carefully chosen pinout greatly reduces the crosstalk between each amplifier. Up to four back-terminated 75 Ω video loads can be driven by each amplifier, with a typical differential gain and phase performance of 0.01%/0.17°, respectively. The AD8079B, with a gain of +2.2, can be employed as a single gain-trimming element in a video signal chain. Finally, the AD8079A/B used in conjunction with our AD8116 crosspoint matrix, provides a complete turn-key solution to video distribution.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling. Line lengths on the order of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of 4.7 µF and 0.1 µF is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈ 4.7 Ω for optimum results.

DC Errors and Noise

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 24) they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain always appears at the output as $I_{BN} \times R_F$. The input voltage noise of the AD8079 is a low 2 nV/$\sqrt{\text{Hz}}$. At low gains though the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifications for the AD8079 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD8079 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BI} \times R_F$$

where:
$R_F = R_I = 750\ \Omega$ for AD8079A
$R_F = 750\ \Omega$, $R_I = 625\ \Omega$ for AD8079B

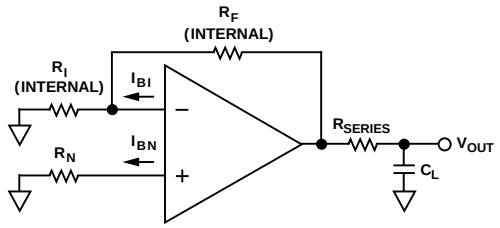


Figure 24. Output Offset Voltage

Driving Capacitive Loads

The AD8079 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series output resistance (R_{SERIES}). The graph in Figure 25 shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

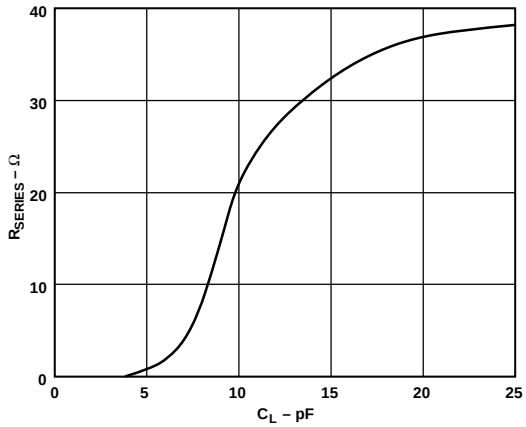


Figure 25. Recommended R_{SERIES} vs. Capacitive Load

Operation as a Video Line Driver

The AD8079 has been designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.02°) meet the most exacting HDTV demands for driving one video load with each amplifier. The AD8079 also drives four back terminated loads (two each), as shown in Figure 26, with equally impressive performance (0.01%, 0.07°). Another important consideration is isolation between loads in a multiple load application. The AD8079 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

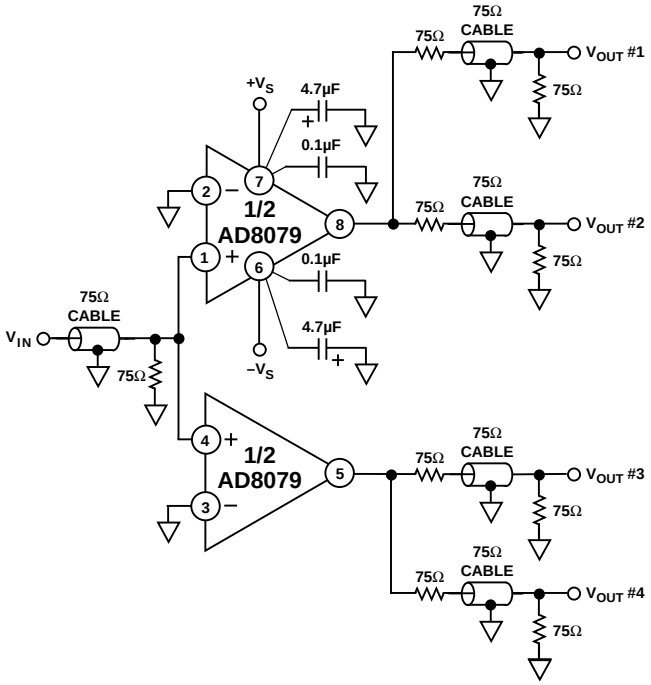


Figure 26. Video Line Driver

Single-Ended to Differential Driver Using an AD8079

The two halves of an AD8079 can be configured to create a single-ended to differential high speed driver with a –3 dB bandwidth in excess of 110 MHz as shown in Figure 27. Although the individual op amps are each current feedback with internal feedback resistors, the overall architecture yields a circuit with attributes normally associated with voltage feedback amplifiers, while offering the speed advantages inherent in current feedback amplifiers. In addition, the gain of the circuit can be changed by varying a single resistor, R_F, which is often not possible in a dual op amp differential driver.

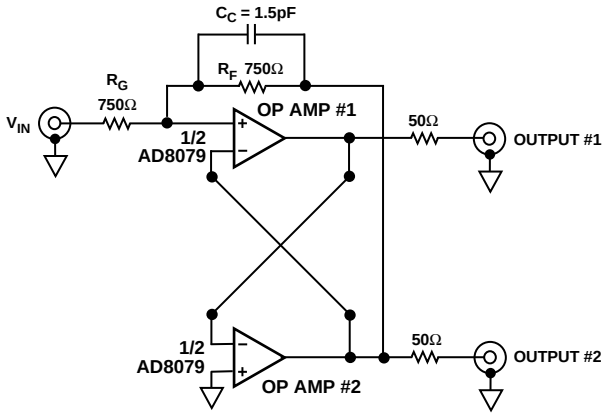


Figure 27. Differential Line Driver

The current feedback nature of the op amps, in addition to enabling the wide bandwidth, provides an output drive of more than 3 V p-p into a 20 Ω load for each output at 20 MHz. On the other hand, the voltage feedback nature provides symmetrical high impedance inputs and allows the use of reactive components in the feedback network.

The circuit consists of the two op amps each configured as a unity gain follower by the 750 Ω feedback resistors between each op amp's output and inverting input. The output of each op amp has a 750 Ω resistor to the inverting input of the other op amp. Thus, each output drives the other op amp through a unity gain inverter configuration. By connecting the two amplifiers as cross-coupled inverters, their outputs are free to be equal and opposite, assuring zero-output common-mode voltage.

With this circuit configuration, the common-mode signal of the outputs is reduced. If one output moves slightly higher, the negative input to the other op amp drives its output to go slightly lower and thus preserves the symmetry of the complementary outputs which reduces the common-mode signal.

The resulting architecture offers several advantages. First, the gain can be changed by changing a single resistor. Changing either R_F or R_G will change the gain as in an inverting op amp circuit. For most types of differential circuits, more than one resistor must be changed to change gain and still maintain good CMR.

Reactive elements can be used in the feedback network. This is in contrast to current feedback amplifiers that restrict the use of reactive elements in the feedback. The circuit described requires about 1.3 pF of capacitance in shunt across R_F in order to optimize peaking and realize a –3 dB bandwidth of more than 110 MHz.

The peaking exhibited by the circuit is very sensitive to the value of this capacitor. Parasitics in the board layout on the order of tenths of picofarads will influence the frequency response and the value required for the feedback capacitor, so a good layout is essential.

The shunt capacitor type selection is also critical. Good microwave type chip capacitors with high Q were found to yield best performance.

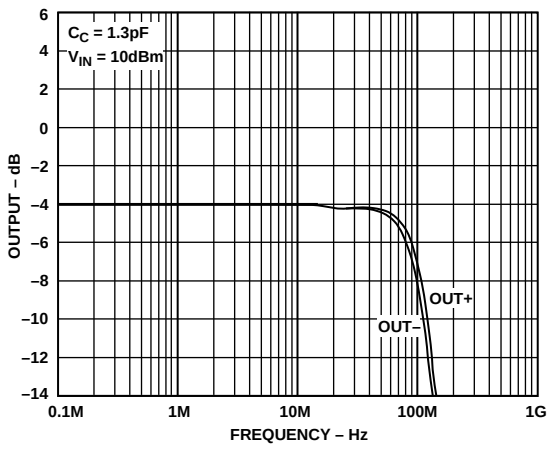


Figure 28. Differential Driver Frequency Response

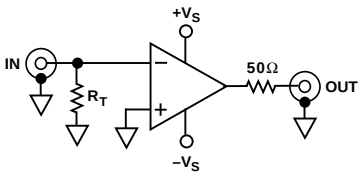
Layout Considerations

The specified high speed performance of the AD8079 requires careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

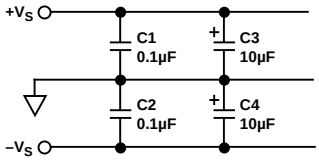
The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 29). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional large (4.7 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large-signal changes at the output.

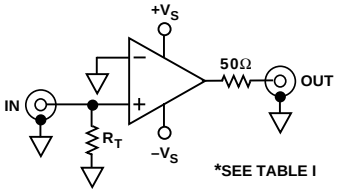
Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.



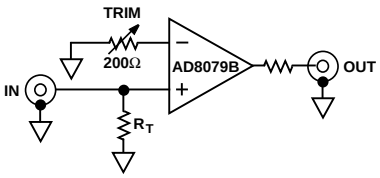
Inverting Configuration



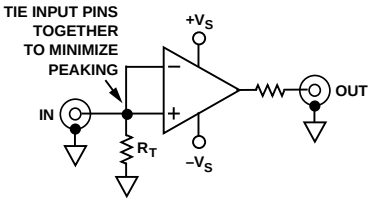
Supply Bypassing



Noninverting Configuration (G = +2)



Optional Gain Trim (G = +2 → +2.2)



Noninverting Configuration (G = +1)

Figure 29. Inverting and Noninverting Configurations

Table I. Recommended Component Values

Component	–1	+1	+2/+2.2
R_T (Nominal) (Ω)	53.6	49.9	49.9
Small Signal BW (MHz)	220	750	260
0.1 dB Flatness (MHz)	50	100	50

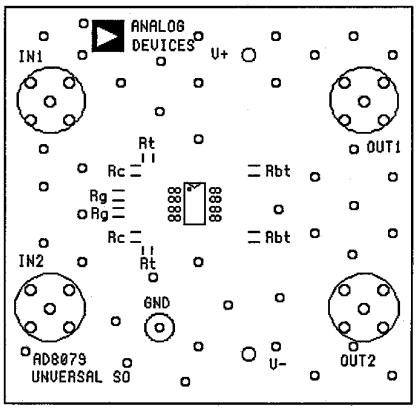


Figure 30. Board Layout (Silkscreen)

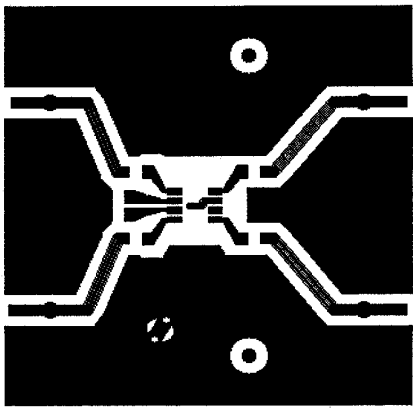


Figure 31. Board Layout (Component Layer)

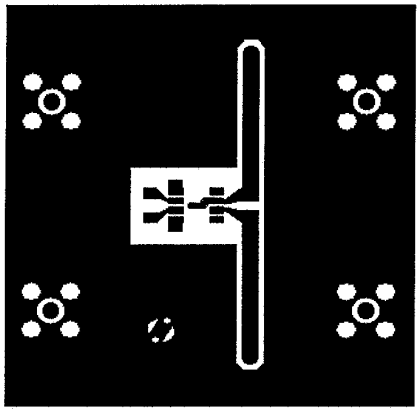
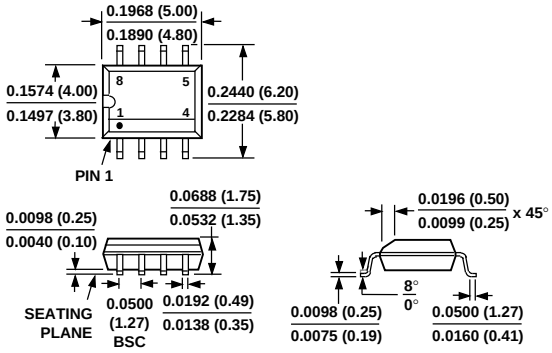


Figure 32. Board Layout (Solder Side; Looking Through the Board)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



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