Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4–Bit Counter Can Divide Independently in BCD or Binary
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- Schmitt Triggered Clock Conditioning 1725 G. G. D. M.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 2.)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

- 1. Maximum Ratings are those values beyond which damage to the device may occur.
- 2. Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



ON Semiconductor

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PDIP-16 P SUFFIX **CASE 648**



MARKING



TSSOP-16 **DT SUFFIX** CASE 948F





SOIC-16 DW SUFFIX **CASE 751G**



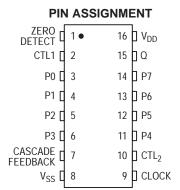
= Assembly Location

WL or L = Wafer Lot YY or Y = YearWW or W = Work Week

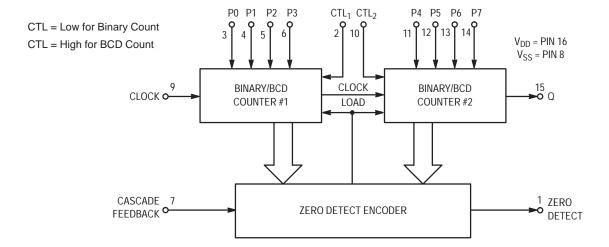
ORDERING INFORMATION

	Device	Package	Shipping
ı	MC14569BCP	PDIP-16	2000/Box
	MC14569BDT	TSSOP-16	96/Rail
	MC14569BDW	SOIC-16	47/Rail
	MC14569BDWR2	SOIC-16	1000/Tape & Reel





BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			V _{DD}	- 5	5°C		25°C		125	5°C	
Characteristic		Symbol	Vdc	Min	Max	Min	Typ ^(3.)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0 10 15	_ _ _	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	Source	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		I _{in}	15	_	±0.1	_	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	_ _ _	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current ^(4.) (5 (Dynamic plus Quiesce Per Package) (C _L = 50 pF on all outp buffers switching)	ent,	I _T	5.0 10 15			$I_{T} = (1$.58 μΑ/kHz) .20 μΑ/kHz) .95 μΑ/kHz)	f + I _{DD}			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$)

		V _{DD}				
Characteristic	Symbol	Vdc	Min	Typ ^(6.)	Max	Unit
Output Rise Time	tтLH	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Output Fall Time	t _{THL}	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Turn–On Delay Time Zero Detect Output	t _{PLH}	5.0 10 15	_ _ _	420 175 125	700 300 250	ns
Q Output		5.0 10 15	_ _ _	675 285 200	1200 500 400	ns
Turn–Off Delay Time Zero Detect Output	t _{PHL}	5.0 10 15	=	380 150 100	600 300 200	ns
Q Output		5.0 10 15	_ _ _	530 225 155	1000 400 300	ns
Clock Pulse Width	twн	5.0 10 15	300 150 115	100 45 30	_ _ _	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	_ _ _	3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15		NO LIMIT		μѕ

^{6.} Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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SWITCHING WAVEFORMS

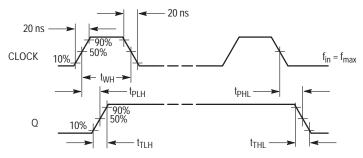


Figure 1.

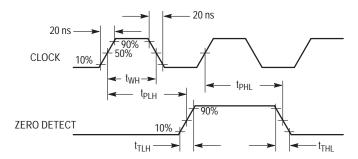


Figure 2.

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, **P5**, **P6**, **P7** (**Pins 11**, **12**, **13**, **14**) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (**Pin 1**) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL₁ (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL₂ (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

 V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

OPERATING CHARACTERISTICS

The MC14569B is a programmable divide–by–N dual 4–bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL₁ and CTL₂.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to $V_{\rm DD}$.

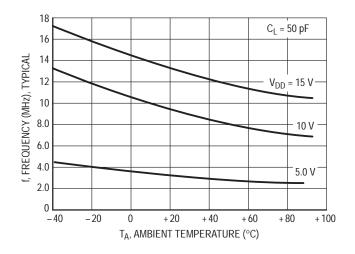


Table 1. Mode Controls (Cascade Feedback = Low)

Counter Co	ntrol Values	Divide Ratio			
CTL ₁	CTL ₂	Zero Detect	Q		
0	0	256	256		
0	1	160	160		
1	0	160	160		
1	1	100	100		

NOTE: Data Preset Inputs (P0–P7) are "Don't Cares" while Cascade Feedback is Low.

Table 2. Mode Controls ($CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High)$

			Preset	Inputs				Divide	Ratio	
P7	P6	P5	P4	Р3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
				•		•	•		X	
				•		•			X	
	١.			•		•			X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
	١.			•		•			X	
	١.			•		•			X	
	١.			•		•			X	
0	0	1	0	0	0	0	0	32	X	
				•		•	•		X	
				•		•			X	
				•		•	•		X	
0	1	0	0	0	0	0	0	64	X	
				•		•			X	
				•		•			X	
				•		•			X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	Q Output Active
	١.			•		•				
	١.			•		•				
	١.			•		•				
1	0	0	0	1	0	0	0	136	136	
				•		•	•			
	١.			•		•				
	١.			•		•				
1	1	1	1	1	1	1	1	255	255	*
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	20			
128	64	32 16 8 4 2 1				1			Bit Value	
	Counter #2 Counter #1							Counting		
	Bin	ary			Bin	ary				Sequence

X = No Output (Always Low)

Table 3. Mode Controls (CTL₁ = High, CTL₂ = Low, Cascade Feedback = High)

				Inputs	<u> </u>	•			Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	x	Min Count
0	0	0	0	0	0	1	1	3	x	
									x	
								•	x	
								•	x	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
	١ .			١ .	١ .	١ .		•	X	
		•	•				•	•	x	
	•	•		•	•	١ ٠		•	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
	•	•	•		•		•	•	X	
	٠ ا	•	•		٠ ا	•	•	•	X	
		•				•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
١ .	•	•	•	١ .	•	٠ ا	•	•	X X	
١.	•	•	•		•	١.	•	•	X	
0	1	0	0	0	0	0	0	• 40	X	
.	ł				ł	ł			X	
:					:	:			X	
:			`.	`	`	`	`.		X	
0	1	0	1	0	0	0	0	50	X	
	:		:					•	X	
١.	١.			١.	١.	١.			X	
١.	١.			١.			١.		x	
0	1	1	0	0	0	0	0	60	x	
	.				.				x	
								•	x	
		•						•	X	
0	1	1	1	0	0	0	0	70	X	
	•				•	١ .		•	X	
	•	•			•	٠ ا		•	x	
:		•	•					•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•		•	•	•	•	•	
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		•				•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
:	:		:	:	:	:	:	•	:	
:	:		:	:	:	:	:			
	1	1	1	0	0	0	0	• 150	150	
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1	1	1	1	1	0	0	1	159	159	\
80	80 40 20 10 8 4 2 1							•	Bit Value	
Counter #2 Counter #1									Counting	
										Sequence
	Binary BCD									·

X = No Output (Always Low)

Table 4. Mode Controls (CTL₁ = Low, CTL₂ = High, Cascade Feedback = High)

P7				Preset	Values			ou, o 12,		Ratio	ic – r ligity
O	P7	P6	P5	P4	P3	P2	P1	P0		Q	Comments
O	0	0	0	0	0	0	0	0			
O	0	0	0	0	0	0	0	1			Illegal State
			l .								Min Count
Counter#2 Counter#1 Counter #2 Counter #4 Count	0	0	0	0	0	0	1	1	3		
No	•			•		•	•	•	•		
0 0 0 0 1 0 0 0 1 1 1 1 1 1 1 5 X 0 0 0 0 1 0 0 1 0 0 0 0 0 16 X 1 0 0 0 1 1 0 0 0 0 0 16 X 2 0 0 0 0 1 1 1 1 1 1 1 31 X 0 0 0 0 1 1 1 1 1 1 1 31 X 0 0 0 1 1 0 0 0 0 0 0 32 X 2 0 0 0 1 1 1 0 0 0 0 0 48 X 3 0 0 0 1 1 1 0 0 0 0 0 48 X 4 0 0 0 1 1 1 0 0 0 0 0 48 X 5 0 0 0 1 1 1 0 0 0 0 0 0 64 X 6 0 1 0 0 0 0 0 0 0 0 64 X 7 0 0 1 0 0 0 0 0 0 0 64 X 8 0 0 0 1 0 0 0 0 0 0 0 64 X 9 0 0 1 0 0 0 0 0 0 0 64 X 9 0 0 1 0 0 0 0 0 0 0 64 X 9 0 0 1 0 0 1 0 0 0 0 0 80 X 9 0 0 1 0 1 0 0 0 0 0 0 80 X 9 0 0 1 1 1 0 0 0 0 0 0 112 X 9 0 0 1 1 1 1 0 0 0 0 0 0 112 X 9 0 0 1 1 1 1 0 0 0 0 0 112 X 9 0 0 1 1 1 1 1 0 0 0 0 0 112 X 9 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	•	•			ł						
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											Bit Value
		Coun	ter #2	•		Count	ter #1				Counting

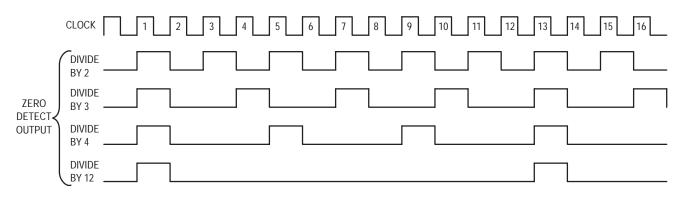
X = No Output (Always Low)

Table 5. Mode Controls $(CTL_1 = High, CTL_2 = High, Cascade Feedback = High)$

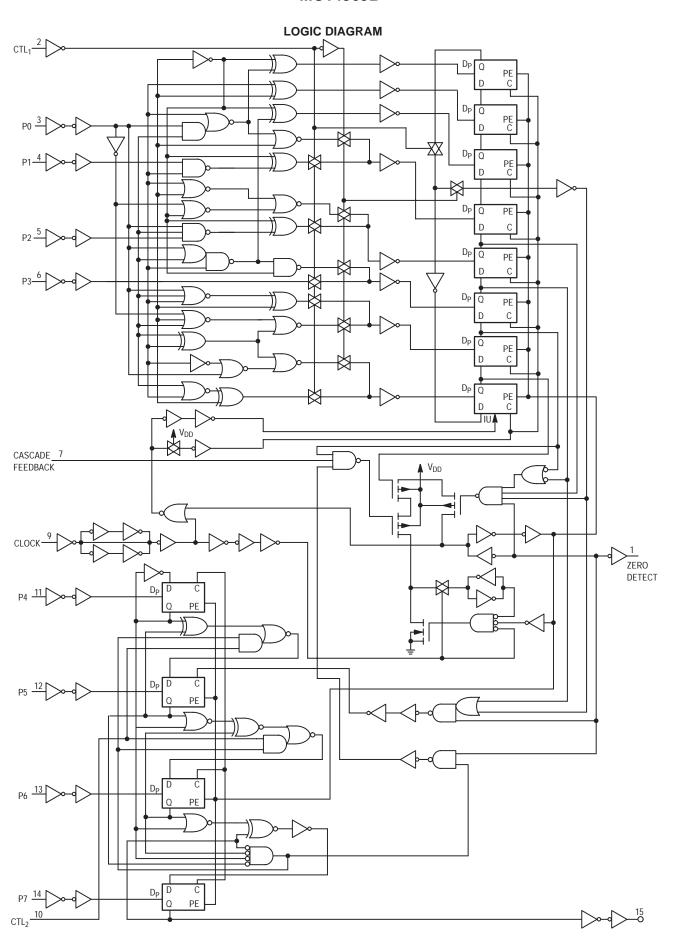
P7				Preset	Values				Divide	Ratio	
0	P7	P6	P5	P4	P3	P2	P1	P0		Q	Comments
O	0	0		0		0		0			
0	0	0	0	0		0	0	1	Х		
	0	0	0	0		0	1	0			Min Count
	0	0	0	0	0	0	1	1	3		
	•		•	•		•	•	•	•		
0 0 0 1 0 0 1 9 X 0 0 0 1 0 0 10 X X X X 0 0 1 1 0 0 0 30 X X X X .	•	•	•		•	•	•	•	•		
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1 0 0 1 0 0 1 99 99 ♥ 80 40 20 10 8 4 2 1 Bit Value	•		•		•			•			
80 40 20 10 8 4 2 1 Bit Value	•				•	.	•	•	•		
	1	0	0	1	1	0	0	1	99	99	*
Counter #2 Counter #1 Counter	80	40	20	10	8	4	2	1			Bit Value
BCD BCD Sequence		Counter #2 Counter #1 BCD BCD								Counting Sequence	

X = No Output (Always Low)

TIMING DIAGRAM MC14569B



http://onsomi.com



TYPICAL APPLICATIONS

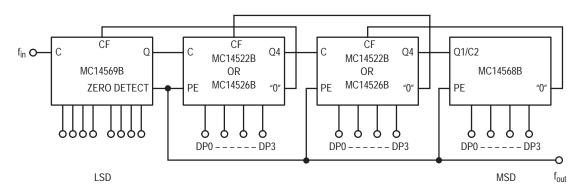


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

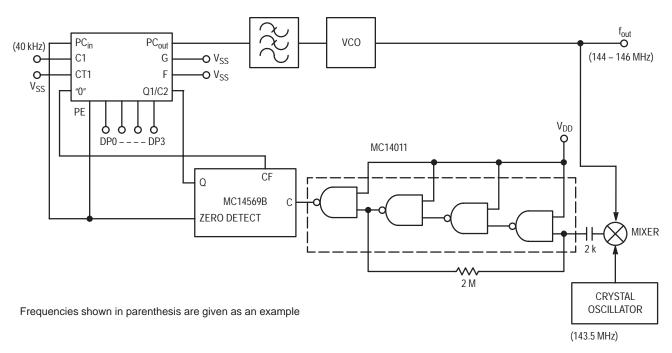
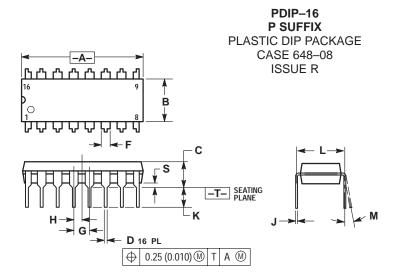


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

PACKAGE DIMENSIONS



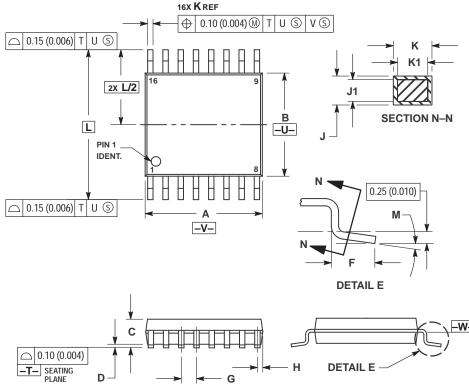
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27	BSC
٦	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

TSSOP-16 **DT SUFFIX**

PLASTIC TSSOP PACKAGE CASE 948F-01 **ISSUE O**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.

 - 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM

 - PROTRUSION SHALL BE JOB (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

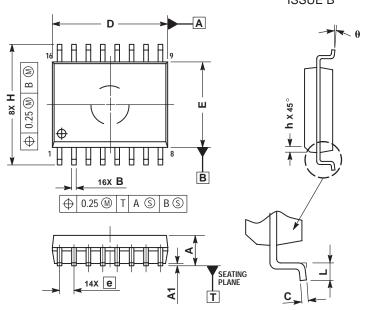
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W-.

	IVIILLIIV	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.18	0.28	0.007	0.011	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252		
M	0°	8°	0°	8°	

PACKAGE DIMENSIONS

SOIC-16 **DW SUFFIX** PLASTIC SOIC PACKAGE CASE 751G-03 **ISSUE B**



- NOTES:

 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS
DIM	MIN	MAX
Α	2.35	2.65
A1	0.10	0.25
В	0.35	0.49
С	0.23	0.32
D	10.15	10.45
Ε	7.40	7.60
е	1.27	BSC
Н	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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