CMOS 1.8 V to 5.5 V, 2.5 Ω SPDT Switch/2:1 Mux In Tiny SC70 Package

ADG779

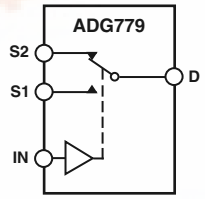
FEATURES

1.8 V to 5.5 V Single Supply
2.5 Ω On Resistance
0.75 Ω On-Resistance Flatness
–3 dB Bandwidth >200 MHz
Rail-to-Rail Operation
6-Lead SC70 Package
Fast Switching Times
  t_{ON} 20 ns
  t_{OFF} 6 ns
Typical Power Consumption (<0.01 μW)
TTL/CMOS-Compatible

APPLICATIONS

Battery-Powered Systems
Communication Systems
Sample Hold Systems
Audio Signal Routing
Video Switching
Mechanical Reed Relay Replacement

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR
A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG779 is a monolithic CMOS SPDT (single-pole, double-throw) switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The ADG779 operates from a single supply range of 1.8 V to 5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices.

Each switch of the ADG779 conducts equally well in both directions when on. The ADG779 exhibits break-before-make switching action.

Because of the advanced submicron process, –3 dB bandwidth of greater than 200 MHz can be achieved.

The ADG779 is available in a 6-lead SC70 package.

PRODUCT HIGHLIGHTS

1. Tiny 6-Lead SC70 Package.
2. 1.8 V to 5.5 V Single Supply Operation. The ADG779 offers high performance, including low on resistance and fast switching times, and is fully specified and guaranteed with 3 V and 5 V supply rails.
3. Very Low R_{ON} (5 Ω max at 5 V, 10 Ω max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
4. On-Resistance Flatness ($R_{FLAT(ON)}$) (0.75 Ω typ).
5. –3 dB Bandwidth >200 MHz.
6. Low Power Dissipation. CMOS construction ensures low power dissipation.
7. 14 ns Switching Times.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com

ADG779–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2 .5		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA,
	5	6	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})		0.1	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
		1.2	Ω max	
LEAKAGE CURRENTS[2]				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01	±0.05	nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V, Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01	±0.05	nA typ	V_S = V_D = 1 V, or V_S = V_D = 4.5 V, Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	14		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns max	V_S = 3 V, Test Circuit 4
t_{OFF}	3		ns typ	R_L = 300 Ω, C_L = 35 pF
		6	ns max	V_S = 3 V, Test Circuit 4
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF,
		1	ns min	V_{S1} = V_{S2} = 3 V, Test Circuit 5
Off Isolation	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 6
Channel-to-Channel Crosstalk	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 7
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
C_S (OFF)	7		pF typ	f = 1 MHz
C_D, C_S (ON)	27		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.001		µA typ	
		1.0	µA max	

NOTES

[1]Temperature ranges are as follows: B Version, –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6	7	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA,
		10	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})		0.1	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		2.5	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
LEAKAGE CURRENTS[2]				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01	±0.05	nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01	±0.05	nA typ	V_S = V_D = 1 V, or V_S = V_D = 3 V, Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	16		ns typ	R_L = 300 Ω, C_L = 35 pF
		24	ns max	V_S = 2 V, Test Circuit 4
t_{OFF}	4		ns typ	R_L = 300 Ω, C_L = 35 pF
		7	ns max	V_S = 2 V, Test Circuit 4
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V, Test Circuit 5
Off Isolation	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 6
Channel-to-Channel Crosstalk	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 7
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
C_S (OFF)	7		pF typ	f = 1 MHz
C_D, C_S (ON)	27		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V Digital Inputs = 0 V or 3 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

NOTES

[1]Temperature ranges are as follows: B Version, –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog, Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
SC70 Package, Power Dissipation . . . . . 315 mW
θ_{JA} Thermal Impedance . . . . . 332°C/W
θ_{JC} Thermal Impedance . . . . . 120°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

NOTES

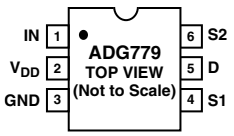
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

ADG779 IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

PIN CONFIGURATION
6-Lead SC70



TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels i.e., R_{ON} max – R_{ON} min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the switch "ON."
V_D (V_S)	Analog Voltage on Terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
On Response	The frequency response of the "ON" switch.
On Loss	The loss due to the "ON" resistance of the switch.

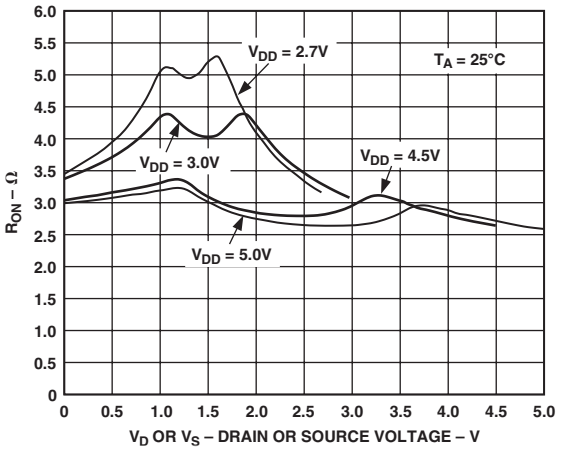
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information*
ADG779BKS	–40°C to +85°C	SC70 (Plastic Surface Mount)	KS-6	SKB

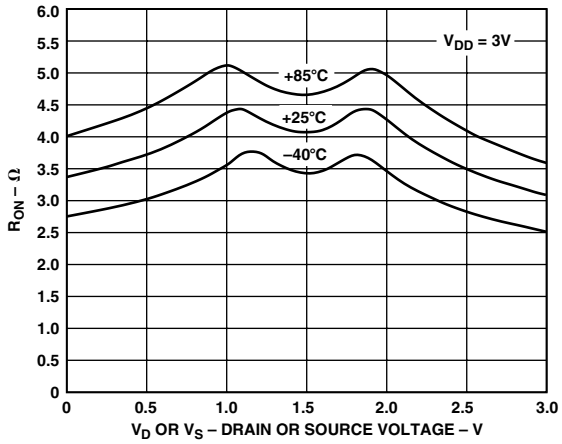
*Brand = Brand on these packages is limited to three characters due to space constraints.

CAUTION

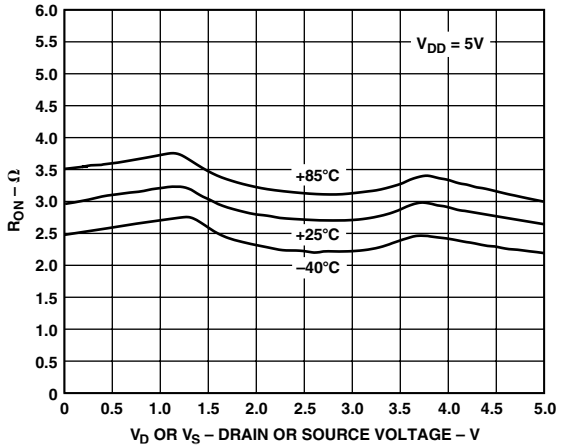
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG779 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



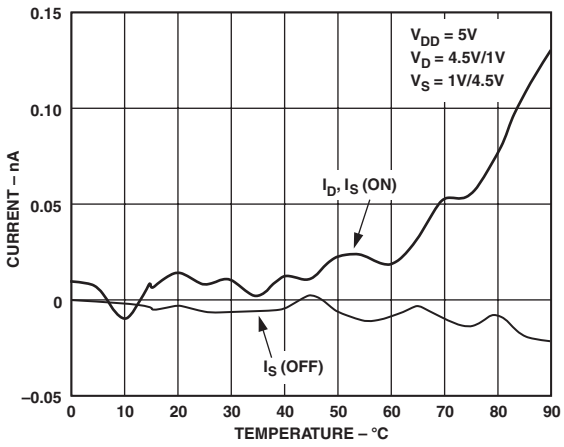
TPC 1. On Resistance as a Function of V_D (V_S) Single Supplies



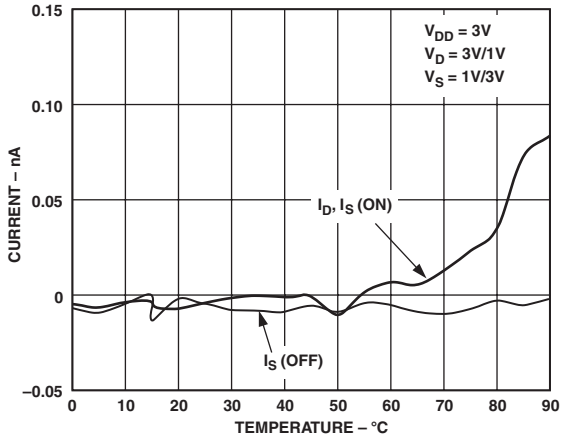
TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 3 V



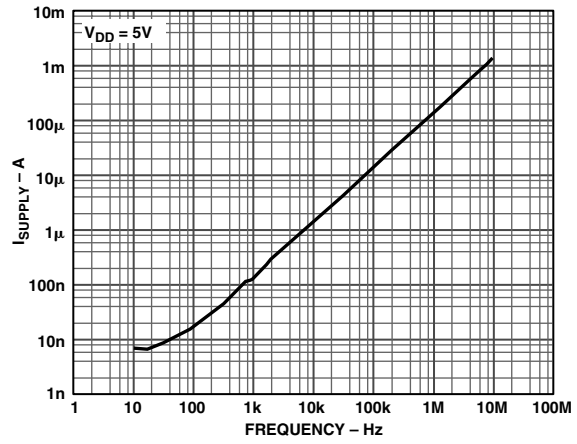
TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 5 V



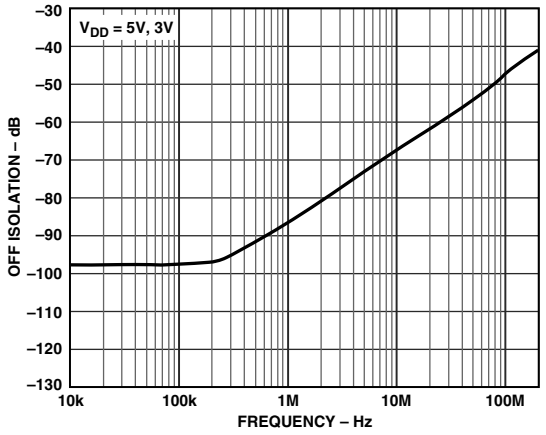
TPC 4. Leakage Currents as a Function of Temperature



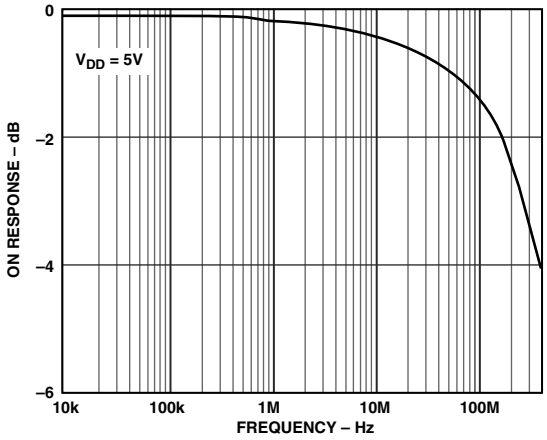
TPC 5. Leakage Currents as a Function of Temperature



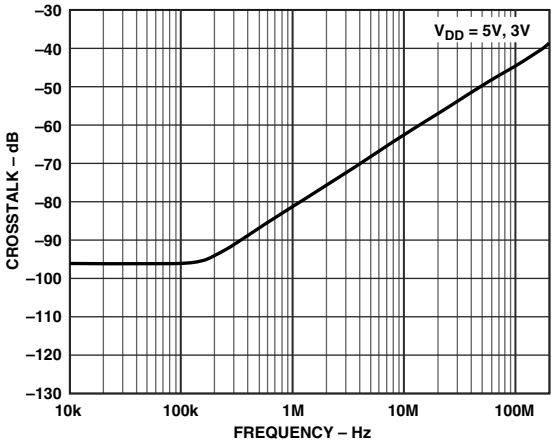
TPC 6. Supply Current vs. Input Switching Frequency



TPC 7. Off Isolation vs. Frequency

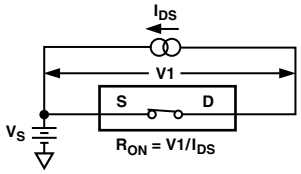


TPC 9. On Response vs. Frequency

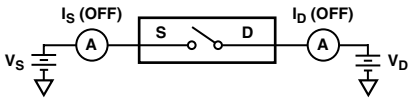


TPC 8. Crosstalk vs. Frequency

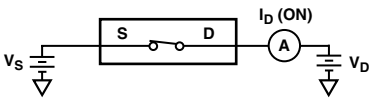
Test Circuits



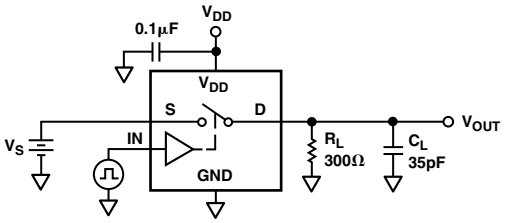
Test Circuit 1. On Resistance

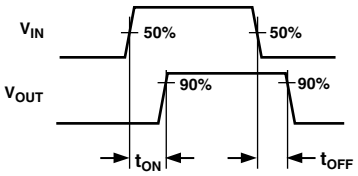


Test Circuit 2. Off Leakage

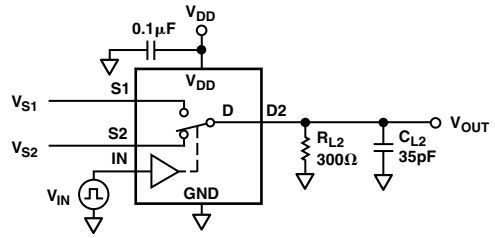


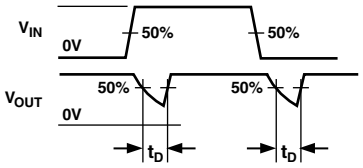
Test Circuit 3. On Leakage



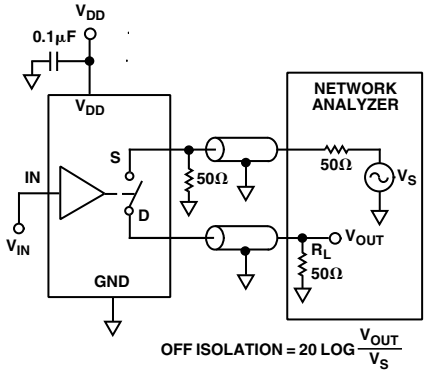


Test Circuit 4. Switching Times

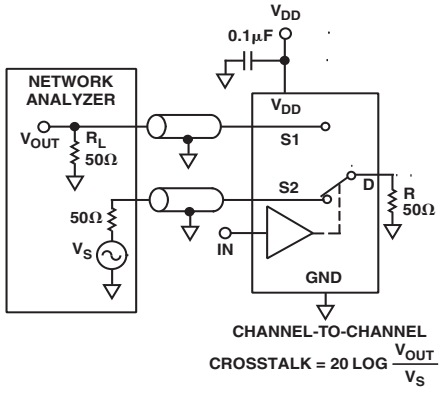




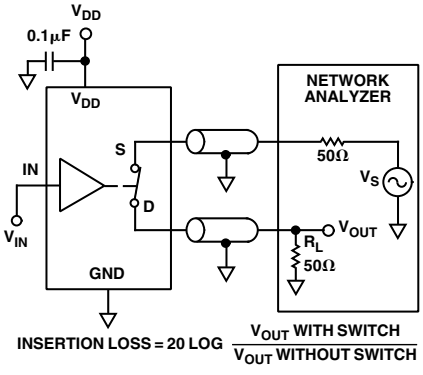
Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk

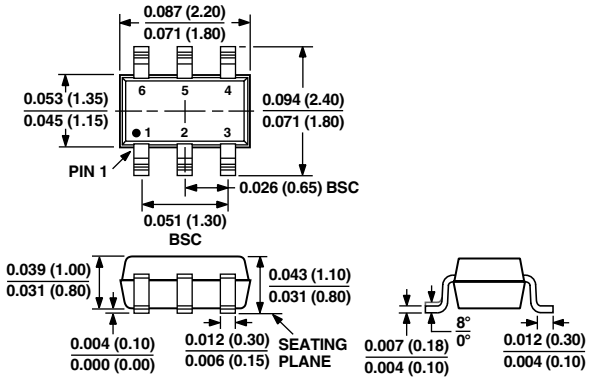


Test Circuit 8. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Plastic Surface Mount Package (SC70)
(KS-6)



C02491–1.5–7/01(0)

PRINTED IN U.S.A.