



CMOS Low Voltage 4 Ω SPDT Switch

ADG719

FEATURES

- +1.8 V to +5.5 V Single Supply
- 4 Ω (Max) On Resistance
- 0.75 Ω (Typ) On-Resistance Flatness
- 3 dB Bandwidth >200 MHz
- Rail-to-Rail Operation
- 6-Lead SOT-23 Package, 8-Lead μ SOIC Package
- Fast Switching Times

t_{ON} 20 ns

t_{OFF} 6 ns

Typical Power Consumption (<0.01 μ W)

TTL/CMOS Compatible

APPLICATIONS

- Battery Powered Systems
- Communication Systems
- Sample Hold Systems
- Audio Signal Routing
- Video Switching
- Mechanical Reed Relay Replacement

GENERAL DESCRIPTION

The ADG719 is a monolithic CMOS SPDT switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

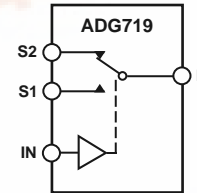
The ADG719 can operate from a single supply range of +1.8 V to +5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices.

Each switch of the ADG719 conducts equally well in both directions when on. The ADG719 exhibits break-before-make switching action.

Because of the advanced submicron process, -3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG719 is available in a 6-lead SOT-23 package and an 8-lead μ SOIC package.

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V Single Supply Operation. The ADG719 offers high performance, including low on resistance and fast switching times and is fully specified and guaranteed with +3 V and +5 V supply rails.
2. Very Low R_{ON} (4 Ω max at 5 V, 10 Ω max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
3. On-Resistance Flatness ($R_{FLAT(ON)}$) (0.75 Ω typ).
4. -3 dB Bandwidth >200 MHz.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF} .
7. Tiny 6-lead SOT-23 and 8-lead μ SOIC packages.

REV. A

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ADG719—SPECIFICATIONS¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.)

| Parameter | B Version | | Units | Test Conditions/Comments |
|--|------------|-----------------|-------------------|---|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 4 | 5 | Ω max | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ Test Circuit 1 |
| On Resistance Match Between Channels (ΔR_{ON}) | | 0.1 | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| | | 0.4 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.75 | | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| | | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 | | nA typ | $V_{DD} = +5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$ Test Circuit 2 |
| | ± 0.25 | ± 0.35 | nA max | |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 | | nA typ | $V_S = V_D = 1\text{ V}$, or $V_S = V_D = 4.5\text{ V}$ Test Circuit 3 |
| | ± 0.25 | ± 0.35 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 14 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4 |
| | | 20 | ns max | |
| t_{OFF} | 3 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4 |
| | | 6 | ns max | |
| Break-Before-Make Time Delay, t_D | 8 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5 |
| | | 1 | ns min | |
| Off Isolation | -67 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 6 |
| | -87 | | dB typ | |
| Channel-to-Channel Crosstalk | -62 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 7 |
| | -82 | | dB typ | |
| Bandwidth -3 dB | 200 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 8 |
| C_S (OFF) | 7 | | pF typ | |
| C_D , C_S (ON) | 27 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5 V |
| | | 1.0 | μA max | |

NOTES

¹Temperature ranges are as follows: B Version, -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹ ($V_{DD} = +3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.)

| Parameter | B Version | | Units | Test Conditions/Comments |
|--|--------------------------|-----------------|--|---|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 6 | 7 10 | Ω typ Ω max | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$, Test Circuit 1 |
| On Resistance Match Between Channels (ΔR_{ON}) | | 0.1 0.4 | Ω typ Ω max | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | | 2.5 | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 ± 0.25 | ± 0.35 | nA typ nA max | $V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$, Test Circuit 2 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 ± 0.25 | ± 0.35 | nA typ nA max | $V_S = V_D = 1\text{ V}$, or $V_S = V_D = 3\text{ V}$, Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.4 | V max | |
| Input Current I_{INL} or I_{INH} | 0.005 | ± 0.1 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 16 | 24 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 4 |
| t_{OFF} | 4 | 7 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 4 |
| Break-Before-Make Time Delay, t_D | 8 | 1 | ns typ ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 2\text{ V}$, Test Circuit 5 |
| Off Isolation | -67 -87 | | dB typ dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 6 |
| Channel-to-Channel Crosstalk | -62 -82 | | dB typ dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 7 |
| Bandwidth -3 dB | 200 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 8 |
| C_S (OFF) | 7 | | pF typ | |
| C_D , C_S (ON) | 27 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | 1.0 | μA typ μA max | $V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3 V |

NOTES¹Temperature ranges are as follows: B Version, -40°C to $+85^\circ\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG719

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

| | |
|-------------------------------------|---|
| V _{DD} to GND | -0.3 V to +7 V |
| Analog, Digital Inputs ² | -0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First |
| Peak Current, S or D | 100 mA (Pulsed at 1 ms, 10% Duty Cycle max) |
| Continuous Current, S or D | 30 mA |
| Operating Temperature Range | |
| Industrial (B Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | +150°C |
| μSOIC Package, Power Dissipation | 315 mW |
| θ _{JA} Thermal Impedance | 206°C/W |
| θ _{JC} Thermal Impedance | 44°C/W |
| SOT-23 Package, Power Dissipation | 282 mW |
| θ _{JA} Thermal Impedance | 229.6°C/W |
| θ _{JC} Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | +215°C |
| Infrared (15 sec) | +220°C |
| ESD | 1 kV |

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

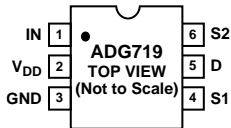
²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

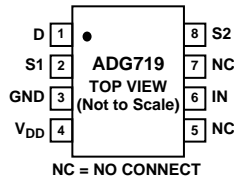
| ADG719 IN | Switch S1 | Switch S2 |
|-----------|-----------|-----------|
| 0 | ON | OFF |
| 1 | OFF | ON |

PIN CONFIGURATIONS

**6-Lead SOT-23
(RT-6)**



**8-Lead μSOIC
(RM-8)**



ORDERING GUIDE

| Model | Temperature Range | Brand* | Package Description | Package Option |
|-----------|-------------------|--------|--------------------------------|----------------|
| ADG719BRM | -40°C to +85°C | S5B | μSOIC (microSmall Outline IC) | RM-8 |
| ADG719BRT | -40°C to +85°C | S5B | SOT-23 (Plastic Surface Mount) | RT-6 |

*Brand = Due to package size limitations, these three characters represent the part number.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG719 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

| | |
|--------------------------------------|--|
| V _{DD} | Most Positive Power Supply Potential. |
| GND | Ground (0 V) Reference. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| IN | Logic Control Input. |
| R _{ON} | Ohmic resistance between D and S. |
| ΔR _{ON} | On resistance match between any two channels i.e., R _{ON} max – R _{ON} min. |
| R _{FLAT(ON)} | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| I _S (OFF) | Source Leakage Current with the switch “OFF.” |
| I _D , I _S (ON) | Channel Leakage Current with the switch “ON.” |
| V _D (V _S) | Analog Voltage on Terminals D, S. |
| C _S (OFF) | “OFF” Switch Source Capacitance. |
| C _D (OFF) | “OFF” Switch Drain Capacitance. |
| C _D , C _S (ON) | “ON” Switch Capacitance. |
| t _{ON} | Delay between applying the digital control input and the output switching on. |
| t _{OFF} | Delay between applying the digital control input and the output switching off. |
| t _D | “OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A measure of unwanted signal coupling through an “OFF” switch. |
| Bandwidth | The frequency at which the output is attenuated by -3 dBs. |
| On Response | The frequency response of the “ON” switch. |
| On Loss | The voltage drop across the “ON” switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0 dB at very low frequencies. |



Typical Performance Characteristics—ADG719

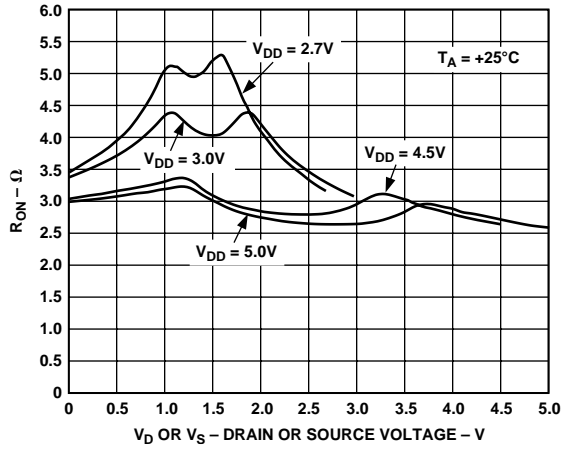


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

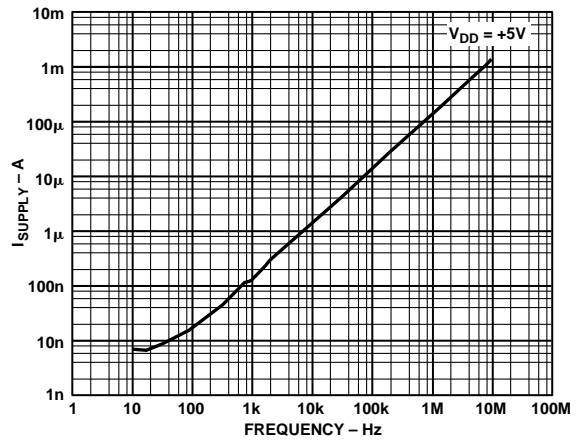


Figure 4. Supply Current vs. Input Switching Frequency

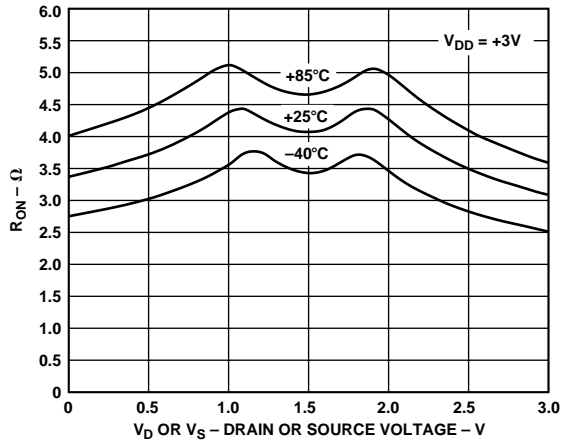


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 3V$

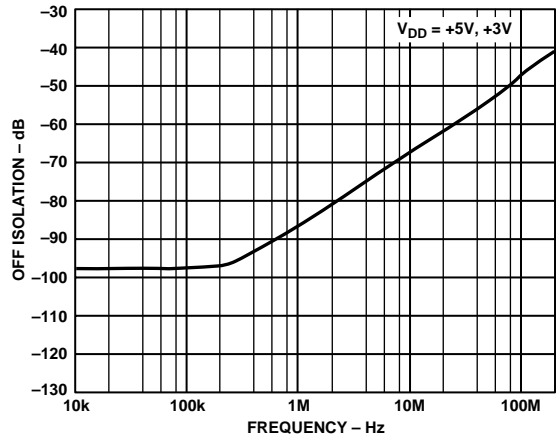


Figure 5. Off Isolation vs. Frequency

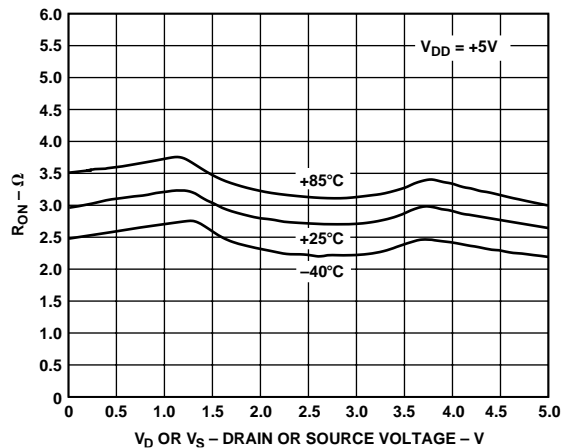


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 5V$

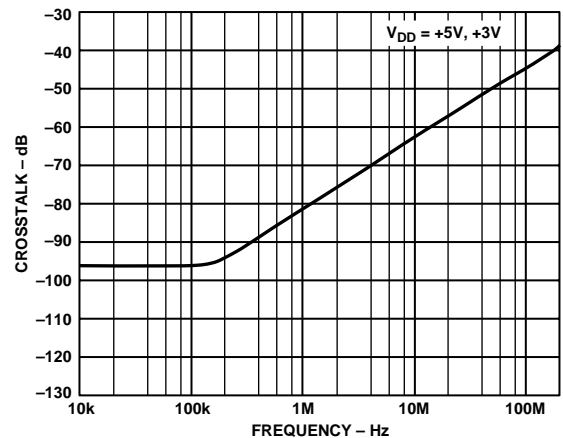


Figure 6. Crosstalk vs. Frequency

ADG719

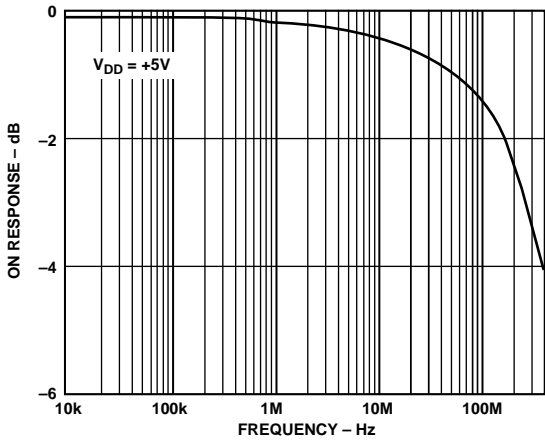
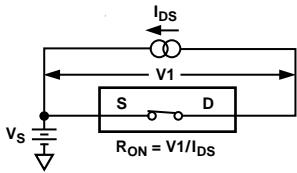
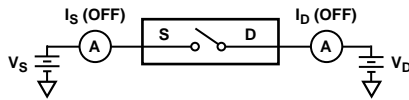


Figure 7. On Response vs. Frequency

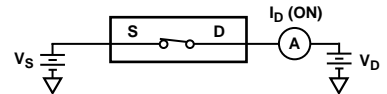
Test Circuits



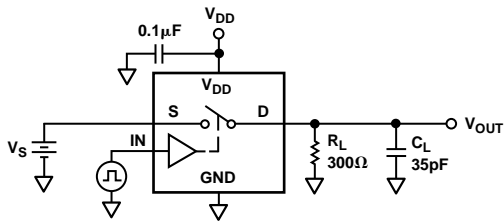
Test Circuit 1. On Resistance



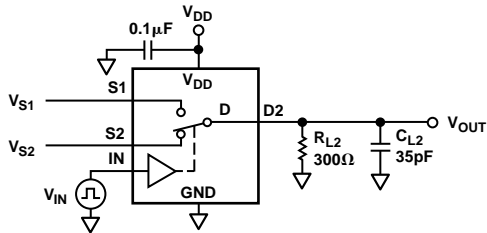
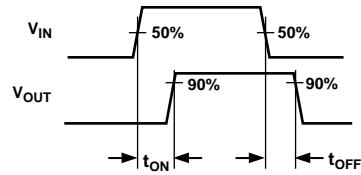
Test Circuit 2. Off Leakage



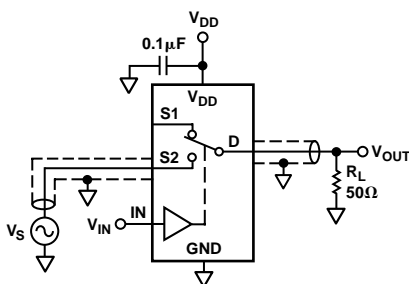
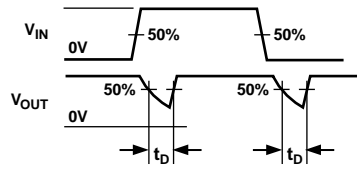
Test Circuit 3. On Leakage



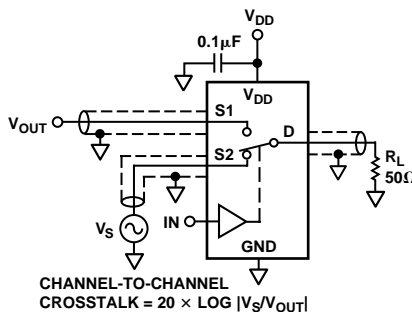
Test Circuit 4. Switching Times



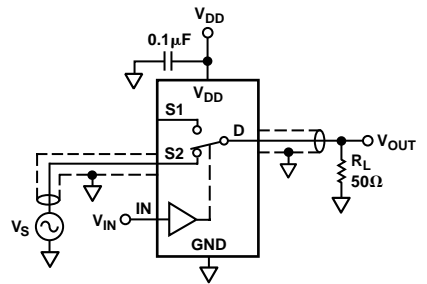
Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Bandwidth

APPLICATIONS INFORMATION

The ADG719 belongs to Analog Devices' new family of CMOS switches. This series of general purpose switches have improved switching times, lower on resistance, higher bandwidths, low power consumption and low leakage currents.

ADG719 Supply Voltages

Functionality of the ADG719 extends from +1.8 V to +5.5 V single supply, which makes it ideal for battery powered instruments, where important design parameters are power efficiency and performance.

It is important to note that the supply voltage effects the input signal range, the on resistance and the switching times of the part. By taking a look at the typical performance characteristics and the specifications, the effects of the power supplies can be clearly seen.

For $V_{DD} = +1.8$ V operation, R_{ON} is typically 40 Ω over the temperature range.

On Response vs. Frequency

Figure 8 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances will further degrade some performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

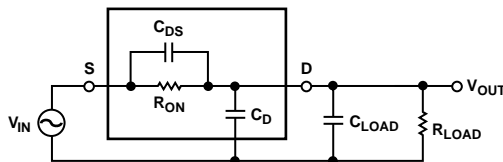


Figure 8. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 8) is of the form $A(s)$ shown below.

$$A(s) = R_T \left[\frac{s(R_{ON} C_{DS}) + 1}{s(R_T R_{ON} C_T) + 1} \right]$$

where:

$$R_T = R_{LOAD} / (R_{LOAD} + R_{ON})$$

$$C_T = C_{LOAD} + C_D + C_{DS}$$

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS} . This capacitance creates a frequency zero in the numerator of the transfer function $A(s)$. Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with C_{DS} and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of $A(s)$.

The dominant effect of the output capacitance, C_D , causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth a switch must have a low input and output capacitance and low on resistance. The On Response vs. Frequency plot for the ADG719 can be seen in Figure 7.

Off Isolation

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, C_{DS} , couples the input signal to the output load, when the switch is off as shown in Figure 9.

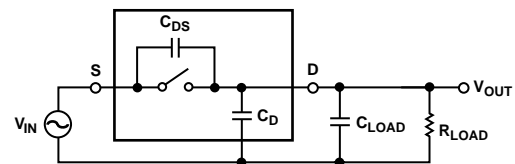


Figure 9. Off Isolation Is Affected by External Load Resistance and Capacitance

The larger the value of C_{DS} , larger values of feedthrough will be produced. The typical performance characteristic graph of Figure 5 illustrates the drop in off isolation as a function of frequency. From dc to roughly 200 kHz, the switch shows better than -95 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than -67 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest C_{DS} as possible. The values of load resistance and capacitance affect off isolation also, as they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

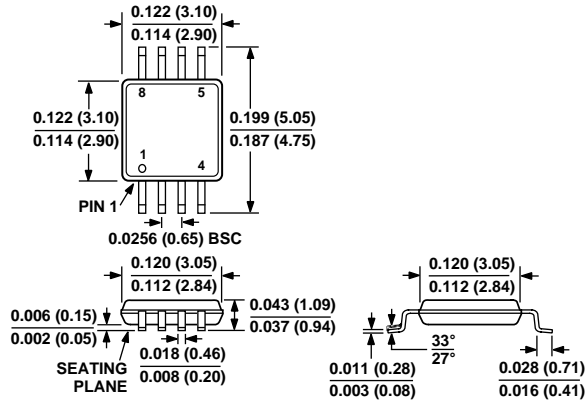
$$A(s) = \left[\frac{s(R_{LOAD} C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1} \right]$$

ADG719

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μ SOIC (RM-8)



6-Lead Plastic Surface Mount Package (RT-6)

