19-2274; Rev 0; 1/02

MAXIM

Dual LVDS Line Receiver

General Description

The MAX9159 dual low-voltage differential signaling (LVDS) receiver is ideal for applications requiring high speed, low power, and low noise. The MAX9159 is pin compatible with the SN65LVDS9637. The MAX9159 conforms to the ANSI TIA/EIA-644 LVDS standard and converts LVDS to LVTTL-compatible outputs. A fail-safe feature sets the output high when the inputs are undriven and open, terminated, or shorted. The MAX9159 is available in an 8-pin SO package and fully specified for the -40°C to +85°C extended temperature range.

Refer to the MAX9111/MAX9113 data sheet for higher performance single/dual LVDS line receivers in SOT23 and SO packages. Refer to the MAX9110/MAX9112 data sheet for single/dual LVDS line drivers in SOT23 and SO packages.

Applications

Network Switches/Routers
Telecom Switching Equipment
Cellular Phone Base Stations
Digital Copiers
LCD Displays
Backplane Interconnect
Clock Distribution

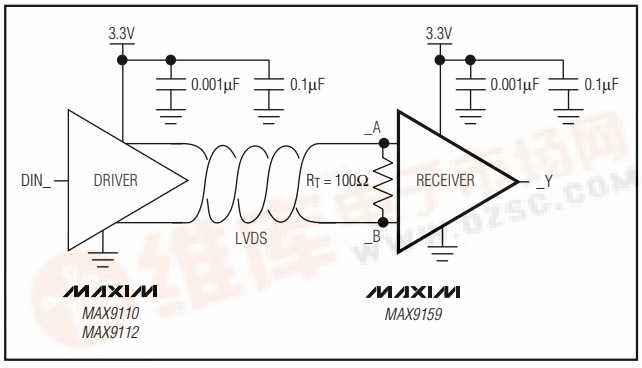
Features

- Pin Compatible with SN65LVDS9637
- Fail-Safe Circuit Sets Output High for Undriven Inputs
- Conforms to ANSI TIA/EIA-644 Standard
- Single 3.3V Supply
- Designed for Data Rates up to 400Mbps
- ±100mV (max) Differential Input Threshold
- 2.2ns (typ) Propagation Delay
- 41mW (typ) Power Dissipation per Receiver at 200MHz
- ±8kV ESD Protection for LVDS Inputs
- Low-Voltage TTL (LVTTL) Logic Output Levels

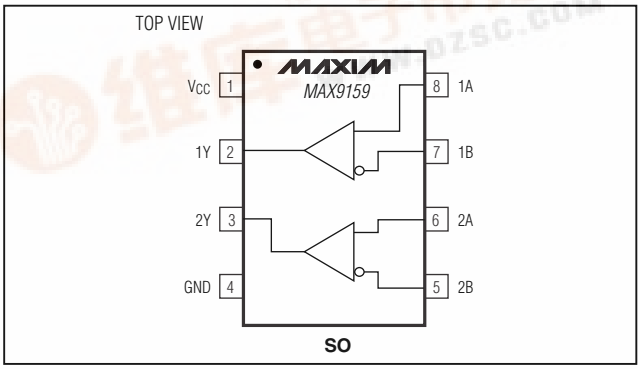
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9159ESA	-40°C to +85°C	8 SO

Typical Operating Circuit



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +4V
1A, 1B, 2A, 2B to GND .....-0.5V to +4V
Y1, Y2 to GND .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation .....(T_A = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection LVDS Inputs (1A, 1B, 2A, 2B)
Human Body Model .....±8kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 0.6V, common-mode input voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUTS (1A, 1B, 2A, 2B)							
Differential Input High Threshold	V_{TH}					100	mV
Differential Input Low Threshold	V_{TL}			-100			mV
Input Current	I_I	_A or _B inputs	V_{IN} = 0	-1.0	-2.3	-20	µA
			V_{IN} = 2.4V	-0.3	-0.67		
Input Current with Differential Input	I_{ID}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V; _A or _B inputs		-20		20	µA
Power-Off Input Current	$I_{I(OFF)}$	V_{CC} = 0, V_{IN} = 3.6V; _A or _B inputs			2.3	20	µA
Power-Off Input Current with Differential Input	$I_{ID(OFF)}$	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0; _A or _B inputs		-15		15	µA
Input Resistor 1	R_{IN1}	V_{CC} = 0 or 3.6V, Figure 1		35			kΩ
Input Resistor 2	R_{IN2}	V_{CC} = 0 or 3.6V, Figure 1		157			kΩ
LVTTL OUTPUTS (Y1, Y2)							
Output High Voltage	V_{OH}	I_{OH} = -8mA		2.4	3.14		V
		I_{OH} = -4mA		2.8	3.2		
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.19	0.4	V
SUPPLY							
Supply Current	I_{CC}	No load			5.7	10	mA

SWITCHING CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 0.6V, common-mode input voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, C_L = 10pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Figures 2 and 3) (Notes 3, 4,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay High to Low	t_{PHL}		1.5	2.2	3	ns
Propagation Delay Low to High	t_{PLH}		1.5	2.13	3	ns
Pulse Skew $\|t_{PHL} - t_{PLH}\|$	$t_{SK(P)}$			0.07	0.4	ns
Channel-to-Channel Output Skew (Note 6)	$t_{SK(O)}$			0.03	0.3	ns
Part-to-Part Skew (Note 7)	$t_{SK(PP)}$				1	ns
Output Signal Rise Time (20% to 80%)	t_R			0.40	0.8	ns
Output Signal Fall Time (80% to 20%)	t_F			0.42	0.8	ns

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground, except V_{TH}, V_{TL}, and V_{ID}.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes scope probe and test jig capacitance.

Note 5: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \le$ 1ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ±0.2ns.

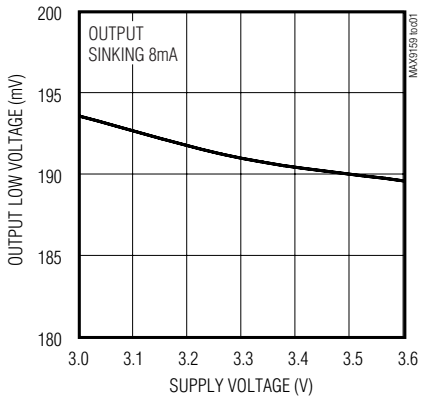
Note 6: $t_{SK(O)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

Note 7: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

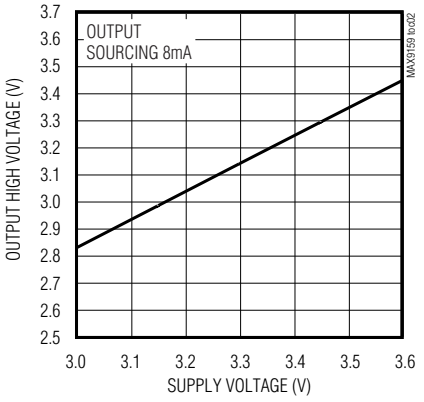
Typical Operating Characteristics

(V_{CC} = 3.3V, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 200MHz, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

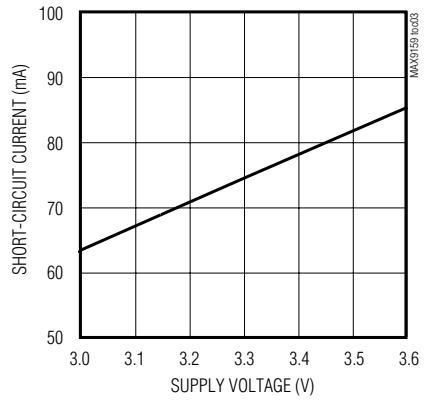
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



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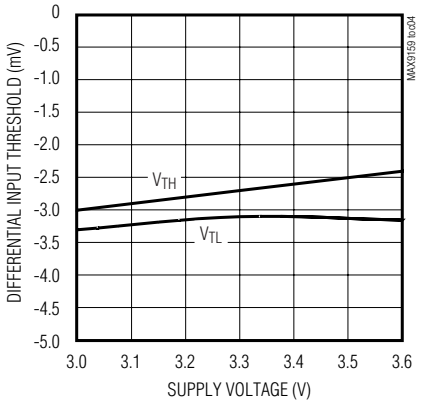
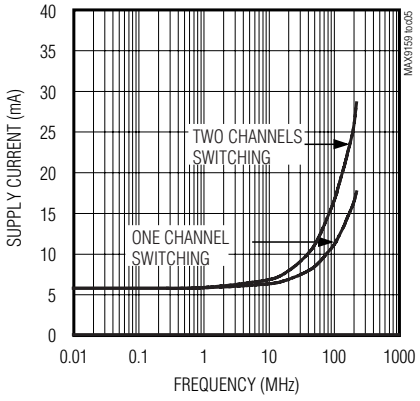
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 200MHz, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

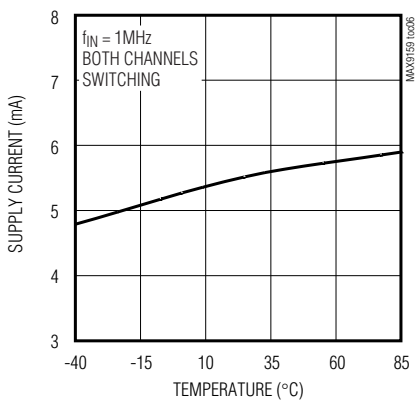
DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



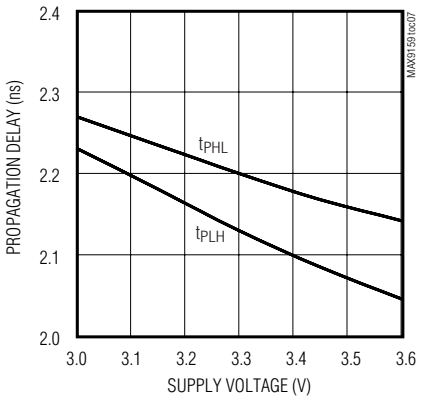
SUPPLY CURRENT vs. FREQUENCY



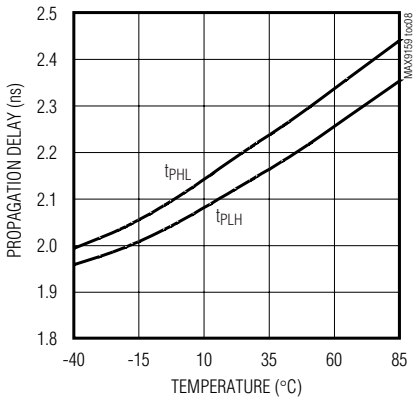
SUPPLY CURRENT vs. TEMPERATURE



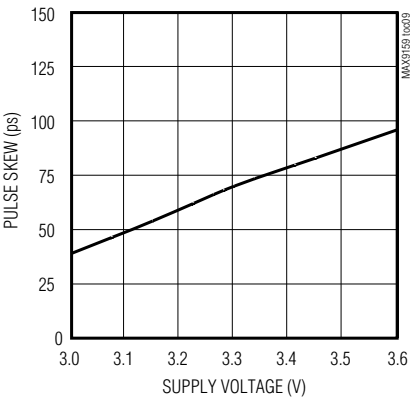
PROPAGATION DELAY vs. SUPPLY VOLTAGE



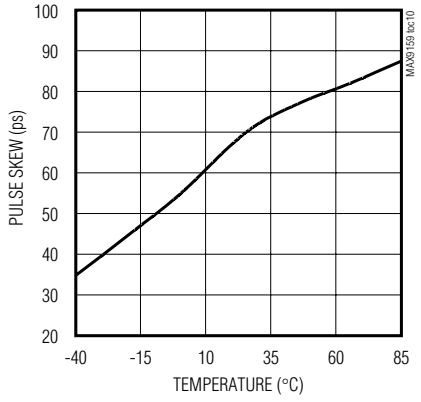
PROPAGATION DELAY vs. TEMPERATURE



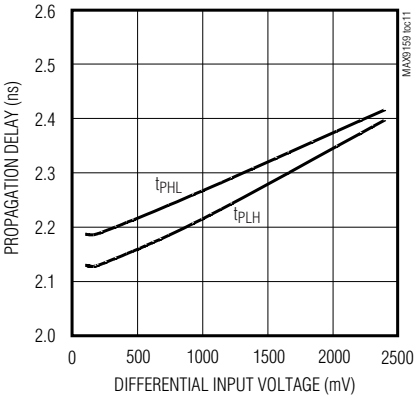
PULSE SKEW vs. SUPPLY VOLTAGE



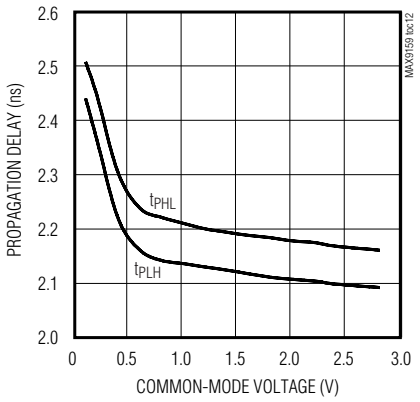
PULSE SKEW vs. TEMPERATURE



PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE



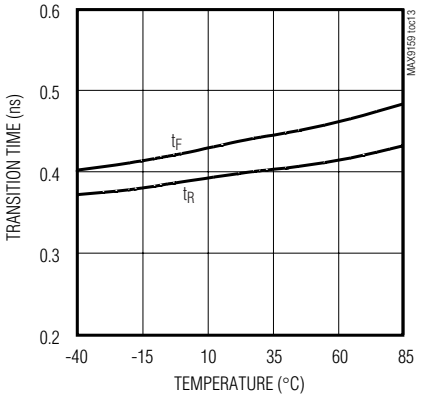
PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



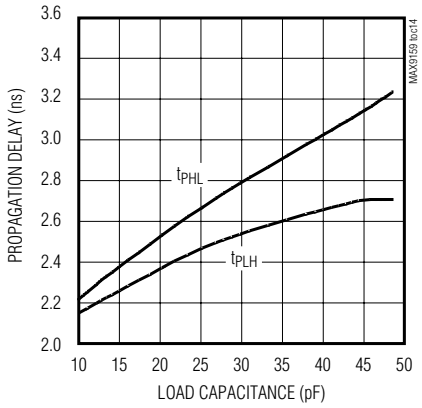
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 200MHz, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

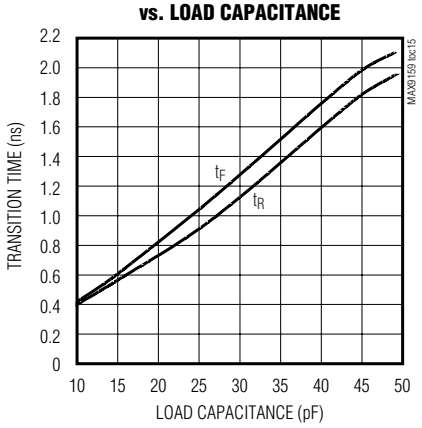
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. LOAD CAPACITANCE



TRANSITION TIME vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power Supply
2	1Y	Channel 1 Output
3	2Y	Channel 2 Output
4	GND	Ground
5	2B	Channel 2 Inverting Differential Input
6	2A	Channel 2 Noninverting Differential Input
7	1B	Channel 1 Inverting Differential Input
8	1A	Channel 1 Noninverting Differential Input

Detailed Description

LVDS is intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9159 is a dual LVDS line receiver ideal for applications requiring high data rates, low power, and low noise. The device accepts an LVDS input and translates it to an LVTTL output. The receiver detects differential signals as low as 100mV and as high as 0.6V within an input voltage range of 0 to 2.4V.

The 250mV to 450mV differential output of an LVDS driver is nominally centered around a 1.25V offset. This offset, coupled with the receiver's 0 to 2.4V input voltage range, allows an approximate ±1V shift in the signal (as seen by the receiver). This allows for a difference in ground references of the driver and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to 2.4V referenced to receiver ground.

Fail-Safe

The fail-safe feature of the MAX9159 sets the output high and reduces supply current when:

- Inputs are open.
- Inputs are undriven and shorted.
- Inputs are undriven and terminated.

A fail-safe circuit is important because under these conditions, noise at the input may switch the receiver and it may appear to the system that data is being received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when an LVDS driver output is in high impedance. A short condition can occur because of a cable failure.

The fail-safe input network (Figure 1) samples the input common-mode voltage and compares it to V_{CC} - 0.3V (nominal). When the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than V_{CC} - 0.3V and the fail-safe circuit is not acti-

Dual LVDS Line Receiver

vated. If the inputs are open or if the inputs are undriven and shorted or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the fail-safe circuit pulls both inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the device.

Differential Traces

Input trace characteristics affect the performance of the MAX9159. Use controlled-impedance PC board traces, typically 100Ω. Match the termination resistor to this characteristic impedance. Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation. Input differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should typically have a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

In point-to-point connections, the MAX9159 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance is typically 100Ω, but may range between 90Ω to 132Ω, depending on the characteristic impedance of the transmission medium.

When using the MAX9159, minimize the distance between the input termination resistor and the MAX9159 inputs. Use 1% surface-mount resistors.

Board Layout

For LVDS applications, use a four-layer PC board with separate layers for power, ground, and input/output. To minimize crosstalk, do not run the output in parallel with the inputs.

Chip Information

TRANSISTOR COUNT: 461

PROCESS: CMOS

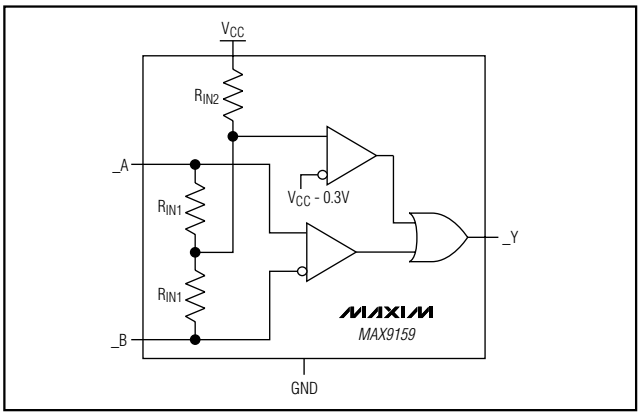


Figure 1. Input Fail-Safe Network

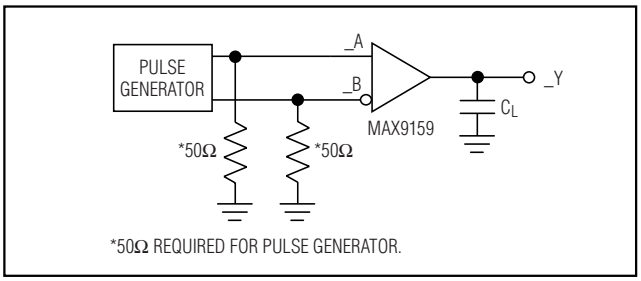


Figure 2. Propagation Delay and Transition-Time Test Circuit

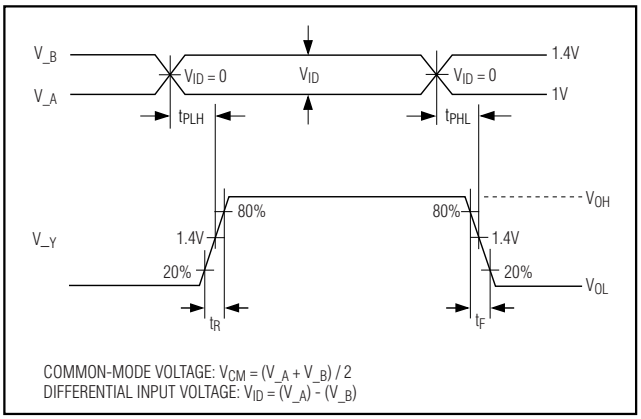
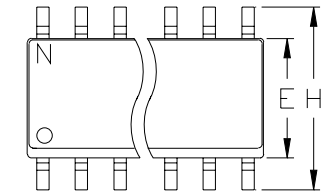


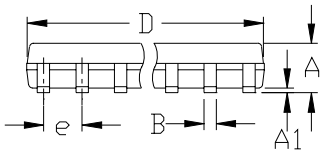
Figure 3. Propagation Delay and Transition-Time Waveforms

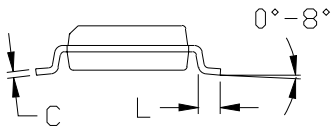
Dual LVDS Line Receiver

Package Information

SOICN.EPS







	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" (TITLE)

1/1

21-0041 A (DOCUMENT CONTROL NUMBER REV)