INITIAL RELEASE
Final Electrical Specifications

LT1469

Dual 90MHz, 22V/µs 16-Bit Accurate Operational Amplifier

February 2000

FEATURES

- **90MHz Gain Bandwidth, f = 100kHz**
- **Maximum Input Offset Voltage: 125µV**
- **Settling Time: 900ns (A_V = –1, 150µV, 10V Step)**
- **22V/µs Slew Rate**
- Low Distortion: –96.5dB for 100kHz, $10V_{P-P}$
- Maximum Input Offset Voltage Drift: 3µV/°C
- Maximum Inverting Input Bias Current: 10nA
- Minimum DC Gain: 300V/mV
- Minimum Output Swing into 2k: ±12.8V
- Unity-Gain Stable
- Input Noise Voltage: 5nV/√Hz
- Input Noise Current: 0.6pA/√Hz
- Total Input Noise Optimized for 1kΩ < R_S < 20kΩ
- Specified at ±5V and ±15V Supplies

APPLICATIONS

- Precision Instrumentation
- High Accuracy Data Acquisition Systems
- 16-Bit DAC Current-to-Voltage Converter
- ADC Buffer
- Low Distortion Active Filters
- Photodiode Amplifiers

DESCRIPTION

The LT®1469 is a dual, precision high speed operational amplifier with 16-bit accuracy and 900ns settling to 150µV for 10V signals. This unique blend of precision and AC performance makes the LT1469 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

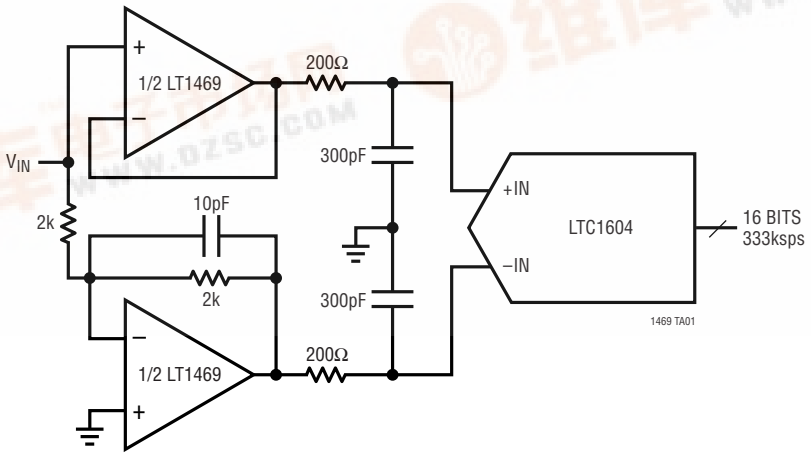
The 90MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance.

The 22V/µs slew rate of the LT1469 improves large signal performance compared to other precision op amps in applications such as active filters and instrumentation amplifiers.

The LT1469 is manufactured on Linear Technology's complementary bipolar process and is available in 8-pin PDIP and SO packages. A single version,the LT1468, is also available.

TYPICAL APPLICATION

16-Bit Accurate Single Ended to Differential ADC Buffer

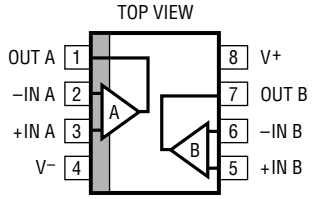


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1469CS8 LT1469IS8 LT1469CN8 LT1469IN8
S8 PART MARKING
1469 1469I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V		30 50	125 200	µV µV
I_{OS}	Input Offset Current		±5V to ±15V		13	±50	nA
I_B–	Inverting Input Bias Current		±5V to ±15V		3	±10	nA
I_B+	Noninverting Input Bias Current		±5V to ±15V		–10	±40	nA
e_n	Input Noise Voltage Density	f = 10kHz	±5V to ±15V		5		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz	±5V to ±15V		0.6		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±12.5V Differential	±15V ±15V	100 50	240 150		MΩ kΩ
C_{IN}	Input Capacitance		±15V		4		pF
V_{CM}	Input Voltage Range (Positive)		±15V ±5V	12.5 2.5	13.5 3.5		V V
	Input Voltage Range (Negative)		±15V ±5V		–14.3 –4.3	–12.5 –2.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V V_{CM} = ±2.5V	±15V ±5V	96 96	110 112		dB dB
	Minimum Supply Voltage	Guaranteed by PSRR			±2.5	±4.5	V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		100	112		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12.5V, R_L = 10k V_{OUT} = ±12.5V, R_L = 2k V_{OUT} = ±2.5V, R_L = 10k V_{OUT} = ±2.5V, R_L = 2k	±15V ±15V ±5V ±5V	300 300 200 200	9000 5000 6000 3000		V/mV V/mV V/mV V/mV
V_{OUT}	Maximum Output Swing	R_L = 10k, 1mV Overdrive R_L = 2k, 1mV Overdrive R_L = 10k, 1mV Overdrive R_L = 2k, 1mV Overdrive	±15V ±15V ±5V ±5V	±13 ±12.8 ±3 ±2.8	±13.6 ±13.5 ±3.6 ±3.5		V V V V
I_{OUT}	Maximum Output Current	V_{OUT} = ±12.5V, 1mV Overdrive V_{OUT} = ±2.5V, 1mV Overdrive	±15V ±5V	±15 ±15	±22 ±22		mA mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 0.2V Overdrive (Note 3)	±15V	±25	±40		mA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
SR	Slew Rate	A_V = –10, R_L = 2k (Note 6)	±15V ±5V	15 11	22 17		V/µs V/µs
FPBW	Full-Power Bandwidth	10V Peak, (Note 7) 3V Peak, (Note 7)	±15V ±5V		350 900		kHz kHz
GBW	Gain Bandwidth Product	f = 100kHz, R_L = 2k	±15V ±5V	60 55	90 88		MHz MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V	±15V ±5V		11 12		ns ns
OS	Overshoot	A_V = 1, 0.1V	±15V ±5V		30 35		% %
t_{PD}	Propagation Delay	A_V = 1, 50% V_{IN} to 50% V_{OUT}, 0.1V	±15V ±5V		9 10		ns ns
t_S	Settling Time	10V Step, 0.01%, A_V = –1 10V Step, 150µV, A_V = –1 5V Step, 0.01%, A_V = –1	±15V ±15V ±5V		760 900 770		ns ns ns
THD	Total Harmonic Distortion	A_V = 1, 10V_{P-P}, 100kHz	±15V		–96.5		dB
R_{OUT}	Output Resistance	A_V = 1, f = 100kHz	±15V		0.02		Ω
	Channel Separation	V_{OUT} = ±12.5V, R_L = 2k V_{OUT} = ±2.5V, R_L = 2k	±15V ±5V	100 100	120 120		dB dB
I_S	Supply Current	Per Amplifier	±15V ±5V		4.1 3.8	5.2 5	mA mA
ΔV_{OS}	Input Offset Voltage Match		±15V ±5V			225 350	µV µV
ΔI_B–	Inverting Input Bias Current Match		±5V to ±15V			±18	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V			±78	nA
ΔCMRR	Common Mode Rejection Match	V_{CM} = ±12.5V (Note 9) V_{CM} = ±2.5V (Note 9)	±15V ±5V	93 93			dB dB
ΔPSRR	Power Supply Rejection Match	V_S = ±4.5V to ±15V (Note 9)		97			dB

The ● denotes the specifications which apply over the temperature range 0°C ≤ T_A ≤ 70°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V	● ●			350 350	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 8)	±5V to ±15V	●		1	3	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			±80	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 8)	±5V to ±15V	●		60		pA/°C
I_B–	Inverting Input Bias Current		±5V to ±15V	●			±20	nA
ΔI_B–/ΔT	Inverting Input Bias Current Drift	(Note 8)	±5V to ±15V	●		40		pA/°C
I_B+	Noninverting Input Bias Current		±5V to ±15V	●			±60	nA
V_{CM}	Input Voltage Range (Positive)		±15V ±5V	● ●	12.5 2.5			V V
	Input Voltage Range (Negative)		±15V ±5V	● ●			–12.5 –2.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V V_{CM} = ±2.5V	±15V ±5V	● ●	94 94			dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0°C \le T_A \le 70°C$, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
	Minimum Supply Voltage	Guaranteed by PSRR		●			±4.5	V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		●	95			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12.5V, R_L = 10k	±15V	●	100			V/mV
		V_{OUT} = ±12.5V, R_L = 2k	±15V	●	100			V/mV
		V_{OUT} = ±2.5V, R_L = 10k	±5V	●	100			V/mV
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	100			V/mV
V_{OUT}	Maximum Output Swing	R_L = 10k, 1mV Overdrive	±15V	●	±12.9			V
		R_L = 2k, 1mV Overdrive	±15V	●	±12.7			V
		R_L = 10k, 1mV Overdrive	±5V	●	±2.9			V
		R_L = 2k, 1mV Overdrive	±5V	●	±2.7			V
I_{OUT}	Maximum Output Current	V_{OUT} = ±12.5V, 1mV Overdrive	±15V	●	±12.5			mA
		V_{OUT} = ±2.5V, 1mV Overdrive	±5V	●	±12.5			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 0.2V Overdrive (Note 3)	±15V	●	±17			mA
SR	Slew Rate	A_V = –10, R_L = 2k (Note 6)	±15V	●	13			V/µs
			±5V	●	9			V/µs
GBW	Gain Bandwidth Product	f = 100kHz, R_L = 2k	±15V	●	55			MHz
			±5V	●	50			MHz
	Channel Separation	V_{OUT} = ±12.5V, R_L = 2k	±15V	●	98			dB
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	98			dB
I_S	Supply Current	Per Amplifier	±15V	●			6.5	mA
			±5V	●			6.3	mA
ΔV_{OS}	Input Offset Voltage Match		±15V	●			600	µV
			±5V	●			600	µV
ΔI_B-	Inverting Input Bias Current Match		±5V to ±15V	●			±38	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V	●			±118	nA
ΔCMRR	Common Mode Rejection Match	V_{CM} = ±12.5V (Note 9)	±15V	●	91			dB
		V_{CM} = ±2.5V (Note 9)	±5V	●	91			dB
ΔPSRR	Power Supply Rejection Match	V_S = ±4.5V to ±15V (Note 9)		●	92			dB

The ● denotes the specifications which apply over the temperature range $-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			500	µV
			±5V	●			500	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 8)	±5V to ±15V	●		1	4	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			±120	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 8)	±5V to ±15V	●		120		pA/°C
I_B-	Inverting Input Bias Current		±5V to ±15V	●			±40	nA
$\Delta I_B-/\Delta T$	Inverting Input Bias Current Drift	(Note 8)	±5V to ±15V	●		80		pA/°C
I_B+	Noninverting Input Bias Current		±5V to ±15V	●			±80	nA
V_{CM}	Input Voltage Range (Positive)		±15V	●	12.5			V
			±5V	●	2.5			V
	Input Voltage Range (Negative)		±15V	●			–12.5	V
			±5V	●			–2.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V	±15V	●	92			dB
		V_{CM} = ±2.5V	±5V	●	92			dB
	Minimum Supply Voltage	Guaranteed by PSRR		●			±4.5	V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		●	93			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12,5V, R_L = 10k	±15V	●	75			V/mV
		V_{OUT} = ±12.5V, R_L = 2k	±15V	●	75			V/mV
		V_{OUT} = ±2.5V, R_L = 10k	±5V	●	75			V/mV
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	75			V/mV
V_{OUT}	Maximum Output Swing	R_L = 10k, 1mV Overdrive	±15V	●	±12.8			V
		R_L = 2k, 1mV Overdrive	±15V	●	±12.6			V
		R_L = 10k, 1mV Overdrive	±5V	●	±2.8			V
		R_L = 2k, 1mV Overdrive	±5V	●	±2.6			V
I_{OUT}	Maximum Output Current	V_{OUT} = ±12.5V, 1mV Overdrive	±15V	●	±7			mA
		V_{OUT} = ±2.5V, 1mV Overdrive	±5V	●	±7			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 0.2V Overdrive (Note 3)	±15V	●	±12			mA
SR	Slew Rate	A_V = –10, R_L = 2k (Note 6)	±15V	●	9			V/µs
			±5V	●	6			V/µs
GBW	Gain Bandwidth Product	f = 100kHz, R_L = 2k	±15V	●	45			MHz
			±5V	●	40			MHz
	Channel Separation	V_{OUT} = ±12.5V, R_L = 2k	±15V	●	96			dB
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	96			dB
I_S	Supply Current	Per Amplifier	±15V	●			7	mA
			±5V	●			6.8	mA
ΔV_{OS}	Input Offset Voltage Match		±15V	●			800	µV
			±5V	●			800	µV
ΔI_B-	Inverting Input Bias Current Match		±5V to ±15V	●			±78	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V	●			±158	nA
ΔCMRR	Common Mode Rejection Match	V_{CM} = ±12.5V (Note 9)	±15V	●	89			dB
		V_{CM} = ±2.5V (Note 9)	±5V	●	89			dB
ΔPSRR	Power Supply Rejection Match	V_S = ±4.5V to ±15V (Note 9)		●	90			dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1469C and LT1469I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT1469C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1469I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Slew rate is measured between ±8V on the output with ±12V swing for ±15V supplies and ±2V on the output with ±3V swing for ±5V supplies.

Note 7: Full-power bandwidth is calculated from the slew rate. $FPBW = SR/2\pi V_P$.

Note 8: This parameter is not 100% tested.

Note 9: ΔCMRR and ΔPSRR are defined as follows: 1) CMRR and PSRR are measured in µV/V on each amplifier; 2) the difference between the two sides is calculated in µV/V; 3) the result is converted to dB.

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1469 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01μF to 0.1μF) in parallel with low ESR bypass capacitors (1μF to 10μF tantalum). For best DC performance, use "star" grounding techniques, equalize input trace lengths and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_B– specification).

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: for inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below).

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short and the two input leads should be as close together as possible and maintained at the same temperature.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of value $C_F > R_G \bullet C_{IN}/R_F$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be a DAC I-to-V converter as shown on the back page of the data sheet where the DAC can have many tens of picofarads of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor.

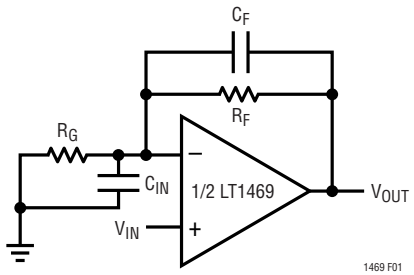


Figure 1. Nulling Input Capacitance

APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1469 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If large differential input voltages are anticipated, limit the input current to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA.

The LT1469 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1469 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

The total input noise of the LT1469 is optimized for a source resistance between 1k and 20k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 1k, voltage noise of the amplifier dominates. When the source resistance is above 20k, the input noise current is the dominant contributor.

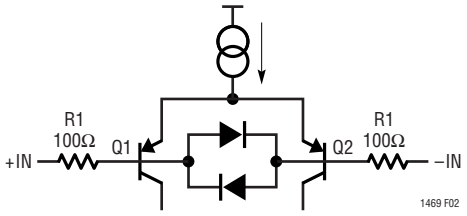


Figure 2. Input Stage Protection

APPLICATIONS INFORMATION

Capacitive Loading

The LT1469 drives capacitive loads of up to 100pF in unity-gain and 300pF in a gain of –1. When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Figure 3.

Settling Time

The LT1469 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling, even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling measurements—Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements and AN74 extends the state-of-the-art while concentrating on settling time with a 16-bit current output DAC input.

The settling of the DAC I-to-V converter on the back page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 20pF across the 6k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 1.33µs. The actual settling time is 1.7µs at the output of the LT1469. The LT1469 is the fastest Linear Technology amplifier in this application.

The RC output noise filter adds a slight settling time delay of 100ns but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

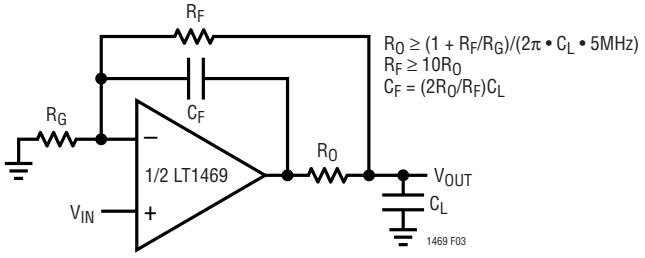
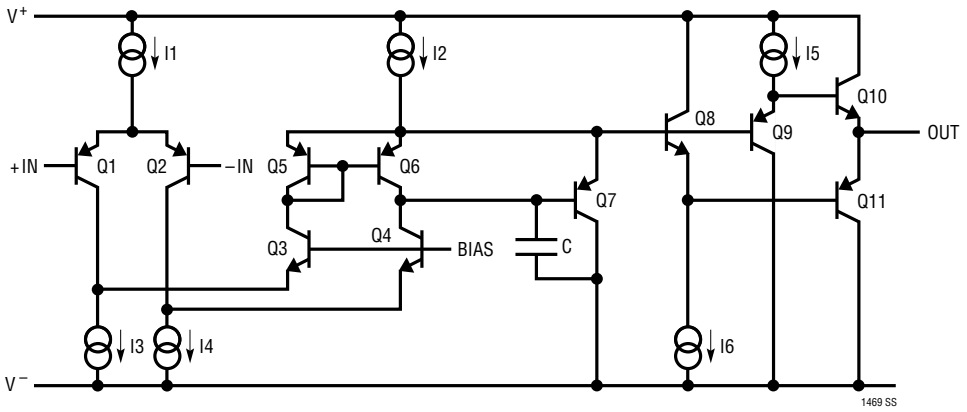


Figure 3. Driving Capacitive Loads

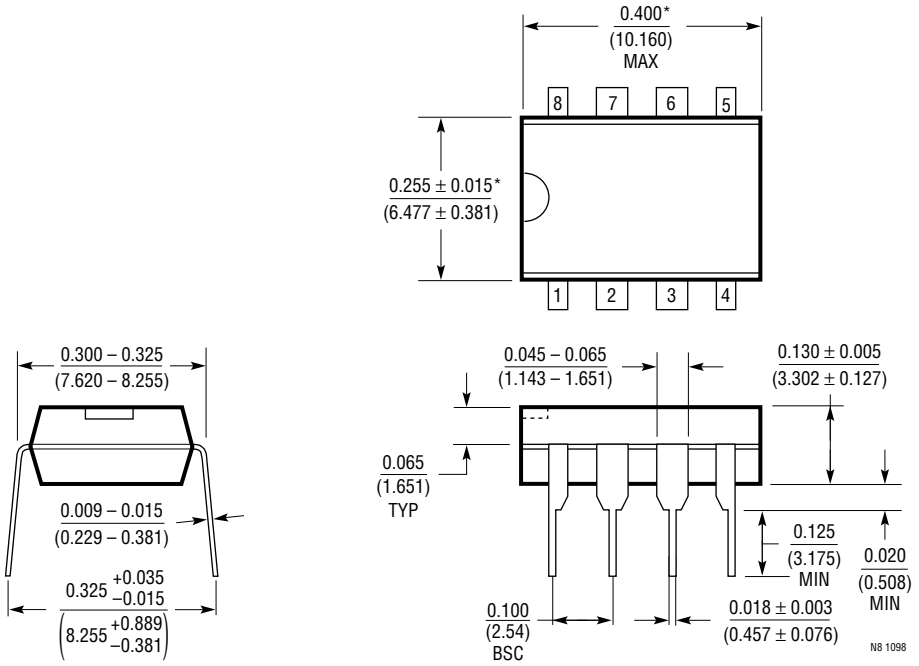
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

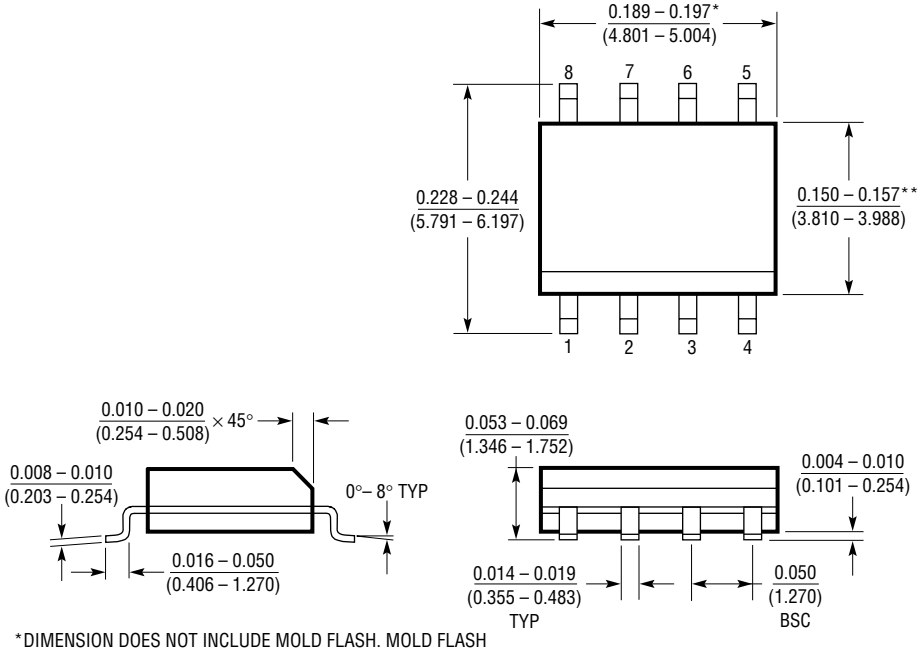


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



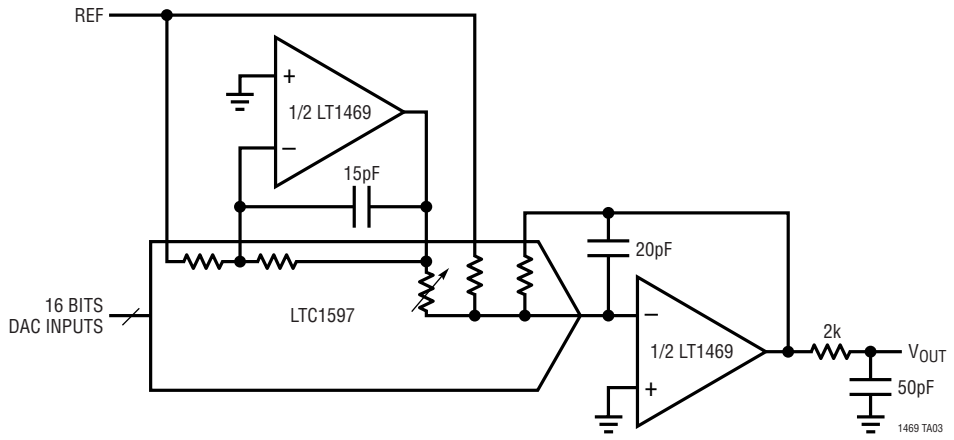
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

TYPICAL APPLICATION

16-Bit DAC I-to-V Converter and Reference Inverter for Bipolar Output Swing (V_{OUT} = –10V to 10V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Precision Instrumentation Amplifier	Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity
LT1468	Single 90MHz, 22V/µs, 16-Bit Accurate Op Amp	75µV Max V_{OS}, Single Version of LT1469
LTC1595/LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1597	16-Bit Parallel Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors
LT1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = –100dB
LTC1605	Single 5V, 16-Bit, 100ksps Sampling ADC	Low Power, ±10V Inputs, Parallel/Byte Interface