MIC2589/MIC2595

Single-Channel, Negative High-Voltage Hot Swap Power Controllers/Sequencers

General Description

The MIC2589 and MIC2595 are single-channel, negative-voltage hot swap controllers designed to address the need for safe insertion and removal of circuit boards into "live" system backplanes, while using few external components. The MIC2589/89R and the MIC2595/95R are each available in 14-pin SOIC packaging and work in conjunction with an external N-Channel MOSFET for which the gate drive is controlled to provide inrush current limiting and output voltage slew-rate control. Overcurrent fault protection is also provided for which the overcurrent threshold and the overcurrent duration are programmable. Very fast fault response is provided to ensure that system power supplies maintain regulation even during output short circuits. This family offers two responses to a circuit breaker fault condition: the MIC2589 and MIC2595 latch the circuit breaker's output off if the overcurrent threshold interval is exceeded while the MIC2589R and MIC2595R automatically attempt to restart at a fixed duty cycle after a current limit fault. A primary Power-Good signal and two secondary (delayed and staggered) Power-Good signals are provided to indicate that the output voltage of the inrush current limiter is within its valid operating range. These signals can be used to perform an all-at-once or a sequenced enabling of one or more DC-DC power modules.

All support documentation can be found on Micrel's web site at www.micrel.com.

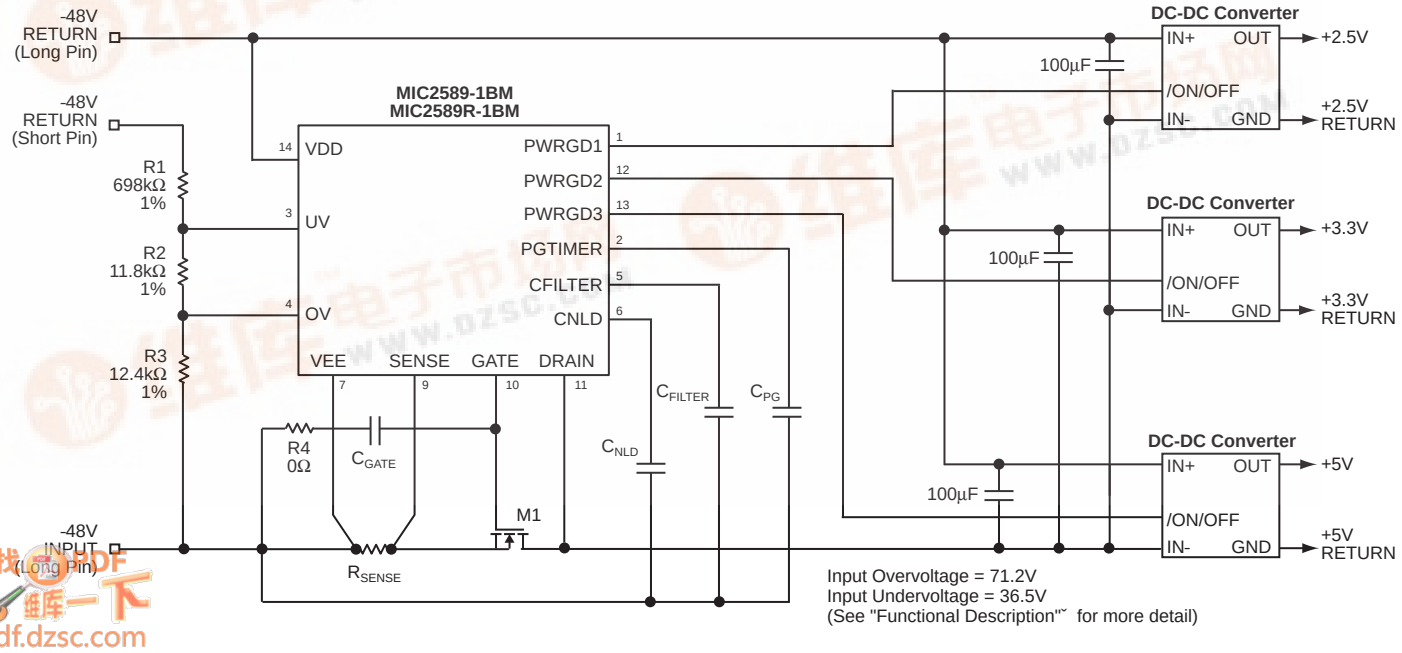
Features

- Provides safe insertion and removal from live –48V (nominal) backplanes
- Operates from –19V to –80V
- Fast responding circuit breaker (<1µs) to short circuit conditions
- User-programmable overcurrent detector response time
- Electronic circuit breaker function:
  - Output latch OFF (MIC2589/95) or
  - Output auto-retry (MIC2589R/95R)
- Active current regulation precisely controls inrush currents
- Regulated maximum output currents into faults
- Programmable undervoltage and overvoltage lockouts (MIC2589/89R)
- Programmable UVLO hysteresis (MIC2595/95R)
- Staggered 'Power-Good' outputs provide load sequencing
- Fault reporting:
  - Active-HIGH (MIC25XX-1) and Active-LOW (MIC25XX-2) Power-Good signal output

Applications

- Central office switching
- –48V power distribution
- Distributed power systems

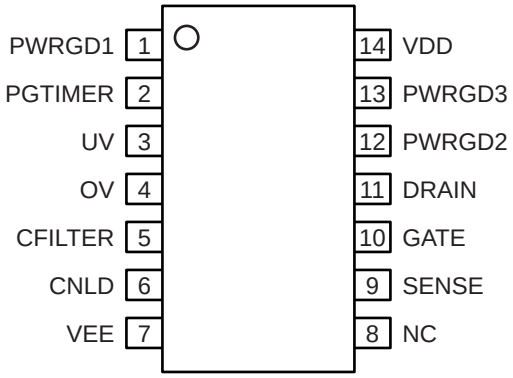
Typical Application



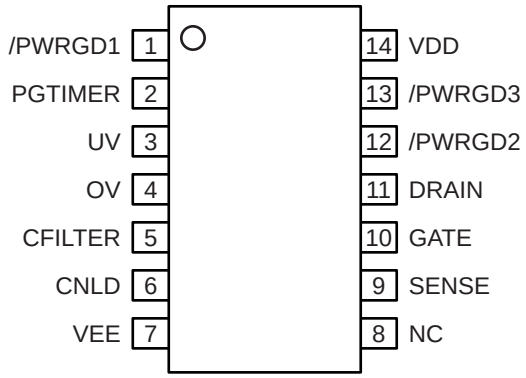
Ordering Information

Part Number	PWRGD Polarity	Input Voltage Monitor Pins	Circuit Breaker Function	Package
MIC2589-1BM	Active-High	Programmable UVLO & OVLO	Latched Off	14-pin SOIC
MIC2589-2BM	Active-Low	Programmable UVLO & OVLO	Latched Off	14-pin SOIC
MIC2589R-1BM	Active-High	Programmable UVLO & OVLO	Auto-Retry	14-pin SOIC
MIC2589R-2BM	Active-Low	Programmable UVLO & OVLO	Auto-Retry	14-pin SOIC
MIC2595-1BM	Active-High	Programmable UVLO Hysteresis	Latched Off	14-pin SOIC
MIC2595-2BM	Active-Low	Programmable UVLO Hysteresis	Latched Off	14-pin SOIC
MIC2595R-1BM	Active-High	Programmable UVLO Hysteresis	Auto-Retry	14 pin SOIC
MIC2595R-2BM	Active-Low	Programmable UVLO Hysteresis	Auto-Retry	14-pin SOIC

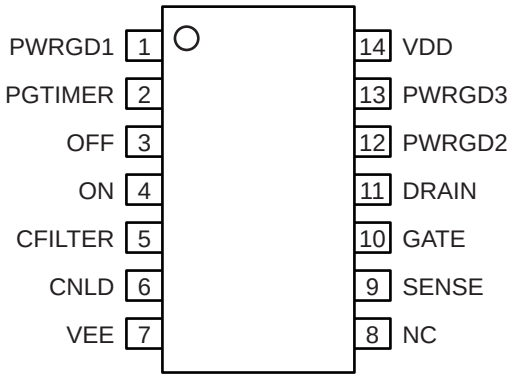
Pin Configuration



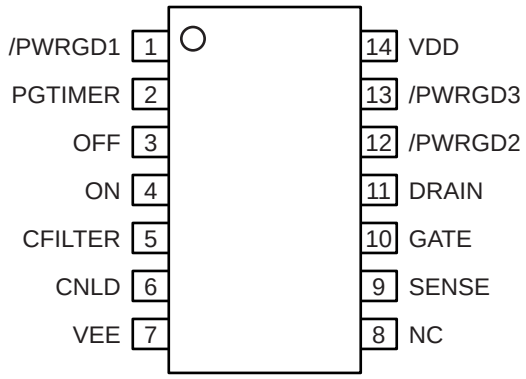
14-Pin SOIC (M)
MIC2589-1BM
MIC2589R-1BM



14-Pin SOIC (M)
MIC2589-2BM
MIC2589R-2BM



14-Pin SOIC (M)
MIC2595-1BM
MIC2595R-1BM



14-Pin SOIC (M)
MIC2595-2BM
MIC2595R-2BM

Pin Description

Pin Number	Pin Name	Pin Function
1	PWRGD1 (MIC25XX-1) Active-High /PWRGD1 (MIC25XX-2) Active-Low	Power-Good Output 1: Asserted when the voltage on the DRAIN pin (V_{DRAIN}) is within V_{PGTH} of VEE, indicating that the output voltage is within proper specifications. For the MIC2589-1 and MIC2985-1, PWRGD1 will be high impedance when V_{DRAIN} is less than V_{PGTH}, and will pull-down to V_{DRAIN} when V_{DRAIN} is greater than V_{PGTH}. For the MIC2589-2 and MIC2595-2, /PWRGD1 will pull-down to V_{DRAIN} when V_{DRAIN} is less than V_{PGTH}, and will be high-impedance when V_{DRAIN} is greater than V_{PGTH}.
2	PGTIMER	A capacitor connected from this pin to VEE sets the time interval between assertions of PWRGD2 (or /PWRGD2) and PWRGD3 (or /PWRGD3) relative to PWRGD1 (or /PWRGD1). See the "Functional Description" for further detail.
3	UV Threshold	MIC2589 and MIC2589R: Undervoltage Threshold Input. When the voltage at the UV pin is less than the V_{UVL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The UV pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the OV and UV pins form a window comparator which define the limits of V_{EE} within which the load may safely be powered.
3	OFF (Turn-Off Threshold)	MIC2595 and MIC2595R: Turn-Off Threshold. When the voltage at the OFF pin is less than the V_{OFFL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The OFF pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the ON and OFF pins provide programmable hysteresis for the MIC2595 to be enabled.
4	OV Threshold	MIC2589 and MIC2589R: Overvoltage Threshold Input. When the voltage at the OV pin is greater than the V_{OVH} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down.
4	ON (Turn-On Threshold)	MIC2595 and MIC2595R: Turn-On Threshold. At initial system power-up or after the part has been shut off by the OFF pin, the voltage on the ON pin must be above the V_{ONH} threshold in order for the MIC2595 to be enabled.
5	CFILTER	Current Limit Response Timer: A capacitor connected between this pin and VEE provides filtering against nuisance tripping of the circuit breaker by setting a time delay, t_{FLT}, for which an overcurrent event must last prior to signaling a fault condition and latching the output off. The minimum time for t_{FLT} will be the time it takes for the output (capacitance) to charge to V_{EE} during start-up. This pin is held to VEE with a 3µA current pull-down when no current limit condition exists. See the "Functional Description" for further details.
6	CNLD	No-Load Detect Timer: A capacitor between this pin and VEE sets the interval, t_{NLD}, for which the current through the external MOSFET can drop below 10% of full-scale current limit before the circuit breaker is tripped. Tying this pin to V_{EE} will disable this function. This pin is held to VEE by an internal NMOS when there is no undercurrent condition.
7	VEE	Negative Supply Voltage Input.
8	NC	No Internal Connection.
9	SENSE	Circuit Breaker Sense Input: A resistor between this pin and VEE sets the current limit trip point for the circuit. When the current limit threshold of IR = 50mV is exceeded for t_{FLT}, the circuit breaker is tripped and the GATE pin is immediately pulled low. Toggling UV or OV will reset the circuit breaker. To disable the circuit breaker, externally tie SENSE and VEE can be connected together.
10	GATE	Gate Drive Output: Connects to the Gate of an N-Channel MOSFET.
11	DRAIN	Drain Sense Input: Connects to the Drain of an N-Channel MOSFET.

Pin Number	Pin Name	Pin Function
12	PWRGD2 (MIC2589-1) (MIC2595-1)	Power-Good Output 2: Asserted when the following is true: (PWRGD1 = Asserted) AND (Time after Assertion of PWRGD1 = Time PWRGD2, as programmed by the capacitor on PGTIMER). Once PWRGD1 is asserted, the PGTIMER pin begins to change and PWRGD2 will assert when PGTIMER crosses the PWRGD2 threshold ($V_{THRESH(PG2)}$ = 0.63V, typical). Also see PWRGD1 and PGTIMER pin descriptions.
12	/PWRGD2 (MIC2589-2) (MIC2595-2)	/Power-Good Output 2: Asserted when the following is true: (/PWRGD1 = Asserted) AND (Time after Assertion of /PWRGD1 = Time /PWRGD2, as programmed by the capacitor on PGTIMER). Once /PWRGD1 is asserted, the PGTIMER pin begins to change and /PWRGD2 will assert when PGTIMER crosses the /PWRGD2 threshold ($V_{THRESH(PG2)}$ = 0.63V, typical). Also see /PWRGD1 and PGTIMER pin descriptions.
13	PWRGD3 (MIC2589-1) (MIC2595-1)	Power-Good Output 3: Asserted when the following is true: (PWRGD1 = Asserted) AND (Time after Assertion of PWRGD1 = Time PWRGD3, as programmed by the capacitor on PGTIMER). Once PWRGD1 is asserted, the PGTIMER pin begins to change and PWRGD3 will assert when PGTIMER crosses the PWRGD3 threshold ($V_{THRESH(PG3)}$ = 1.15V, typical). Also see PWRGD1 and PGTIMER pin descriptions.
13	/PWRGD3 (MIC2589-2) (MIC2595-2)	/Power-Good Output 3: Open Collector. Asserted when the following is true: (/PWRGD1 = Asserted) AND (Time after Assertion of /PWRGD1 = Time /PWRGD3, as programmed by the capacitor on PGTIMER). Once /PWRGD1 is asserted, the PGTIMER pin begins to change and /PWRGD3 will assert when PGTIMER crosses the /PWRGD3 threshold ($V_{THRESH(PG3)}$ = 1.15V, typical). Also see /PWRGD1 and PGTIMER pin descriptions.
14	VDD	Positive Supply Input.

Absolute Maximum Ratings(1)

(All voltages are referred to V_{EE})

Supply Voltage ($V_{DD} – V_{EE}$) ..... –0.3V to 100V
DRAIN, PWRGD pins ..... –0.3V to 100V
GATE pin ..... –0.3V to 12.5V
SENSE, OV, UV, ON, OFF pins ..... –0.3V to 6V
ESD Ratings(3) 2kV
Soldering
Vapor Phase ..... (60 sec.) +220°C +5 ±0°C
Infrared ..... (15 sec.) +235°C +5 ±0°C

Operating Ratings(2)

Supply Voltage (V_{DD}-V_{EE}) ..... +19V to +80V
Ambient Temperature Range (T_A) ..... –40°C to 85°C
Junction Temperature (T_J) ..... 125°C
Package Thermal Resistance
SOIC (θ_{JA}) ..... 120°C/W

DC Electrical Characteristics(4)

V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C, unless otherwise noted. **Bold** indicates specifications apply over the full operating temperature range of –40°C to 85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD} – V_{EE}$	Supply Voltage		**19**		**80**	
I_{DD}	Supply Current			4	**6**	mA
V_{TRIP}	Circuit Breaker Trip Voltage	$V_{TRIP} = V_{SENSE} – V_{EE}$	**40**	50	**60**	mV
I_{NLDTH}	No-Load Detect Threshold	% of full-scale current limit I_{OUT} decreasing I_{OUT} increasing		 20 22		 % %
I_{NLDHYS}	No-Load Detect Threshold Hysteresis	% of full-scale current limit		2		%
V_{CNLD}	No-Load Detect Timer High Threshold Voltage		**1.17**	1.24	**1.33**	V
I_{CNLD}	No-Load Detect Timer Capacitor Charge Current	**Note 5**	10	25	40	µA
V_{GATE}	GATE Drive Voltage, ($V_{GATE} – V_{EE}$)	$15V \le (V_{DD} – V_{EE}) \le 80V$	**9**	10	**11**	V
I_{GATEON}	GATE Pin Pull-Up Current	$V_{GATE} = V_{EE}$ to 8V $19V \le (V_{DD} – V_{EE}) \le 80V$	**30**	45	**60**	µA
I_{SENSE}	SENSE Pin Current	V_{SENSE} = 50mV		0.2		µA
$I_{GATEOFF}$	GATE Pin Sink Current	$(V_{SENSE} – V_{EE})$ = 100mV V_{GATE} = 2V	100	240		mA
$I_{CFILTER}$	CFILTER Charge Current	$(V_{SENSE} – V_{EE}) > V_{TRIP}$ $V_{CFILTER}$ = 0.75V V_{GATE} = 3V	**65**	95	**135**	µA
	CFILTER Pull-Down Current	$(V_{SENSE} – V_{EE}) < V_{TRIP}$ $V_{CFILTER}$ = 0.75V V_{GATE} = 3V	**2**	4	**6**	µA
$V_{CFILTER(TRIP)}$	High Threshold Voltage Overcurrent Detect Timer	$(V_{SENSE} – V_{EE}) > V_{TRIP}$	**1.17**	1.25	**1.33**	V
$V_{CFILTER(RETRY)}$	Voltage on CFILTER to Trigger Auto-Retry (MIC2589R and MIC2595R only)		**0.17**	0.22	**0.25**	V
$I_{PGTIMER}$	PGTIMER Charge Current	Voltage on PGTIMER = 0.75 V	**30**	45	**80**	µA

Notes:

1. Exceeding the “Absolute Maximum Ratings” may damage the devices.
2. The devices are not guaranteed to function outside the specified Operating Conditions.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF. Machine model: 200pF, no series resistance.
4. Specification for packaged product only.
5. Not 100% tested. Parameters are guaranteed by design.

DC Electrical Characteristics[6]

V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C, unless otherwise noted. **Bold** indicates specifications apply over the full operating temperature range of –40°C to 85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{THRESH(PG2)}$	PGTIMER Threshold Voltage for PWRGD2 and /PWRGD2		**0.5**	0.63	**0.8**	V
$V_{THRESH(PG3)}$	PGTIMER Threshold Voltage for PWRGD3 and /PWRGD3		**1.00**	1.15	**1.30**	V
$R_{PGTIMER}$	PGTIMER Discharge Resistance	Voltage on PGTIMER = 0.5 V	**250**	500	**750**	Ω
V_{OVH}	OV Pin High Threshold Voltage (MIC2589 and 2589R parts only)	Low-to-High transition	**1.198**	1.223	**1.247**	V
V_{OVL}	OV Pin Low threshold Voltage (MIC2589 and 2589R only)	High-to-Low transition	**1.165**	1.203	**1.232**	V
V_{OVHYS}	OV Pin Hysteresis (MIC2589 and 2589R only)			20		mV
V_{UVL}	UV Pin Low threshold Voltage (MIC2589 and 2589R only)	High-to-Low transition	**1.198**	1.223	**1.247**	V
V_{UVH}	UV Pin High Threshold Voltage (MIC2589 and 2589R only)	Low-to-High transition	**1.213**	1.243	**1.272**	V
V_{UVHYS}	UV Pin Hysteresis (MIC2589 and 2589R only)			20		mV
V_{ONH}	ON Pin High Threshold Voltage (MIC2595 and 2595R only)	Low-to-High transition	**1.198**	1.223	**1.247**	V
V_{OFFL}	OFF Pin Low Threshold Voltage (MIC2595 and 2595R only)	High-to-Low transition	**1.198**	1.223	**1.247**	V
I_{CNTRL}	Input Current (OV, UV, ON, OFF Pins)	V_{UV} = 1.25V			**0.5**	µA
V_{PGTH}	Power-Good Threshold	High-to-Low Transition ($V_{DRAIN} – V_{EE}$)	**1.1**	1.26	**1.40**	V
V_{OLPG}	PWRGD Output Voltage (relative to voltage at the DRAIN pin)	$V_{OLPG} – V_{DRAIN}$ $0mA \le I_{PG(LOW)} \le 1mA$				
	MIC25XX-1	$(V_{DRAIN} – V_{EE}) > V_{PGTH}$	**–0.25**		**0.8**	V
	MIC25XX-2	$(V_{DRAIN} – V_{EE}) < V_{PGTH}$	**–0.25**		**0.8**	V
$I_{LKG(PG)}$	PWRGD Output Leakage Current	$V_{PWRGD} = V_{DD}$ = 80 V	**0**		**1**	µA

Note:

6. Specification for packaged product only.

AC Electrical Characteristics[7]

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{OCSENSE}$	Overcurrent Sense to GATE Low Trip Time, Figure 2	$V_{SENSE} - V_{EE}$ = 100mV[8]			3.5	µs
t_{OVPHL}	OV High to GATE Low, Figure 3 (MIC2589 and 2589R only)	OV = 1.5V[8]		1		µs
t_{OVPLH}	OV Low to GATE High, Figure 3 (MIC2589 and 2589R only)	OV = 1.0V[8]		1		µs
t_{UVPHL}	UV Low to GATE Low, Figure 4 (MIC2589 and 2589R only)	UV = 1.0V[8]		1		µs
t_{UVPLH}	UV High to GATE High, Figure 4 (MIC2589 and 2589R only)	UV = 1.5V[8]		1		µs
t_{OFFPHL}	OFF Low to GATE Low, Figure 5 (MIC2595 and 2595R only)	OFF = 1.0V[8]		1		µs
t_{ONPLH}	ON High to GATE High, Figure 5 (MIC2595 and 2595R only)	ON = 1.5V[8]		1		µs
t_{PGLH1}	DRAIN Low to PWRGD1 Output High (-1)	C_{LOAD} on PWRGDx = 50pF, R_{PULLUP} = 100kΩ[8]		3		µs
t_{PGHL1}	DRAIN High to all PWRGDx Outputs Low (-1)	C_{LOAD} on PWRGDx = 50pF, R_{PULLUP} = 100kΩ[8]		5		µs
t_{PGHL2}	DRAIN Low to /PWRGD1 Output Low (-2)	C_{LOAD} on /PWRGDx = 50pF, R_{PULLUP} = 100kΩ[8]		5		µs
t_{PGLH2}	DRAIN High to all /PWRGDx Outputs High (-2)	C_{LOAD} on /PWRGDx = 50pF, R_{PULLUP} = 100kΩ[8]		3		µs

Notes:

7. Specification for packaged product only.
8. Not 100% production tested. Parameters are guaranteed by design.

Test Circuit

[Section under construction]

Timing Diagrams

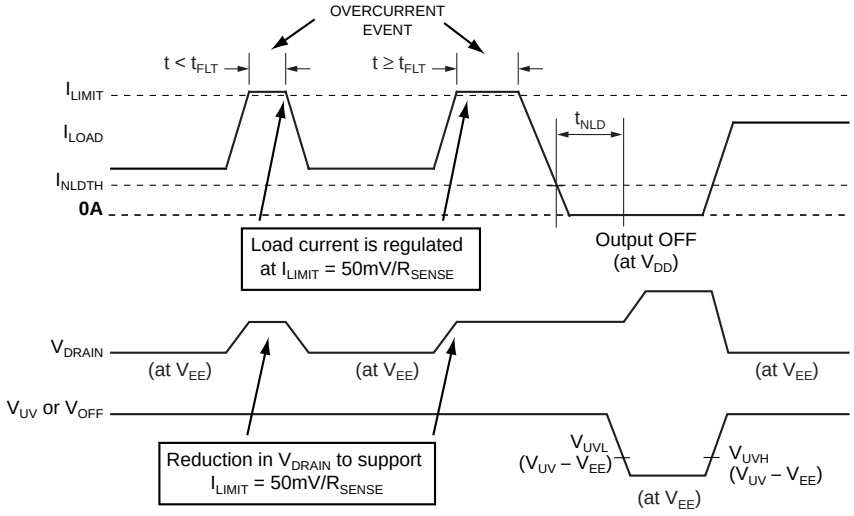


Figure 1. Overcurrent and Undercurrent (No Load) Response

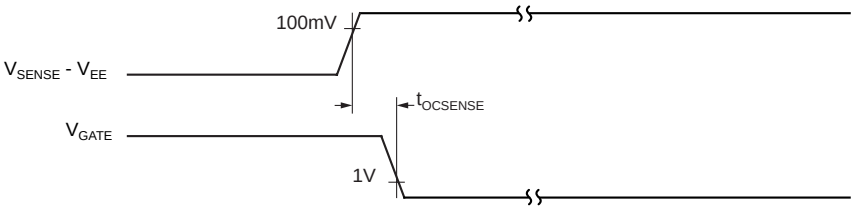


Figure 2. SENSE to GATE LOW Timing Response

Figure 3. MIC2589/89R Overvoltage Response

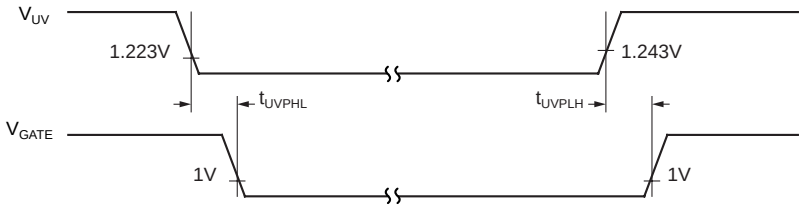


Figure 4. MIC2589/89R Undervoltage Response

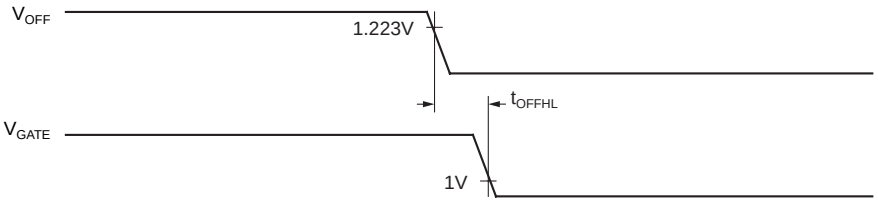


Figure 5a. MIC2595/95R OFF to GATE Drive Response

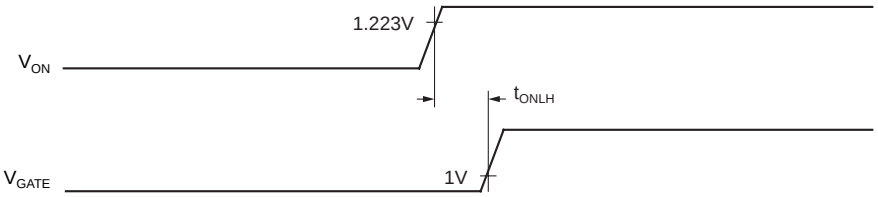


Figure 5b. MIC2595/95R ON to GATE Drive Response

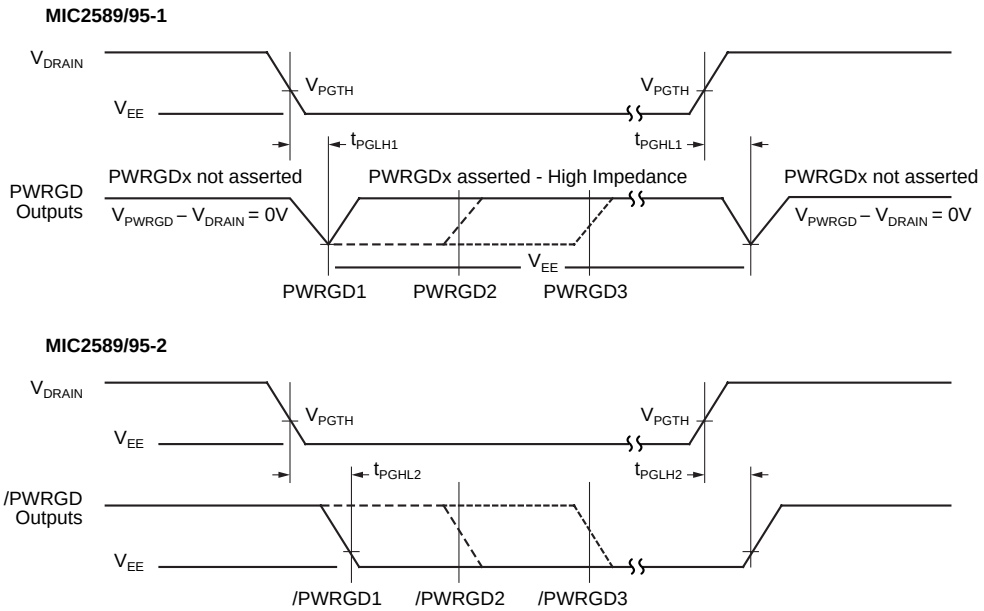
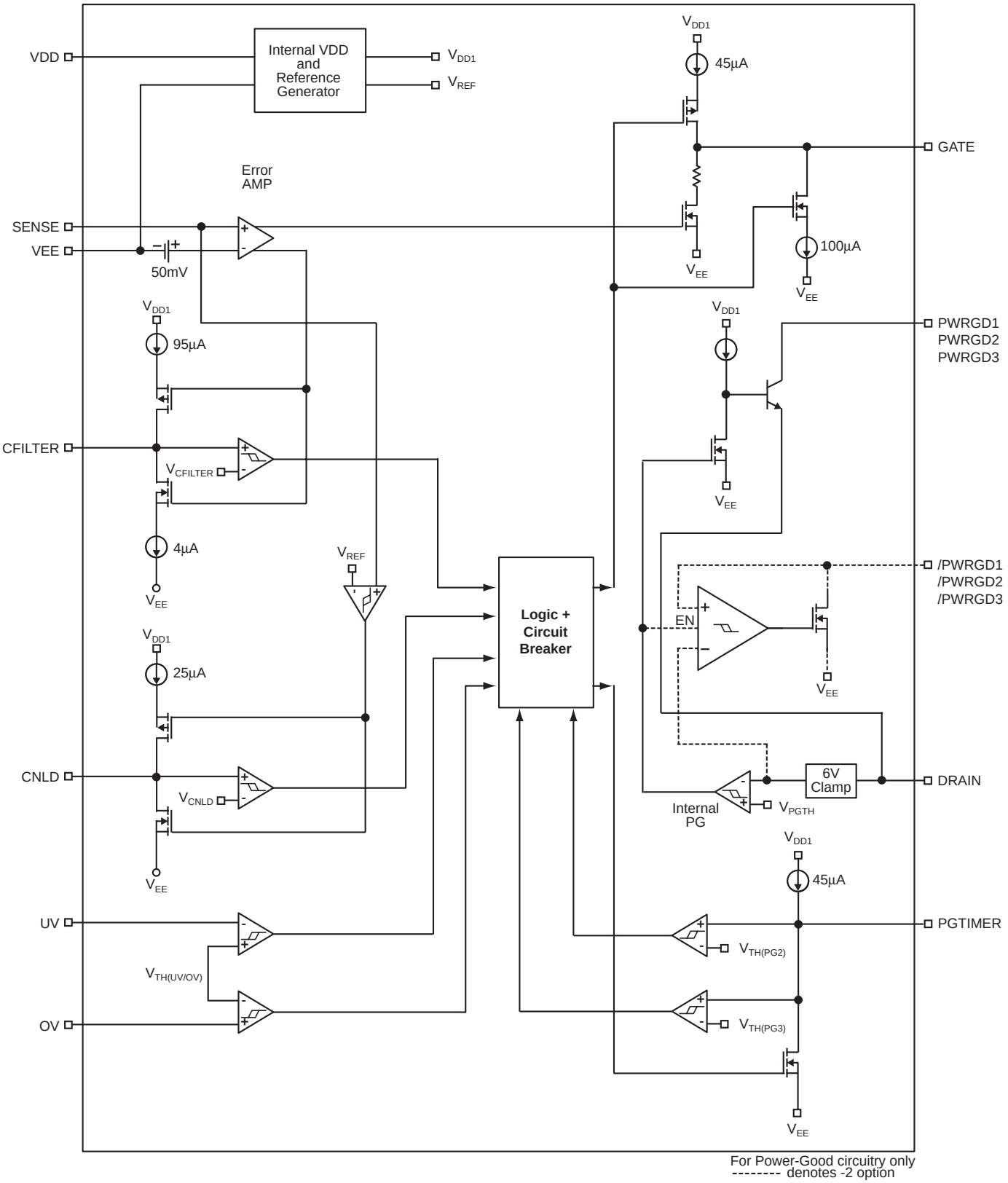


Figure 6. DRAIN to Power-Good Response

Functional Diagram



MIC2589 Block Diagram

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot swapped"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. These current spikes can cause the system's supply voltages to temporarily go out of regulation causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot swap event may cause permanent damage to connectors or on-board components.

The MIC2589 and the MIC2595 are designed to address these issues by limiting the maximum current, which is allowed to flow during hot swap events. This is achieved by implementing a constant-current loop at turn-on. In addition to inrush current control, the MIC2589 and the MIC2595 incorporate input voltage supervisory functions and user-programmable overcurrent protection, thereby providing robust protection for both the system and the circuit board.

Start-Up Cycle

When the input voltage is to the IC is between the overvoltage and undervoltage thresholds (MIC2589 and MIC2589R) or is greater than V_{ON} (MIC2595 and MIC2595R), a start cycle is initiated. When the IC is enabled, the GATE pin voltage rises from 0V with respect to V_{EE} to approximately 10V above V_{EE}. This 10V gate drive is sufficient to fully enhance commonly available power MOSFETs for the lowest possible DC losses. Capacitor C_{GATE} compensates circuitry internal to the IC, while R4 minimizes the potential for high frequency parasitic oscillations from occurring in M1. The drain current of the MOSFET is regulated to ensure that it never exceeds the programmed threshold, as described in the "Circuit Breaker Function" section.

Capacitor C_{FILTER} sets the value of overcurrent detector delay, t_{FLT}, which is the time for which an overcurrent event must last to signal a fault condition and to cause an output latch-off. These devices will be driving a capacitive load in most applications, so a properly chosen value of C_{FILTER} prevents false-, or nuisance-, tripping at turn-on as well as providing immunity to noise spikes after the start-up cycle is complete. The procedure for selecting a value for C_{FILTER} is given in the "Circuit Breaker Function" section.

Resistor R4, in series with the power MOSFET's gate, may be required in some layouts to minimize the potential for parasitic oscillations occurring in M1. Note though, that resistance in this device of the circuit has a slight destabilizing effect upon the MIC2589/95's current regulation loop. If possible, use high-frequency PCB layout techniques and use a dummy resistor, such that R4 = 0Ω. If during prototyping an R4 is required, common values for R4 range between 4.7Ω to 20Ω for various power MOSFETs.

The Power-Good Output Signals

For the MIC2589/95-1 and MIC2589R/95R-1, power-good output signal PWRGD1 will be high impedance when V_{DRAIN} drops below V_{PGTH}, and will pull-down to V_{DRAIN} when V_{DRAIN} is above V_{PGTH}. For the MIC2589/95-2 and the MIC2589R/95R-2, power-good output signal /PWRGD1 will pull down to the potential of the V_{DRAIN} pin when V_{DRAIN} drops below V_{PGTH} and will be high impedance when V_{DRAIN} is above V_{PGTH}. Hence, the -1 parts have an active-high $PWRGD_X$ signal and the -2 parts have an active-low $/PWRGD_X$ output. $PWRGD_X$ (or $/PWRGD_X$) may be used as an enable signal for one or more following DC/DC converter modules or for other system uses as desired. When used as an enable signal, the time necessary for the PWRGD (or /PWRGD) signal to pull-up (when in high impedance state) will depend upon the load (RC) that is present on this output.

Power-good output signals PWRGD2 (/PWRGD2) and PWRGD3 (/PWRGD3) follow the assertion of PWRGD1 (/PWRGD1) with a sequencing delay set by an external capacitor (C_{PG}) from the controller's PGTIMER pin (Pin 2) to V_{EE}. An expression for the sequencing delay between PWRGD2 and PWRGD1 is given by:

$$t_{PGDLY2-1} = \frac{V_{THRESH(PG2)} \times C_{PG}}{I_{PGTIMER}}$$

where $V_{THRESH(PG2)}$ (= 0.63V, typically) is the PWRGD2 threshold voltage for PGTIMER and $I_{PGTIMER}$ (= 45µA, typically) is the internal PGTIMER charge current. Similarly, an expression for the sequencing delay between PWRGD3 and PWRGD2 is given by:

$$t_{PGDLY3-2} = \frac{\left(V_{THRESH(PG3)} - V_{THRESH(PG2)}\right) \times C_{PG}}{I_{PGTIMER}}$$

where $V_{THRESH(PG3)}$ (= 1.15V, typically) is the PWRGD3 threshold voltage for PGTIMER. Therefore, power-good output signal PWRGD2 (/PWRGD2) will be delayed after the assertion of PWRGD1 (/PWRGD1) by:

$$t_{PGDLY2\text{-}1}\ (\text{ms}) \cong 14 \times C_{PG}(\mu\text{F})\ \text{ms}$$

Power-good output signal PWRGD3 (/PWRGD3) follows the assertion of PWRGD2 by a delay:

$$t_{PGDLY3\text{-}2}\ (\text{ms}) \cong 11.5 \times C_{PG}(\mu\text{F})\ \text{ms}$$

For example, for a 10µF value for C_{PG}, power-good output signal PWRGD2 will be asserted 140ms after PWRGD1. Power-good signal PWRGD3 will then be asserted 140ms after PWRGD2 and 255ms after the assertion of PWRGD1. The relationships between V_{DRAIN}, V_{PGTH}, PWRGD1, PWRGD2, and PWRGD3 are shown in Figure 6.

Circuit Breaker Function

The MIC2589/89R and the MIC2595/95R employ an electronic circuit breaker that protects the external power MOSFET and other system components against large-scale faults, such as short circuits. The current-limit threshold is set via an external resistor, R_{SENSE}, connected between the V_{EE} and SENSE. For the MIC2589/89R and MIC2595/95R, a timer is set via capacitor C_{FILTER} that determines the length of the time delay (t_{FLT}) for which the device remains in current limit before the circuit breaker is tripped. This programmable delay prevents tripping of the circuit breaker because of high inrush current charging bulk and distributed capacitive loads. Whenever the voltage across R_{SENSE} exceeds 50mV, two things happen:

1. A constant-current regulation loop is engaged which is designed to hold the voltage across R_{SENSE} equal to 50mV. This protects both the load and the MIC2589/95 circuits from excessively high currents. This current-regulation loop will engage in less than 1µs from the time at which the overvoltage condition on R_{SENSE} occurs.
2. Capacitor C_{FILTER} is charged up to an internal $V_{CFILTER(TRIP)}$ threshold (= 1.25V) by an internal 95µA current source. If the voltage across C_{FILTER} crosses this threshold, the circuit breaker trips and the GATE pin is immediately pulled low by an internal current pull-down. This operation turns off the MOSFET quickly and disconnects the input from the load. The value of C_{FILTER} should be selected to allow the circuit's minimum regulated value of I_{OUT} to equal I_{TRIP} for somewhat longer than the time it takes to charge the total load capacitance.

An initial value for C_{FILTER} is found by calculating the time it will take for the MIC2589/95 to completely charge up the output capacitive load. Assuming the load is enabled by the $PWRGD_X$ (or /$PWRGD_X$) signal(s) of the IC, the turn-on delay time is derived from the following expression, $I = C \times (dv/dt)$:

$$t_{TURN\text{-}ON} = \frac{C_{LOAD} \times (V_{DD} - V_{EE})}{I_{LIMIT}}$$

Using parametric values specific to the MIC2589/95, an expression relating a design nominal value for C_{FILTER} to the circuit's turn-on delay time is:

$$C_{FILTER}(nom) = \frac{(t_{TURN\text{-}ON} \times I_{CFILTER}(typ))}{V_{CFILTER}(typ)} = \frac{t_{TURN\text{-}ON} \times 95\mu A}{1.25V} = t_{TURN\text{-}ON} \times 76 \times 10^{-6} \frac{\mu F}{sec}$$

Substituting the variables above with the specification limits of the MIC2589/95, an expression for the worst-case value for C_{FILTER} is given by:

$$C_{FILTER}(max) = t_{TURN\text{-}ON} \times \left(\frac{135\mu A}{1.17V}\right) = t_{TURN\text{-}ON} \times \left(115.4 \times 10^{-6} \frac{\mu F}{sec}\right)$$

For example, in a system with a C_{LOAD} = 150µF, a maximum ($V_{DD} - V_{EE}$) = 72V, and a maximum load current on a nominal –48V buss of 1.65A, the nominal circuit design equations steps are:

1. Choose $I_{LIMIT} = I_{HOT\_SWAP}(nom)$ = 2A (1.65A + 20%);
2. Select an $R_{SENSE} = \frac{38.8mV}{2A} = 19.4m\Omega$ (closest 1% standard value is 19.6mΩ);
3. Using $I_{CHARGE} = I_{LIMIT}$ = 2A, the application circuit turn-on time is calculated:

$$t_{TURN\text{-}ON} = \frac{(150\mu F \times 72V)}{2A} = 5.4ms \text{ (use 6 ms)}$$

Allowing for capacitor tolerances and a nominal 6ms turn-on time, an initial worst-case value for C_{FILTER} is:

$C_{FILTER(WORST\text{-}CASE)}$ = 6ms x (115.4 × 10^{-6}µF/sec) = 692nF

The closest standard ±5% tolerance capacitor value is 698nF and would be a good initial starting value for prototyping.

Whenever the hot swap controller is not in current limit, C_{FILTER} is discharged to V_{EE} by an internal 4µA current source.

For the MIC2589R/95R devices, the circuit breaker automatically resets after (20) t_{FLT} time constants ($20 \times t_{FLT}$). If the fault condition still exists, capacitor C_{FILTER} will again be charge up to $V_{FILTER(TRIP)}$ where the circuit breaker is tripped. Capacitor C_{FILTER} will then be discharged by an internal 4µA current source until the voltage across C_{FILTER} goes below $V_{FILTER(RETRY)}$, at which time another start cycle is initiated. This will continue until the fault condition is removed or input power is removed/cycled. The duty cycle of the auto-restart function is therefore fixed at 5% and the period of the auto-restart cycle is given by:

$$t_{AUTO\text{-}RESTART} = 20 \times \frac{(C_{FILTER}) \times (1.25V - 0.22V)}{95\mu A} = C_{FILTER} \times \left(216.8 \frac{ms}{\mu F}\right)$$

The auto-restart period for the example above where the worst-case C_{FILTER} was determined to be 698nF is:

$t_{AUTO\text{-}RESTART}$ = 151ms

Current Sensing

As mentioned before, the MIC2589/89R and the MIC2595/95R use an external, low-value resistor in series with the source of the external MOSFET to measure the current flowing into the load. The V_{EE} connection (Pin 7) to the IC is one input to the device's internal current sensing circuits and the SENSE connection (Pin 9) is the other input.

The sense resistor is nominally valued at:

$$R_{SENSE}(nom) = \frac{V_{TRIP}(typ)}{I_{HOT\_SWAP}(nom)}$$

where V_{TRIP}(typ) is the nominal circuit breaker threshold voltage (= 50mV) and I_{HOT_SWAP}(nom) is the nominal hot swap load current level to trip the internal circuit breaker in the application.

To accommodate worst-case tolerances in the sense resistor (for a ±1% initial tolerance, allow ±3% tolerance for variations over time and temperature) and circuit breaker threshold voltages, a slightly more detailed calculation must be used to determine the minimum and maximum hot swap load currents.

As the MIC2589/95's minimum current-limit threshold voltage is 40mV, the minimum hot swap load current is determined where the sense resistor is 3% high:

$$I_{HOT\_SWAP}(min) = \frac{40mV}{1.03 \times R_{SENSE}(nom)} = \frac{38.8mV}{R_{SENSE}(nom)}$$

Keep in mind that the minimum hot swap load current should be greater than the application circuit's upper steady-state load current boundary. Once the lower value of R_{SENSE} has been calculated, it is good practice to check the maximum hot swap load current (I_{HOT_SWAP}(max)) which the circuit may let pass in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum is found using a V_{TRIP}(max) of 60mV and a sense resistor 3% low in value:

$$I_{HOT\_SWAP}(max) = \frac{60mV}{0.97 \times R_{SENSE}(nom)} = \frac{61.9mV}{R_{SENSE}(nom)}$$

In this case, the application circuit must be sturdy enough to operate over an ~1.6-to-1 range in hot swap load currents. For example, if an MIC2595 circuit must pass a minimum hot swap load current of 4A without nuisance trips, R_{SENSE} should be set to $\frac{38.8mV}{4A} = 9.7m\Omega$, and the nearest 1% standard value is 9.76mΩ. At the other tolerance extremes, I_{HOT_SWAP}(max) for the circuit in question is then simply:

$$I_{HOT\_SWAP}(max) = \frac{61.9mV}{9.76m\Omega} = 6.3A$$

With a knowledge of the application circuit's maximum hot swap load current, the power dissipation rating of the sense resistor can be determined using $P = I^2 \times R$. Here, The I is I_{HOT_SWAP}(max) = 6.3A and the R is R_{SENSE}(min) = (0.97)(R_{SENSE}(nom)) = 9.47mΩ. Thus, the sense resistor's maximum power dissipation is:

$$P_{MAX} = (6.3A)^2 \times (9.47m\Omega) = 0.376W$$

A 0.5Ω sense resistor is a good choice in this application.

No-Load Detection

For those applications in which a minimum load current will always be present, the no-load detect capability of the MIC2589/89R/95/95R family offers system designer the ability to perform a shutdown operation on such fault conditions, such as an unscheduled or unexpected removal of PC boards from the system or on-board fuse failure.

As long as the minimum current drawn by the load is at least 20% of the maximum output current (defined by $\frac{V_{TRIP}}{R_{SENSE}}$), the output of the hot swap controllers will remain enabled. If the output current falls below 12% of the maximum output current, the controller's no-load detection loop is enabled. In this loop, an internal current source, I_{CNLD}, will charge an external capacitor C_{NLD}. An expression for the controller's no-load time-out delay is given by:

$$t_{NLD} = V_{CNLD} \times \left(\frac{C_{NLD}}{I_{CNLD}} \right)$$

where V_{CNLD} = 1.24V (typ); I_{CNLD} = 25µA (typ); and C_{NLD} is an external capacitor connected from Pin 6 to V_{EE}. Once the voltage on C_{NLD} reaches its no-load threshold voltage, V_{CNLD}, the loop times out and the controller will shut down until it is reset manually (MIC2589/95) or until it performs an auto-retry operation (MIC2589R/95R).

Undervoltage/Overvoltage Detection (MIC2589 and MIC2589R)

The MIC2589 and the MIC2589R have "UV" and "OV" input pins that can be used to detect input supply rail undervoltage and overvoltage conditions. Undervoltage lockout prevents energizing the load until the supply input is stable and within tolerance. In a similar fashion, overvoltage turnoff prevents damage to sensitive circuit components should the input voltage exceed normal operational limits. Each of these pins is internally connected to analog comparators with 20mV of hysteresis. When the UV pin falls below its V_{UVL} threshold or the OV pin is above its V_{OVH} threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until the UV pin is above its V_{UVH} threshold or the OV pin is below its V_{OVL} threshold. The circuit's UV and OV threshold voltage levels are programmed using the resistor divider R1, R2, and R3 as shown in the "Typical Application" where the equations to set the trip points are shown below. For the following example, the circuit's UV threshold is set to V_{UV} = 37V and the OV threshold is set at V_{OV} = 72V, values commonly used in Central Office power distribution applications.

$$V_{UV} = V_{UVL}(typ) \times \frac{(R1 + R2 + R3)}{(R2 + R3)}$$

$$V_{OV} = V_{OVH}(typ) \times \frac{(R1 + R2 + R3)}{R3}$$

Given V_{UV}, V_{OV}, and any one resistor value, the remaining two resistor values can be determined. A suggested value for R3 is that which will provide approximately 100µA of current through the voltage divider chain at $V_{DD} = V_{UV}$. This yields the following as a starting point:

$$R3 = \frac{V_{OVH}(typ)}{100\mu A} = \frac{1.223V}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ. Solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{OV}}{V_{UV}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{72V}{37V}\right) - 1\right] = 11.73k\Omega$$

The closest standard 1% values for R2 = 11.8kΩ. Lastly, the value for R1 is calculated:

$$R1 = R3 \times \left[\frac{(V_{OV} - 1.223V)}{1.223V}\right] - R2$$

$$R1 = 12.4k\Omega \times \left[\frac{(72V - 1.223V)}{1.223V}\right] - R2$$

$$R1 = 705.81k\Omega$$

The closest standard 1% value for R1 = 698kΩ.

Using standard 1% resistor values, the circuit's nominal UV and OV thresholds are:

V_{UV} = 36.5V
V_{OV} = 71.2V

Programmable UVLO Hysteresis (MIC2595 and MIC2595R)

The MIC2595 and the MIC2595R devices have user-programmable hysteresis by means of the ON and OFF pins (Pins 4 and 3, respectively). This allows setting the MIC2595/95R to turn on at a voltage V1, and not turn off until a second voltage V2, where V2 < V1. This can significantly simplify dealing with source impedances in the supply buss while at the same time increasing the amount of available operating time from a loosely regulated power rail (for example, a battery supply). The MIC2595/95R holds the output off until the voltage at the ON pin is above its V_{ONH} threshold value given in the "Electrical Characteristics" table. Once the output has been enabled by the ON pin, it will remain on until the voltage at the OFF pin falls below its respective V_{OFFL} threshold value, or the part turns off due to an external fault condition. Should either event occur, the GATE pin is immediately pulled low and will remain low until the ON pin voltage once again above its V_{ONH} threshold. The circuit's turn-on and turn-off voltage levels are set using the resistor divider R1, R2, and R3 as shown in the "Typical Application" where the equations to set the trip points are shown below. For the following example, the circuit's ON threshold is set to V_{ON} = 40V and the circuit's OFF threshold is set to V_{OFF} = 35V.

$$V_{ON} = V_{ONH}(typ) \times \frac{(R1 + R2 + R3)}{R3}$$

$$V_{OFF} = V_{OFFL}(typ) \times \frac{(R1 + R2 + R3)}{R2 + R3}$$

Given V_{OFF}, V_{ON}, and any one resistor value, the remaining two resistor values can be readily determined. A suggested value for R3 is that which will provide approximately 100µA of current through the voltage divider chain at $V_{DD} = V_{OFF}$. This yields the following as a starting point:

$$R3 = \frac{V_{OFFL}(typ)}{100\mu A} = \frac{1.223V}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ. Solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{ON}}{V_{OFF}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{40V}{35V}\right) - 1\right] = 1.77k\Omega$$

The closest standard 1% value for R2 = 1.78 kΩ. Lastly, the value for R1 is calculated:

$$R1 = R3 \times \frac{(V_{ON} - 1.223V)}{1.223V} - R2$$

$$R1 = 12.4k\Omega \times \frac{(40V - 1.223V)}{1.223V} - R2$$

R1 = 391.38kΩ

The closest standard 1% value for R1 = 392kΩ.

Using standard 1% resistor values, the circuit's nominal ON and OFF thresholds are:

V_{ON} = 40.1V
V_{OFF} = 35V

Applications Information

4-Wire Kelvin Sensing

Because of the low value typically required for the sense resistor, special care must be used to measure accurately the voltage drop across it. Specifically, the measurement technique across R_{SENSE} must employ 4-wire Kelvin sensing. This is simply a means of ensuring that any voltage drops in the power traces connected to the resistors are not picked up by the signal conductors measuring the voltages across the sense resistors.

Figure 7 illustrates how to implement 4-wire Kelvin sensing. As the figure shows, all the high current in the circuit (from V_{EE} through R_{SENSE} and then to the source of the output MOSFET) flows directly through the power PCB traces and through R_{SENSE}. The voltage drop across R_{SENSE} is sampled in such a way that the high currents through the power traces will not introduce any parasitic voltage drops in the sense leads. It is recommended to connect the hot swap controller's sense leads directly to the sense resistor's metalized contact pads.

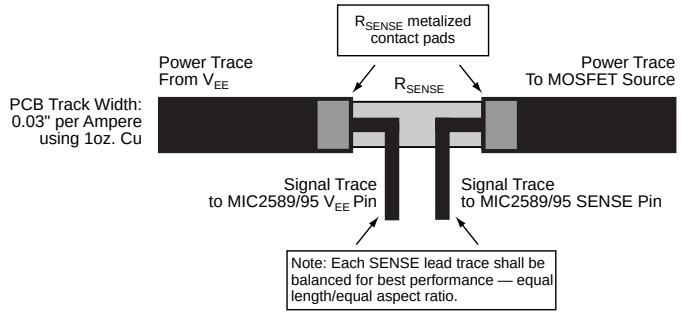


Figure 7. 4-Wire Kelvin Sense Connections for R_{SENSE}

Protection Against Voltage Transients

In many telecom applications, it is very common for circuit boards to encounter large-scale supply-voltage transients in backplane environments. Because backplanes present a complex impedance environment, these transients can be as high as 2.5 times steady-state levels, or 120V in worst-case situations. In addition, a sudden load dump anywhere on the circuit card can generate a very high voltage spike at the drain of the output MOSFET which, in turn, will appear at the DRAIN pin of the MIC2589/95. In both cases, it is good engineering practice to include protective measures to avoid damaging sensitive ICs or the hot swap controller from these large-scale transients. Two typical scenarios in which large-scale transients occur are described below:

1. An output current load dump with no bypass (charge bucket or bulk) capacitance to V_{EE}. For example, if L_{LOAD} = 5µH, V_{IN} = 56V and t_{OFF} = 0.7µs, the resulting peak short-circuit current prior to the MOSFET turning off would reach:

$$\frac{(55V \times 0.7\mu s)}{5\mu H} = 7.7A$$

   If there is no other path for this current to take when the MOSFET turns off, it will avalanche the drain-source junction of the MOSFET. Since the total energy represented is small relative to the sturdiness of modern power MOSFETs, it's unlikely that this will damage the transistor. However, the actual avalanche voltage is unknown; all that can be guaranteed is that it will be greater than the $V_{BD(D-S)}$ of the MOSFET. The drain of the transistor is connected to the DRAIN pin of the MIC2589/95, and the resulting transient does have enough voltage and energy and can damage this, or any, high-voltage hot swap controller.
2. If the load's bypass capacitance (for example, the input filter capacitors for a set of DC-DC converter modules) are on a board from which the board with the MIC2589/95 and the MOSFET can be unplugged, the same type of inductive transient damage can occur to the MIC2589/95.

Protecting the controller and the power MOSFET from damage against these large-scale transients can take the forms shown in Figure 8. It is not mandatory that these techniques are used - the application environment will dictate suitability. As protection against sudden on-card load dumps at the DRAIN pin of the controller, a 2.2µF or larger capacitor directly from DRAIN to VEE of the controller can be used to serve as a charge reservoir. Alternatively, a 68V, 1W, 5% Zener diode clamp can be installed in a similar fashion. Note that the clamp diode's cathode is connected to the DRAIN pin as shown in Figure 8. To protect the hot swap controller from large-scale transients at the card input, a 100V clamp diode (an SMAT70A or equivalent) can be used. In either case, the lead lengths should be short and the layout compact to prevent unwanted transients in the protection circuit.

[Circuit drawing under construction]

Figure 8. Using Large-Scale Transient Protection Devices Around the MIC2589/95 and the MIC2589R/95R

The same logic applies to the input of the MIC2589/95 circuit. Power bus inductance could easily result in localized high-voltage transients during a turn-off event. The potential for overstressing the part in such a case should be kept in check with a suitable input capacitor and/or transient clamping diode.

Power MOSFET Selection

[Section under construction]

Power MOSFET Operating Voltage Requirements

[Section under construction]

Power MOSFET Steady-State Thermal Issues

[Section under construction]

Power MOSFET Transient Thermal Issues

[Section under construction]

PCB Layout Considerations

[Section under construction]

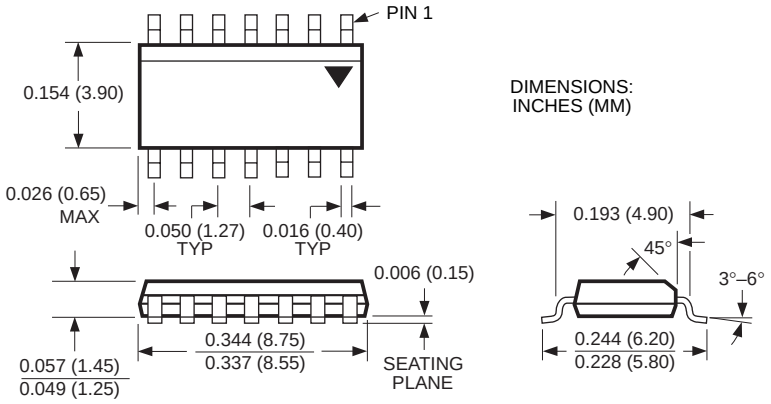
Power MOSFET and Sense Resistor Vendors

Table 1 shows some of the various sense resistor types available for use with the MIC2589/95 product family.

Resistor Vendors	Resistor Types	Contact Data
Vishay (Dale)	"WSL" Series	www.vishay.com/docs/wsl_30100.pdf (203)452-5664
IRC	"OARS" Series "LR" Series (second source to "WSL")	www.irctt.com/pdf_files/OARS.pdf www.irctt.com/pdf_files/LRC.pdf (828) 264-8861

Table 1. Suggested Sense Resistors

Package Information



14-Pin SOIC (M)

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