



CY7C1018V33 CY7C1019V33

128K x 8 Static RAM

Features

- High speed
— $t_{AA} = 10 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE} and \overline{OE} options

Functional Description

The CY7C1018V33/CY7C1019V33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

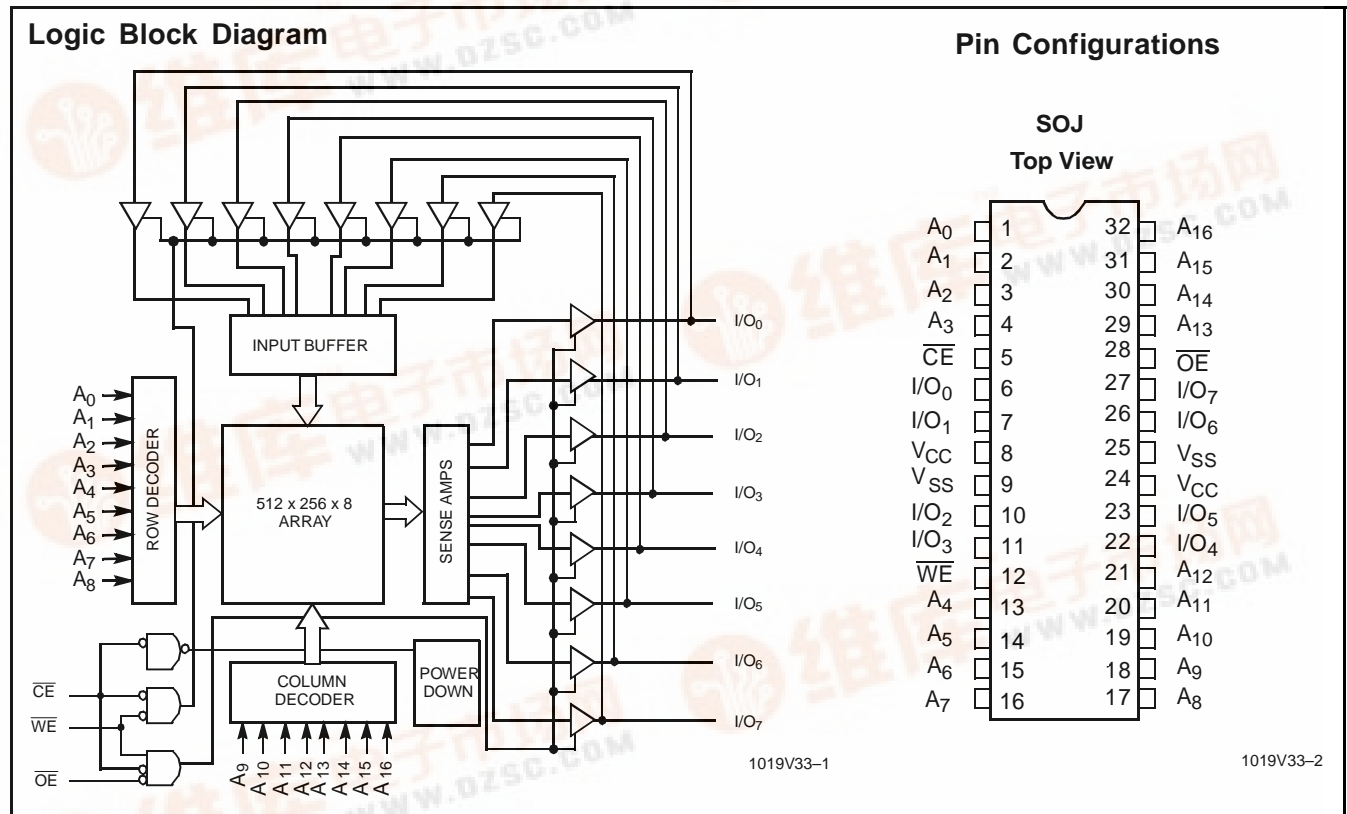
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O

pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1018V33 is available in a standard 300-mil-wide SOJ and CY7C1019V33 is available in a standard 400-mil-wide package. The CY7C1018V33 and CY7C1019V33 are functionally equivalent in all other respects.



Selection Guide

	7C1019V33-10	7C1018V33-12 7C1019V33-12	7C1018V33-15 7C1019V33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	175	160	145
Maximum Standby Current (mA)	5	5	5
L	—	0.5	0.5





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
- DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

- Current into Outputs (LOW) 20 mA
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1019V33-10		7C1018V33-12 7C1019V33-12		7C1018V33-15 7C1019V33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	µA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		175		160		145	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		20		20		20	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		5		5		5	mA
			L	-		0.5		0.5	

Capacitance^[3]

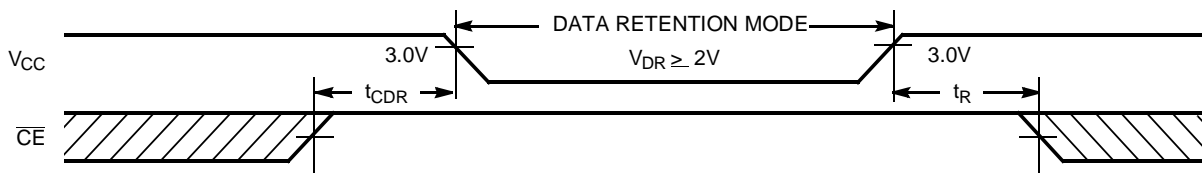
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

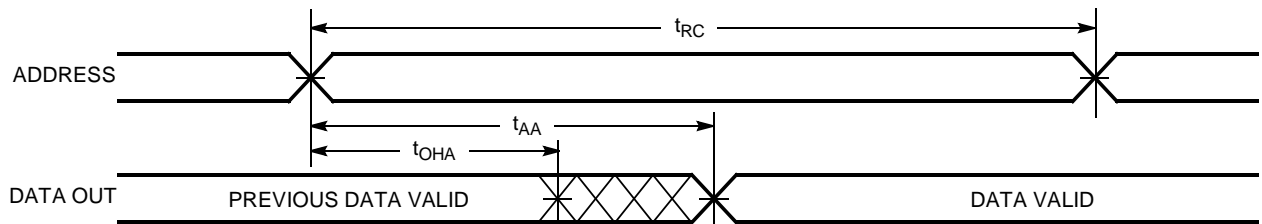
1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics Over the Operating Range (L Version Only)

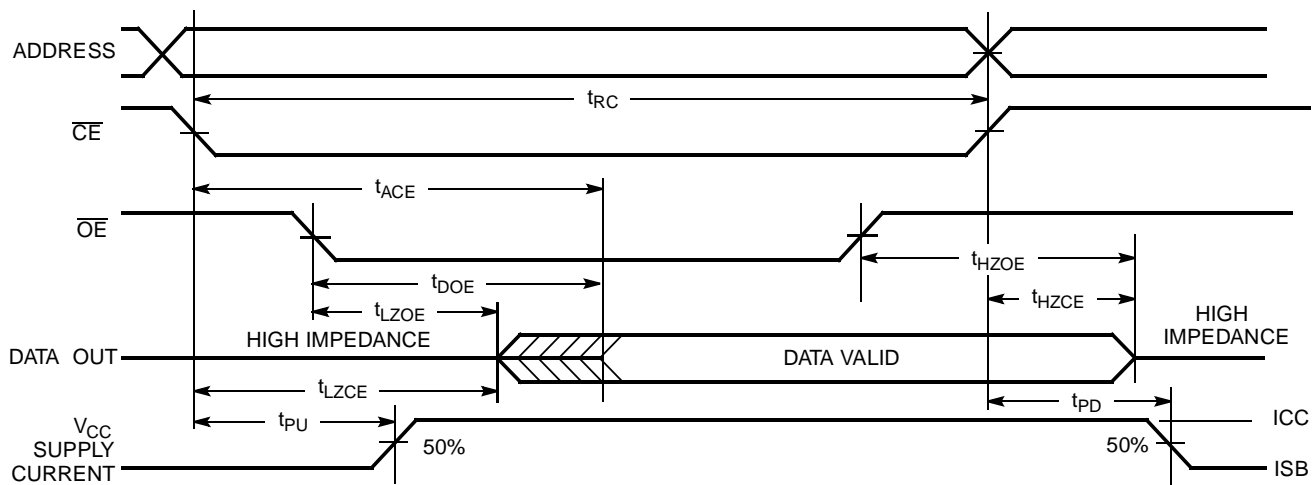
Parameter	Description	Conditions	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed $V_{CC} + 0.5V$	2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$,		150	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
t_R	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform


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Switching Waveforms
Read Cycle No. 1 ^[9, 10]


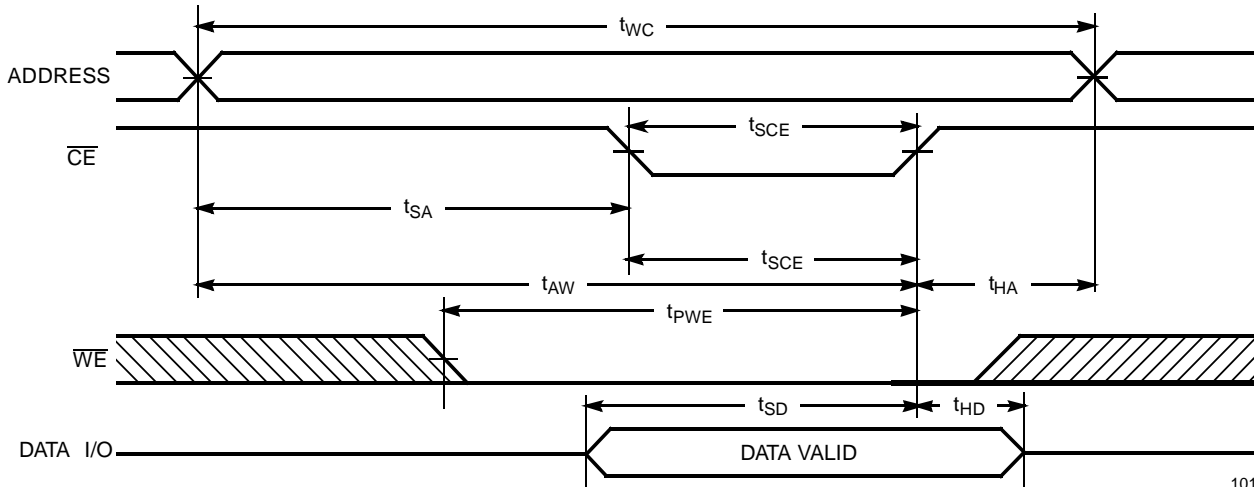
1019V33-6

Read Cycle No. 2 (\overline{OE} Controlled) ^[10, 11]


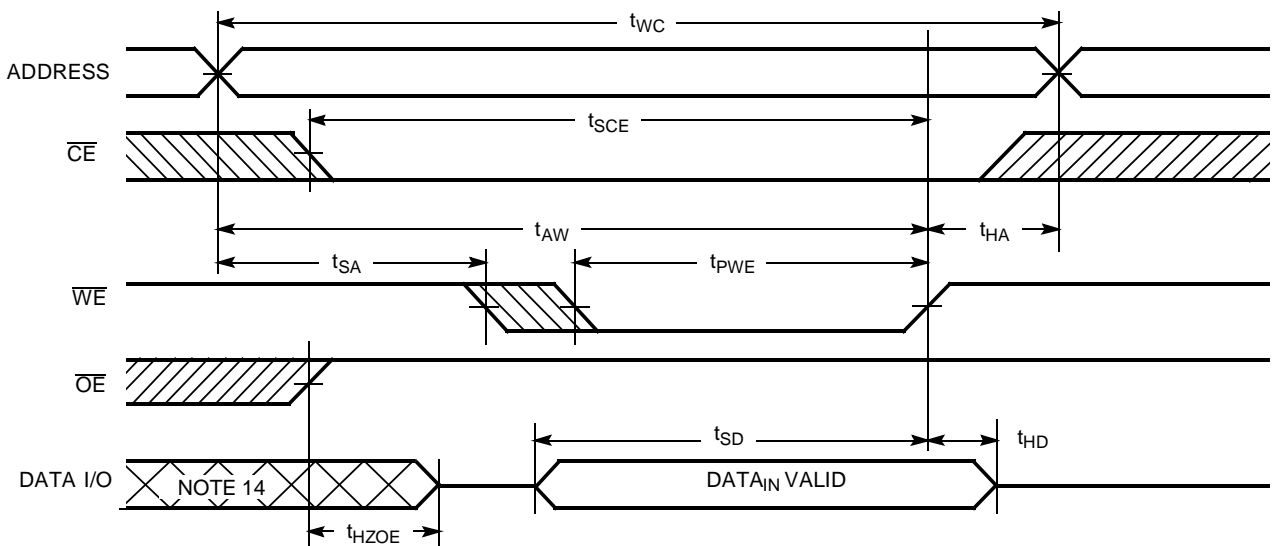
1019V33-7

Notes:

9. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
10. \overline{WE} is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[12, 13]


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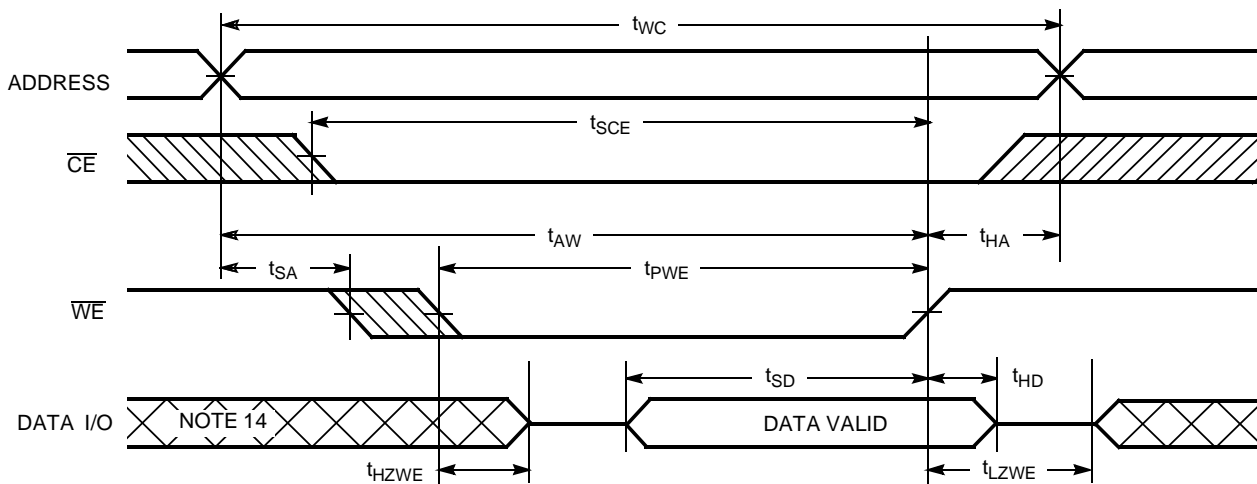
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[12, 13]


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Notes:

12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[13]


1019V33-10

Truth Table

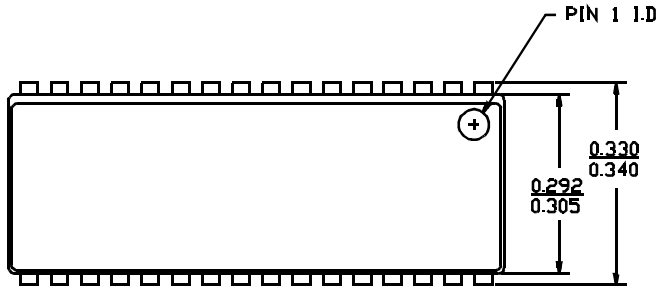
\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1018V33-12VC	V32	32-Lead 300-Mil Molded SOJ	Commercial
	CY7C1018V33L-12VC	V32	32-Lead 300-Mil Molded SOJ	
15	CY7C1018V33-15VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1018V33L-15VC	V32	32-Lead 300-Mil Molded SOJ	
10	CY7C1019V33-10VC	V33	32-Lead 400-Mil Molded SOJ	
12	CY7C1019V33-12VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019V33L-12VC	V33	32-Lead 400-Mil Molded SOJ	
15	CY7C1019V33-15VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019V33L-15VC	V33	32-Lead 400-Mil Molded SOJ	

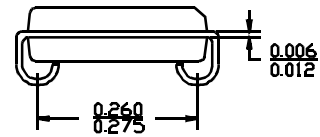
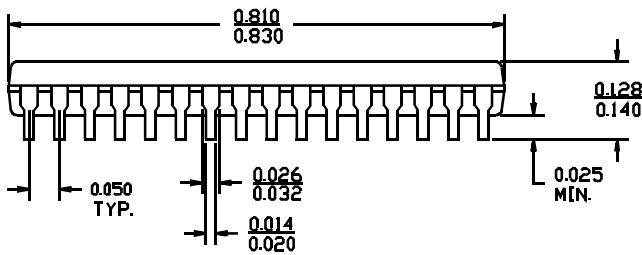
Package Diagram

32-Lead (300-Mil) Molded SOJ V32



DIMENSIONS IN INCHES MIN. MAX.

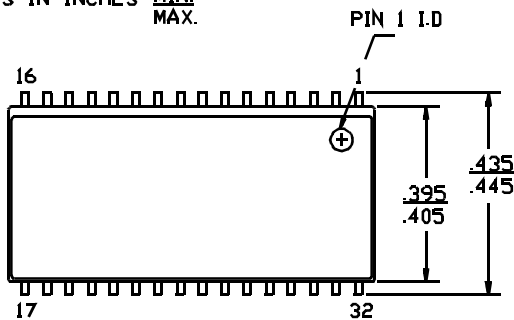
LEAD COPLANARITY 0.004 MAX.



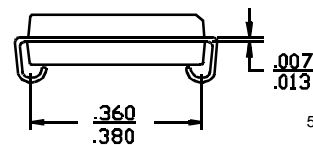
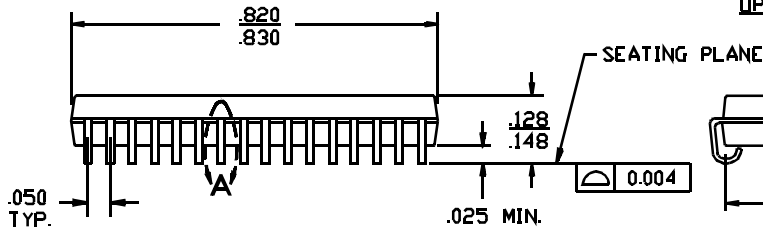
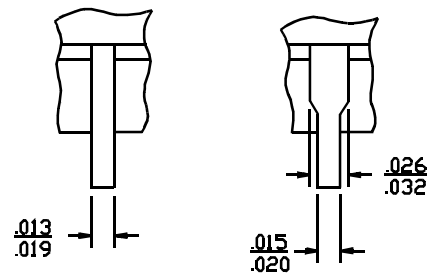
51-85041-A

32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES MIN. MAX.



DETAIL A
EXTERNAL LEAD DESIGN



51-85033-A