CY7C1018V33 CY7C1019V33



128K x 8 Static RAM

Features

- High speed
 --t_{AA} = 10 ns
- CMOS for optimum speed/power
- · Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with CE and OE options

Functional Description

The CY7C1018V33/CY7C1019V33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}) , an active LOW Output Enable (\overline{OE}) , and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

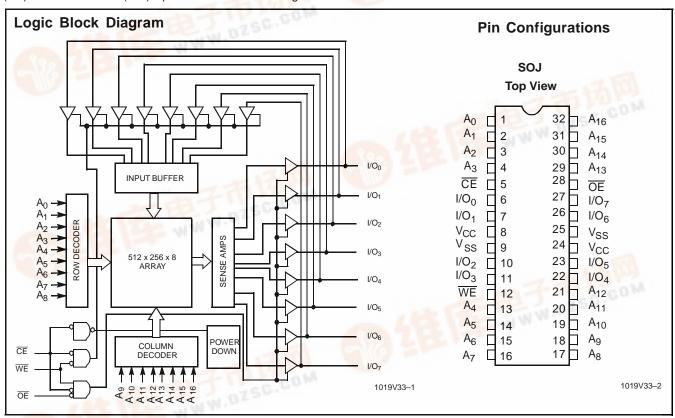
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O

pins (I/O $_0$ through I/O $_7$) is then written into the location specified on the address pins (A $_0$ through A $_{16}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O $_0$ through I/O $_7$) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1018V33 is available in a standard 300-mil-wide SOJ and CY7C1019V33 is available in a standard 400-mil-wide package. The CY7C1018V33 and CY7C1019V33 are functionally equivalent in all other respects.



Selection Guide

1112		7C1019V33-10	7C1018V33-12 7C1019V33-12	7C1018V33-15 7C1019V33-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)		175	160	145
Maximum Standby Current (mA)		5	5	5
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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.) Storage Temperature-65°C to +150°C Ambient Temperature with Power Applied –55°C to +125°C Supply Voltage on V_{CC} to Relative $\mbox{GND}^{[1]}\,....\,-0.5\mbox{V}$ to +7.0V DC Voltage Applied to Outputs in High Z State $^{[1]}$ -0.5V to V CC + 0.5V DC Input Voltage^[1].....-0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Range	Range Ambient Temperature ^[2]	
Commercial	0°C to +70°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

		Test Conditions		7C1019V33-10		7C1018V33-12 7C1019V33-12				
Parameter	Description			Min.	Max.	Min.	Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	V _{CC} = Min.,		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V_{IL}	Input LOW Voltage ^[1]			-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		-1	+1	-1	+1	-1	+1	μΑ
I _{OZ}	Output Leakage Current	$\begin{array}{l} \text{GND} \leq \text{V}_{\text{I}} \leq \text{V}_{\text{CC}}, \\ \text{Output Disabled} \end{array}$		- 5	+5	-5	+5	-5	+5	μΑ
I _{CC}	V _{CC} Operating Supply Current	$V_{CC} = Max.,$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$			175		160		145	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	$\begin{aligned} &\text{Max. V}_{CC}, \overline{CE} \geq \text{V}_{IH} \\ &\text{V}_{IN} \geq \text{V}_{IH} \text{ or} \\ &\text{V}_{IN} \leq \text{V}_{IL}, f = f_{MAX} \end{aligned}$			20		20		20	mA
I _{SB2}	Automatic CE	Max. V _{CC} ,			5		5		5	mA
	Power-Down Current —CMOS Inputs	r-Down Current $\overline{CE} \ge V_{CC} - 0.3V$,			-		0.5		0.5	

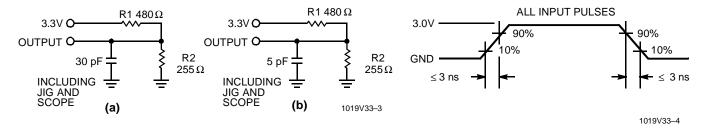
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C$, $f = 1$ MHz,	6	pF
C _{OUT}	Output Capacitance	$V_{CC} = 5.0V$	8	pF

- 1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.
 Tested initially and after any design or process changes that may affect these parameters.



AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics^[4] Over the Operating Range

		7C1019	9V33-10		3V33-12 3V33-12		3V33-15 9V33-15		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit	
READ CYC	READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns	
t _{AA}	Address to Data Valid		10		12		15	ns	
t _{OHA}	Data Hold from Address Change	3		3		3		ns	
t _{ACE}	CE LOW to Data Valid		10		12		15	ns	
t _{DOE}	OE LOW to Data Valid		5		6		7	ns	
t _{LZOE}	OE LOW to Low Z	0		0		0		ns	
t _{HZOE}	OE HIGH to High Z ^[5, 6]		5		6		7	ns	
t _{LZCE}	CE LOW to Low Z ^[6]	3		3		3		ns	
t _{HZCE}	CE HIGH to High Z ^[5, 6]		5		6		7	ns	
t _{PU}	CE LOW to Power-Up	0		0		0		ns	
t _{PD}	CE HIGH to Power-Down		10		12		15	ns	
WRITE CYC	CLE ^[7, 8]	1	•	•	•	•	•		
t _{WC}	Write Cycle Time	10		12		15		ns	
t _{SCE}	CE LOW to Write End	8		9		10		ns	
t _{AW}	Address Set-Up to Write End	7		8		10		ns	
t _{HA}	Address Hold from Write End	0		0		0		ns	
t _{SA}	Address Set-Up to Write Start	0		0		0		ns	
t _{PWE}	WE Pulse Width	7		8		10		ns	
t _{SD}	Data Set-Up to Write End	5		6		8		ns	
t _{HD}	Data Hold from Write End	0		0		0		ns	
t _{LZWE}	WE HIGH to Low Z ^[6]	3		3		3		ns	
t _{HZWE}	WE LOW to High Z ^[5, 6]		5		6		7	ns	

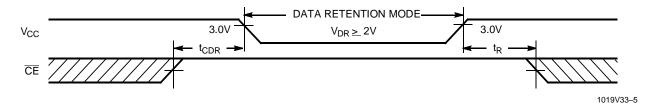
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- 6
- t_{HZOE}, t_{HZOE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}. 7.



Data Retention Characteristics Over the Operating Range (L Version Only)

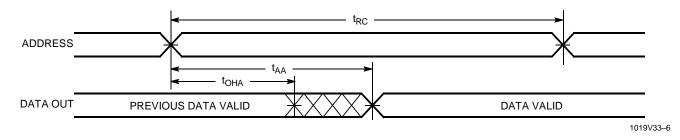
Parameter	Description	Min.	Max	Unit	
V_{DR}	V _{CC} for Data Retention	No input may exceed V _{CC} + 0.5V	2.0		V
I _{CCDR}	Data Retention Current	$\frac{V_{CC}}{CE} = V_{DR} = 2.0V,$ $CE \ge V_{CC} - 0.3V,$		150	μΑ
t _{CDR} ^[3]	Chip Deselect to Data Retention Time	$V_{\text{IN}} \ge V_{\text{CC}} - 0.3 \text{V or } V_{\text{IN}} \le 0.3 \text{V}$	0		ns
t _R	Operation Recovery Time		t _{RC}		ns

Data Retention Waveform

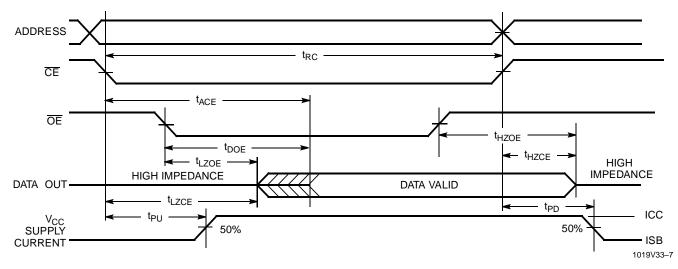


Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)[10, 11]

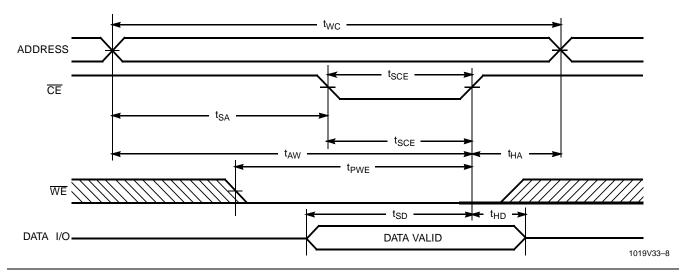


- Device is continuously selected. OE, CE = V_{IL}.
 WE is HIGH for read cycle.
 Address valid prior to or coincident with CE transition LOW.

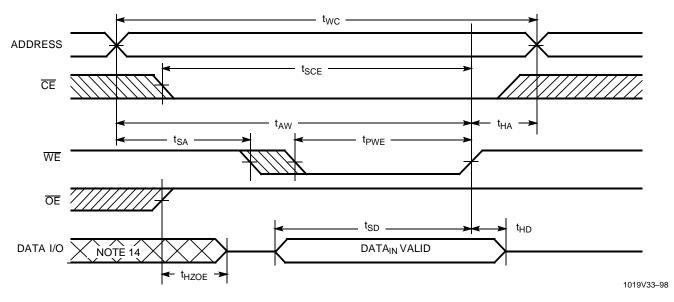


Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)[12, 13]



Write Cycle No. 2 (WE Controlled, OE HIGH During Write)[12, 13]

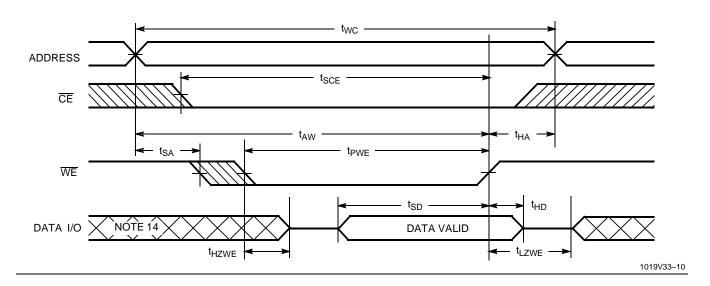


- 12. Data I/O is high impedance if OE = V_{IH}.
 13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
 14. During this period the I/Os are in the output state and input signals should not be applied.



Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[13]



Truth Table

CE	OE	WE	I/O ₀ –I/O ₇	Mode	Power
Н	Х	Х	High Z	Power-Down	Standby (I _{SB})
Х	Х	Х	High Z	Power-Down	Standby (I _{SB})
L	L	Н	Data Out	Read	Active (I _{CC})
L	Х	L	Data In	Write	Active (I _{CC})
L	Н	Н	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

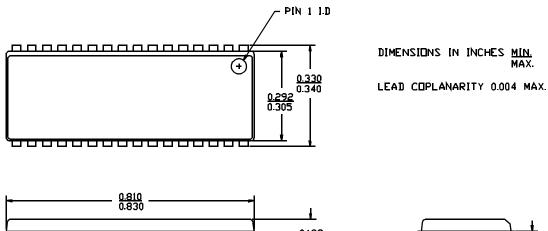
Speed		Package		Operating
(ns)	Ordering Code	Name	Package Type	Range
12	CY7C1018V33-12VC	V32	32-Lead 300-Mil Molded SOJ	Commercial
	CY7C1018V33L-12VC	V32	32-Lead 300-Mil Molded SOJ	
15	CY7C1018V33-15VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1018V33L-15VC	V32	32-Lead 300-Mil Molded SOJ	
10	CY7C1019V33-10VC	V33	32-Lead 400-Mil Molded SOJ	
12	CY7C1019V33-12VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019V33L-12VC	V33	32-Lead 400-Mil Molded SOJ	
15	CY7C1019V33-15VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019V33L-15VC	V33	32-Lead 400-Mil Molded SOJ	

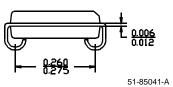
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Package Diagram

32-Lead (300-Mil) Molded SOJ V32





32-Lead (400-Mil) Molded SOJ V33

0.025 M[N.

