查询MB89689供应商 捷多邦，专业PCB打样工厂，24小时加急出货

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12525-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89680 Series

MB89689/P689/W689/PV680

PRELIMINARY

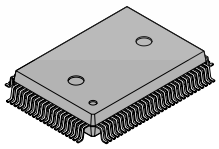
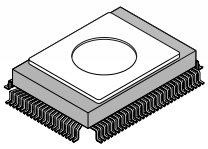
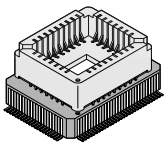
■ OUTLINE

The MB89680 series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, four operating speed control stages, timers, PWM timer, a serial interface, a UART, an A/D converter, and an external interrupt.

■ FEATURES

- F²MC-8L family CPU core
- Dual-clock control system
- Maximum memory space: 64 Kbytes
- Minimum execution time: 0.5 µs/8 MHz
- Interrupt processing time: 4.5 µs/8 MHz
- I/O ports: max. 85 channels
- 21-bit timebase counter
- 8-bit PWM timer
- 8/16-bit timer
- UART
- Serial I/O with 1-byte buffer
- 8-bit A/D converter
- Pulse width counter
- Modem signal output
- External interrupts: 16 channels
- Power-on reset function
- Low-power consumption modes (subclock mode, watch mode, sleep mode, and stop mode)
- CMOS technology

■ PACKAGE

100-pin Plastic QFP	100-pin Ceramic QFP	100-pin Ceramic MQFP
		
(FPT-100P-M06)	(FPT-100C-A02)	(MQP-100C-P01)

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■ PRODUCT LINEUP

Item \ Part number	MB89689	MB89P689	MB89W689	MB89PV680
Classification	Mass-produced product (mask ROM product)	One-time PROM product	EPROM product	Piggyback/ evaluation product (for development)
ROM size	60 K × 8 bits (internal mask ROM)	60 K × 8 bits (internal PROM)	60 K × 8 bits (internal EPROM)	60 K × 8 bits (external ROM)
RAM size	2.0 K × 8 bits			
Instruction bit length	8 bits			
Instruction length	1 byte to 3 bytes			
Data bit length	1, 8, 16 bits			
Number of instructions	136			
Clock generator	Built-in			
Minimum execution time	0.5 µs/8 MHz to 8 µs/8 MHz, 61 µs/32.768 kHz			
Interrupt processing time	4.5 µs/8 MHz to 72 µs/8 MHz, 562.5 µs/32.768 kHz			
Ports ( ) indicate dual function ports	Output ports (N-ch open-drain): 21 (8) Output ports (CMOS): 8 (0) I/O ports (N-ch open-drain): 8 (6) I/O ports (CMOS): 48 (29) Total: 85 (43)			
8-bit PWM timer	8 bits × 1 channel			
8/16-bit timer/counter	8 bits × 2 channels, or 16 bits × 1 channel			
8-bit serial I/O	With 1-byte buffer × 1 channel			
8-bit A/D converter	8 bits × 8 channels			
UART	Full-duplex double buffer Transfer data length: 6 bits to 8 bits 8 baud rates selectability, external clock available			
Pulse width counter	5-bit noise reduction circuit Pulse edge detectable and selectable (rising, falling, and both edges)			
Software modem transmission circuit	1200-bps/2400-bps modem output			
External interrupt	16 channels			
Timebase timer	21 bits			
Watch prescaler	15 bits			
Standby mode	Watch mode, subclock mode, sleep mode, and stop mode			
Process	CMOS			
Power supply voltage*	2.2 V to 6.0 V	2.7 V to 6.0 V		
EPROM for use				MBM27C512-20TV

* : Varies with conditions such as the operating frequency. (See section “■ ELECTRICAL CHARACTERISTICS.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89689 MB89P689	MB89W689	MB89PV680
FPT-100P-M06	○	×	×
FPT-100C-A02	×	○	×
MQP-100C-P01	×	×	○

○ : Available　× : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used.

2. Current Consumption

In the case of the MB89PV680, add the current consumed by the EPROM which is connected to the top socket.

When operated at low speed, the product with an OTPROM or an EPROM will consume more current than the product with a mask ROM.

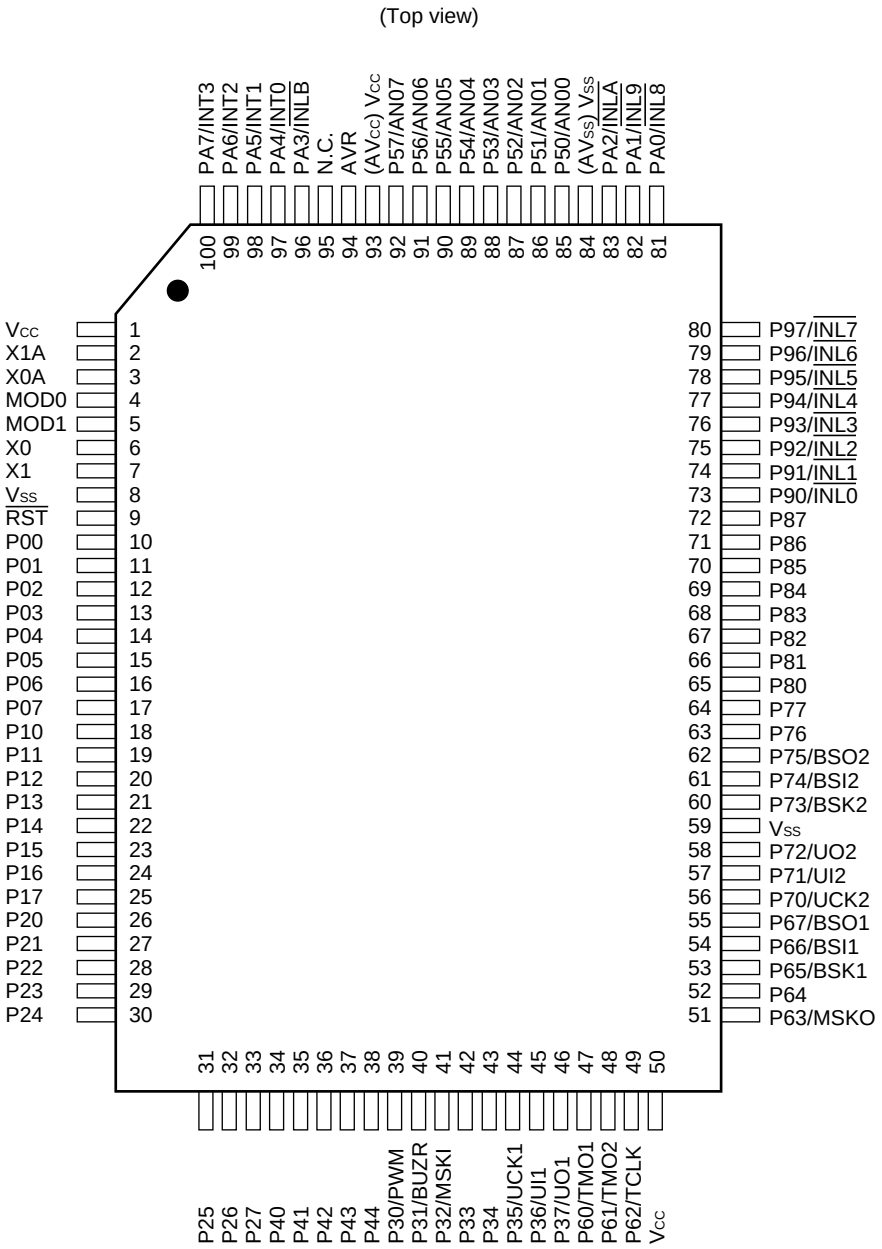
However, the current consumption in sleep/stop modes is the same.

3. Mask Options

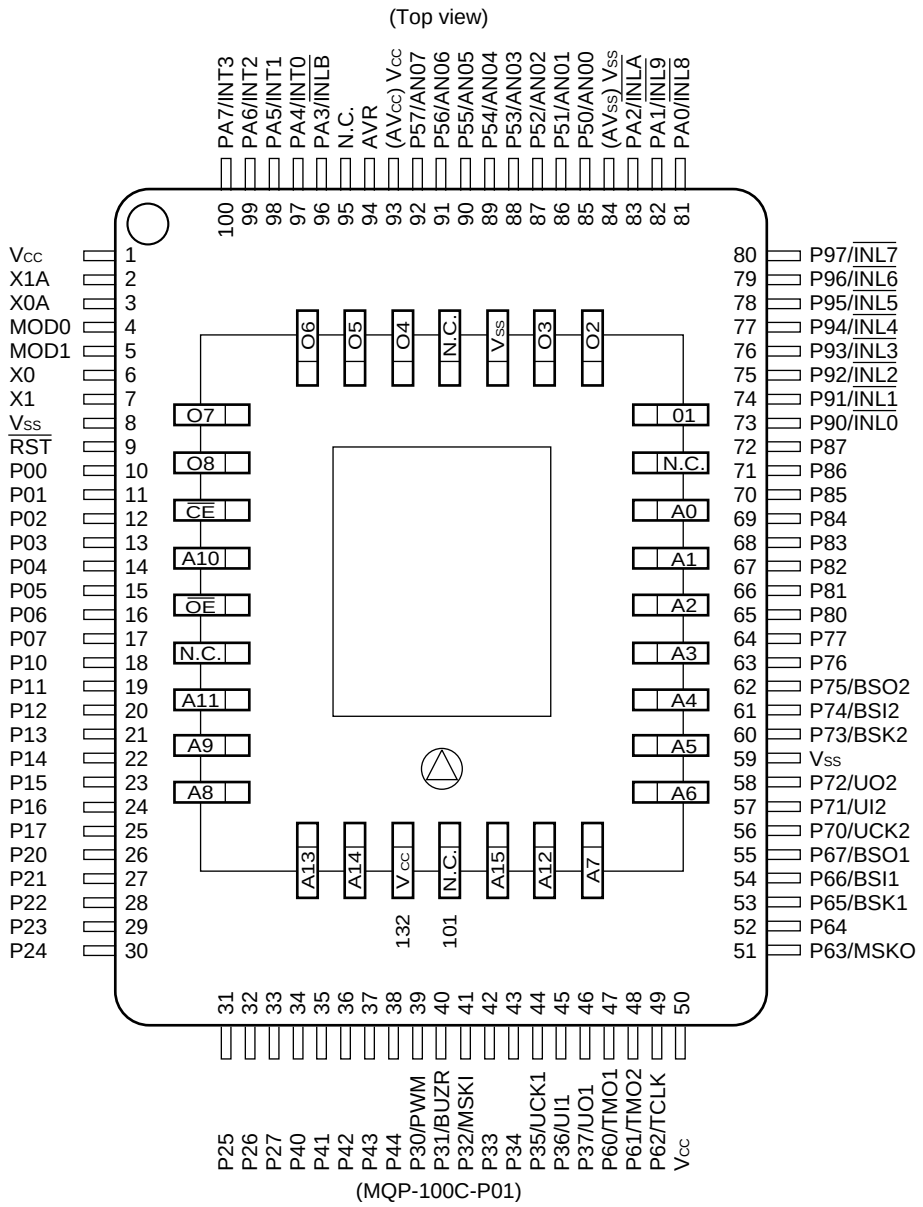
Functions that can be selected as options and how to designate these options vary by the product. Before using options check section "■ Mask Options." Take particular care on the following points:

- Options are fixed on the MB89PV680.

■ PIN ASSIGNMENT



(FPT-100P-M06)
(FPT-100C-A02)



- **Pin assignment on package top (MB89PV680 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
101	N.C.	109	A2	117	N.C.	125	$\overline{OE}$
102	A15	110	A1	118	O4	126	N.C.
103	A12	111	A0	119	O5	127	A11
104	A7	112	N.C.	120	O6	128	A9
105	A6	113	O1	121	O7	129	A8
106	A5	114	O2	122	O8	130	A13
107	A4	115	O3	123	$\overline{CE}$	131	A14
108	A3	116	V_{SS}	124	A10	132	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no. QFP*1, MQFP*2	Pin name	Circuit type	Function
1	V_{CC}	—	Power supply pin
2	X1A	A	Subclock crystal oscillator pins (32.768 kHz)
3	X0A		
4	MOD0	B	Operating mode selection pins Connect to V_{SS} (GND) when using.
5	MOD1		
6	X0	A	Main clock crystal oscillator pins (8 MHz)
7	X1		
8	V_{SS}	—	Power supply (GND) pin
9	$\overline{RST}$	C	Reset input pin
10 to 17	P00 to P07	D	General-purpose I/O ports
18 to 25	P10 to P17	D	General-purpose I/O ports
26 to 33	P20 to P27	F	General-purpose output ports
34 to 38	P40 to P44	I	General-purpose output ports
39	P30/PWM	E	General-purpose I/O port Also serve as an 8-bit PWM.
40	P31/BUZR	E	General-purpose I/O port Also serve as a buzzer output.
41	P32/MSKI	E	General-purpose I/O port Also serve as a pulse width counter.
42, 43	P33, P34	E	General-purpose I/O ports
44, 45, 46	P35/UCK1, P36/UI1, P37/UO1	E	General-purpose I/O ports Also serve as a UART I/O 1.
47, 48, 49	P60/TMO1, P61/TMO2, P62/TCLK	E	General-purpose I/O ports Also serve as an 8/16-bit timer.
50	V_{CC}	—	Power supply pin
51	P63/MSKO	E	General-purpose I/O port Also serve as a modem output.
52	P64	E	General-purpose I/O port
53, 54, 55	P65/BSK1, P66/BSI1, P67/BSO1	E	General-purpose I/O ports Also serve as a serial I/O 1 with 1-byte buffer.

*1: FPT-100P-M06, FPT-100C-A02
*2: MQP-100C-P01

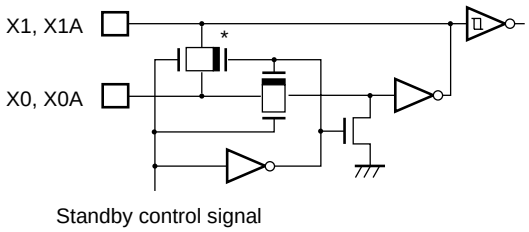
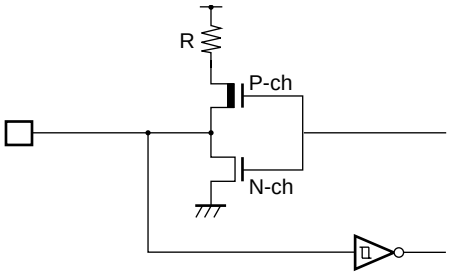
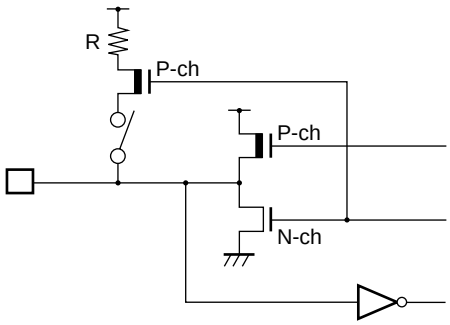
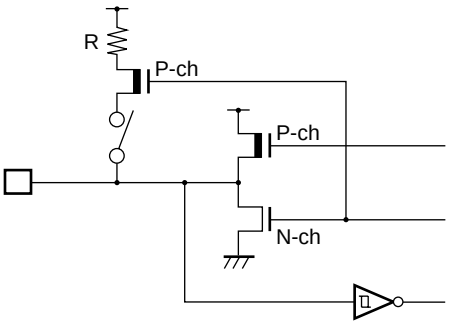
(Continued)

(Continued)

Pin no. QFP*1, MQFP*2	Pin name	Circuit type	Function
56, 57, 58	P70/UCK2, P71/UI2, P72/UO2	H	General-purpose I/O ports Also serve as a UART I/O 2.
59	V_{SS}	—	Power supply (GND) pin
60, 61, 62	P73/BSK2, P74/BSI2, P75/BSO2	H	General-purpose I/O ports Also serve as a serial I/O 2 with 1-byte buffer.
63, 64	P76, P77	H	General-purpose I/O ports
65 to 72	P80 to P87	I	General-purpose output ports
73 to 80	P90/$\overline{\text{INL0}}$ to P97/$\overline{\text{INL7}}$	E	General-purpose I/O ports External interrupt input is hysteresis input.
81 to 83	PA0/$\overline{\text{INL8}}$ to PA2/$\overline{\text{INLA}}$	E	General-purpose I/O ports External interrupt input is hysteresis input.
84	V_{SS} (AV_{SS})	—	(A/D converter) power supply (GND) pin
85 to 92	P50/AN00 to P57/AN07	G	General-purpose I/O ports Also serve as an analog input.
93	V_{CC} (AV_{CC})	—	(A/D converter) power supply pin
94	AVR	—	A/D converter reference voltage input pin
95	N.C.	—	Internally connected pins Be sure to leave them open.
96 to 100	PA3/$\overline{\text{INLB}}$, PA4/INT0 to PA7/INT3	E	General-purpose I/O ports External interrupt input is hysteresis input.

*1: FPT-100P-M06, FPT-100C-A02
*2: MQP-100C-P01

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Main clock (A2) (At an oscillation feedback resistor of approximately 1 MΩ/5.0 V) • Subclock (A1) (At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V * The subclock circuit in the MB89PV680 contains no oscillation feedback resistor.
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional
E		• CMOS output • Hysteresis input • Pull-up resistor optional

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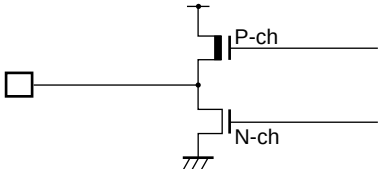
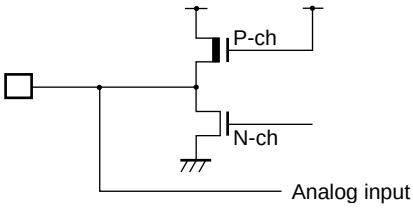
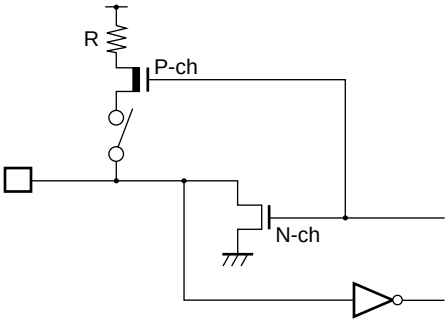
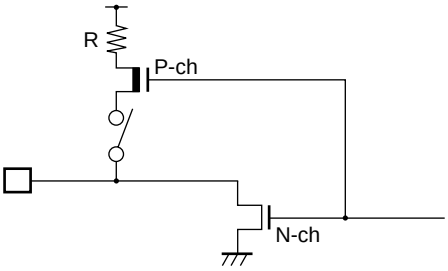
Type	Circuit	Remarks
F		• CMOS output
G		• N-ch open-drain output • Analog input
H		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional
I		• N-ch open-drain output • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P689/W689

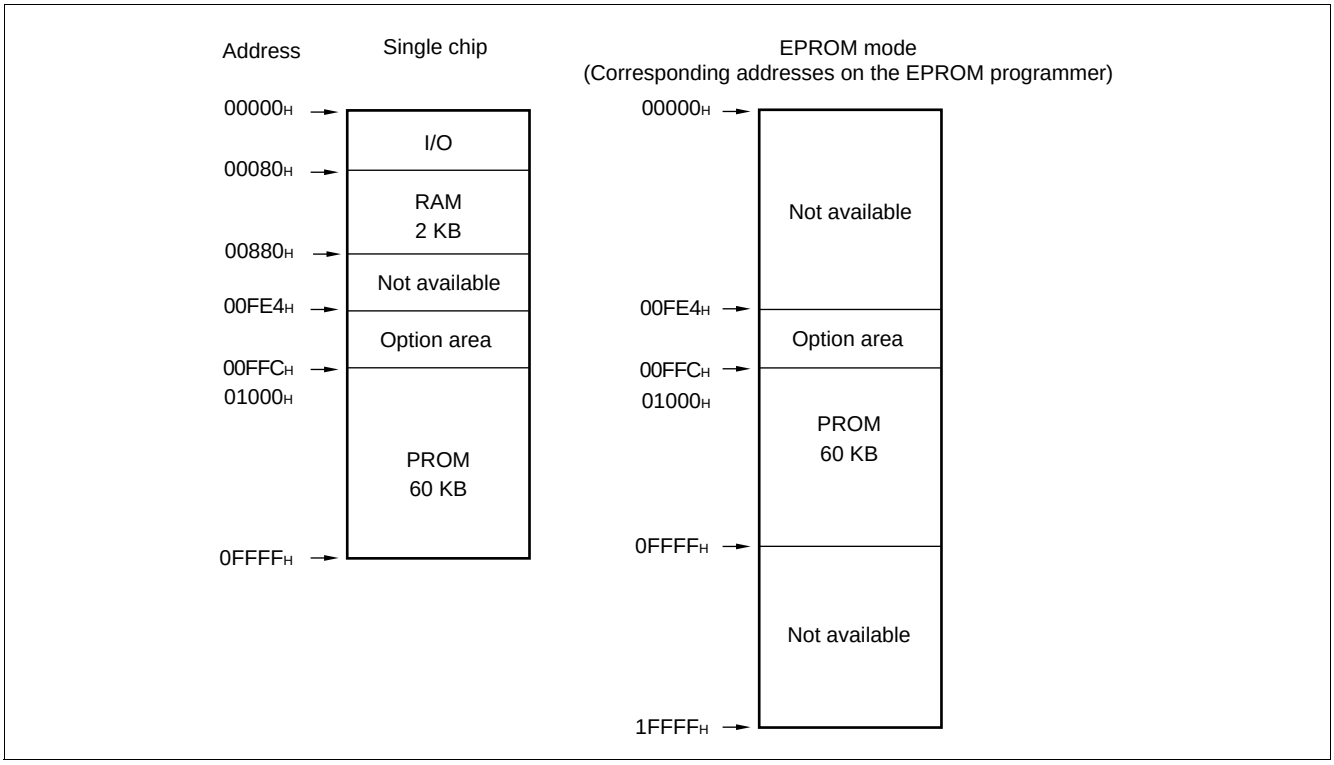
The MB89P689/W689 is an OTPROM version of the MP89680 series.

1. Features

- 60-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalent to the MBM27C1001 in EPROM mode (when programmed with the EPROM programmer) and supporting the 4-byte programming mode

2. Memory Space

Memory space in each mode such as 60-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P689 functions equivalent to the MBM27C1001. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 60 Kbytes (1000H to FFFFH) the PROM can be programmed as follows:

- **Programming procedure**

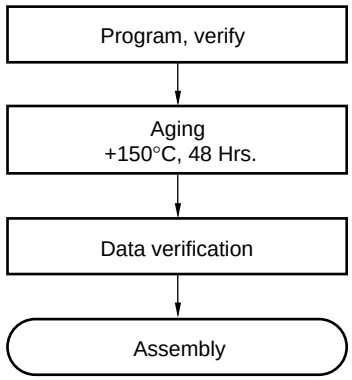
(1) Set the EPROM programmer to MBM27C1001.

(2) Load program data into the EPROM programmer at 1000H to FFFFH.
Load option data into addresses 0FE4H to 0FFCH of the EPROM programmer. (For information about each corresponding option, see “8. Setting PROM Options.”)

(3) Program to 0FE4H to 0FFCH and 1000H to FFFFH with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. MB89W689 Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolent lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000µW/cm^2 for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure time will be much longer than with UV source at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

7. EPROM Programmer Socket Adapter

Part no.	MB89P689PF
Package	QFP-100
Compatible socket adapter Sun Hayato Co., Ltd.	ROM-100QF-32DP-8LA

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

8. Setting PROM Options

The programming procedure is the same as that for the program data. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **PROM option bit map**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00FE4H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual-clock system 1: Dual clock 2: Single clock	Reset output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization time 11 $2^{18}/F_{CH}$ 01 $2^{12}/F_{CH}$	 10 $2^{16}/F_{CH}$ 00 $2^{3}/F_{CH}$
00FE8H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
00FECH	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
00FF0H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
00FF4H	P67 Pull-up Readable and writable	P66 Pull-up Readable and writable	P65 Pull-up Readable and writable	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
00FF8H	P97 Pull-up 1: No 0: Yes	P96 Pull-up 1: No 0: Yes	P95 Pull-up 1: No 0: Yes	P94 Pull-up 1: No 0: Yes	P93 Pull-up 1: No 0: Yes	P92 Pull-up 1: No 0: Yes	P91 Pull-up 1: No 0: Yes	P90 Pull-up 1: No 0: Yes
00FFCH	PA7 Pull-up 1: No 0: Yes	PA6 Pull-up 1: No 0: Yes	PA5 Pull-up 1: No 0: Yes	PA4 Pull-up 1: No 0: Yes	PA3 Pull-up 1: No 0: Yes	PA2 Pull-up 1: No 0: Yes	PA1 Pull-up 1: No 0: Yes	PA0 Pull-up 1: No 0: Yes

Notes:
- Note that the option setting area addresses are at intervals of four addresses to support the 4-byte programming mode.
- In three bytes between adjacent setup addresses, the value written to the preceding setup address is mirrored. Be sure to set the same data in the programmer.
- Each bit is set to ‘1’ as the initialized value.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

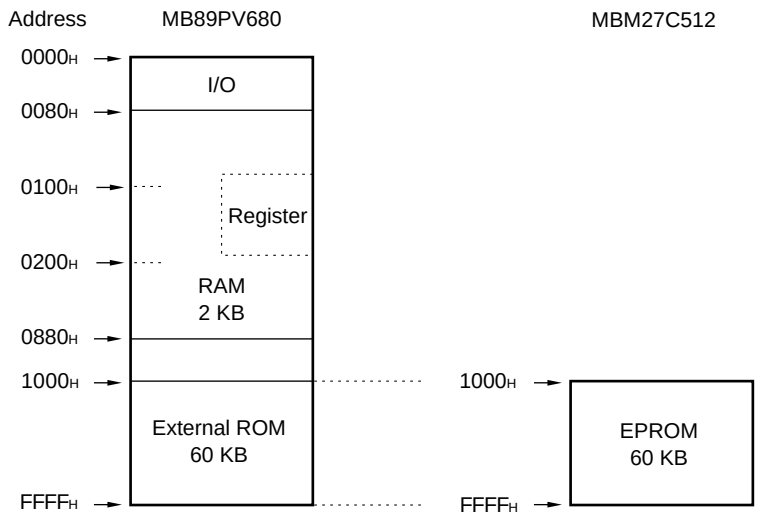
MBM27C512-20TV

2. Programming Socket Adapter

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

3. Memory Space



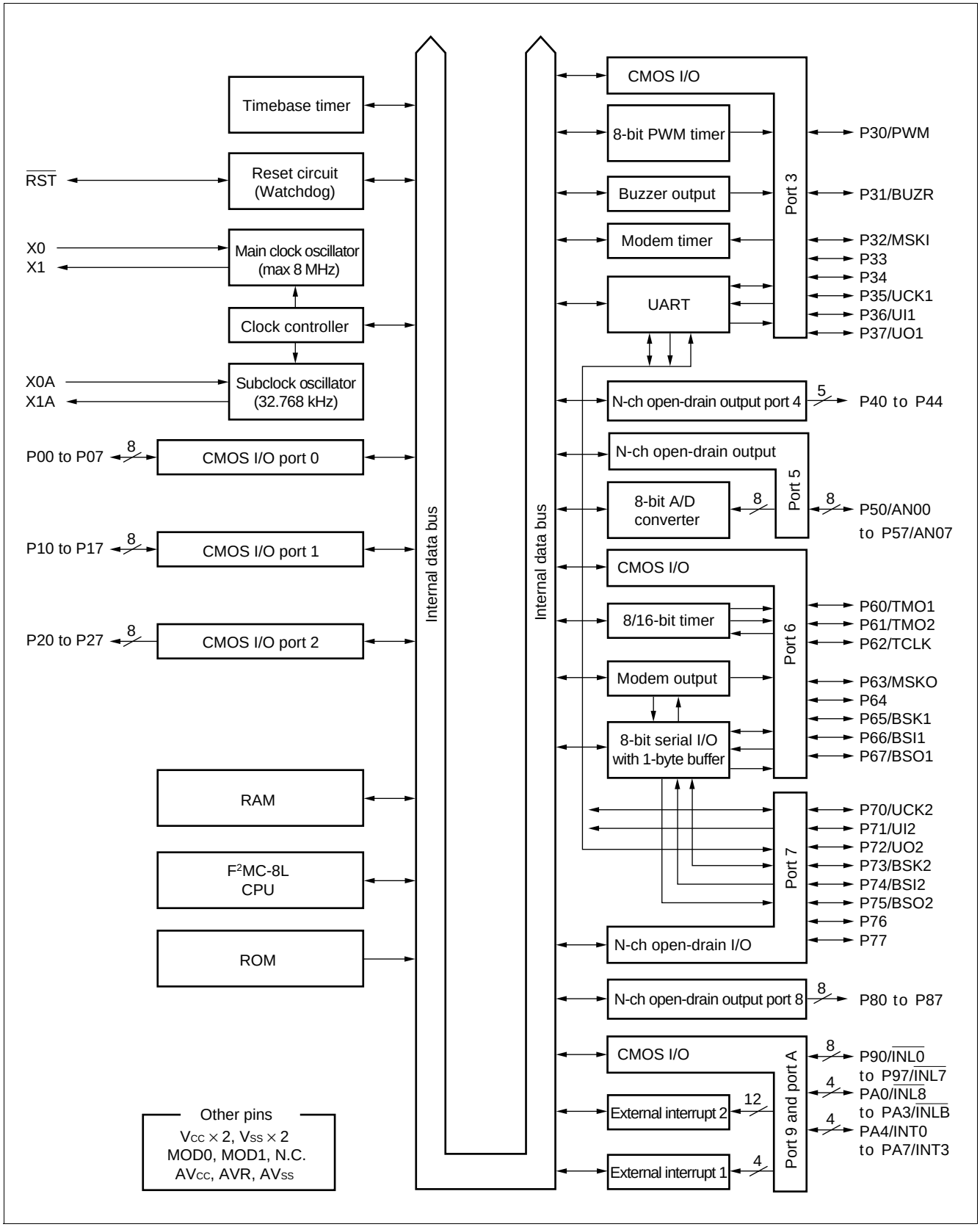
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 1000_H to $FFFF_H$.

(3) Program to 1000_H to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

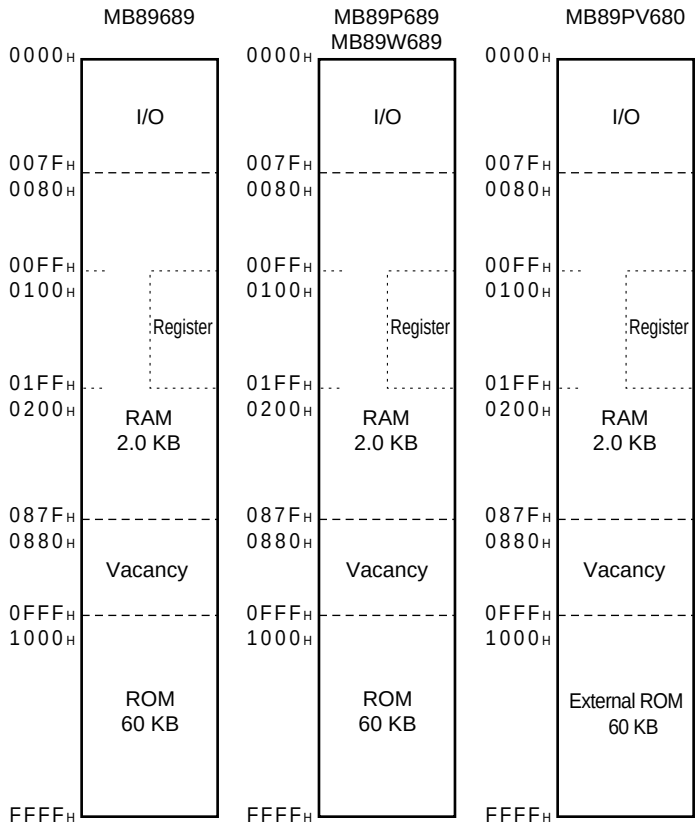


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89680 series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89680 series is structured as illustrated below.

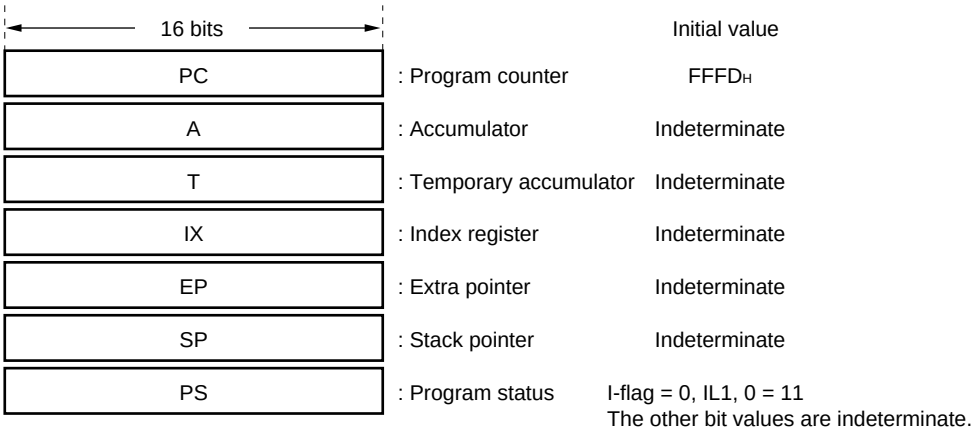
• **Memory space**



2. Registers

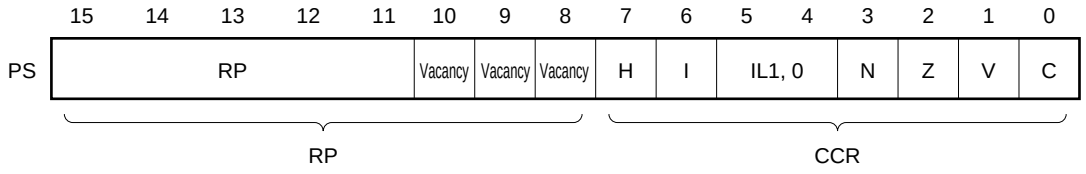
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- **Structure of the program status register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for conversion of actual addresses of the general-purpose register area**

										RP				Lower OP codes		
	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	R4	R3	R2	R1	R0	b2	b1	b0
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Generated addresses	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

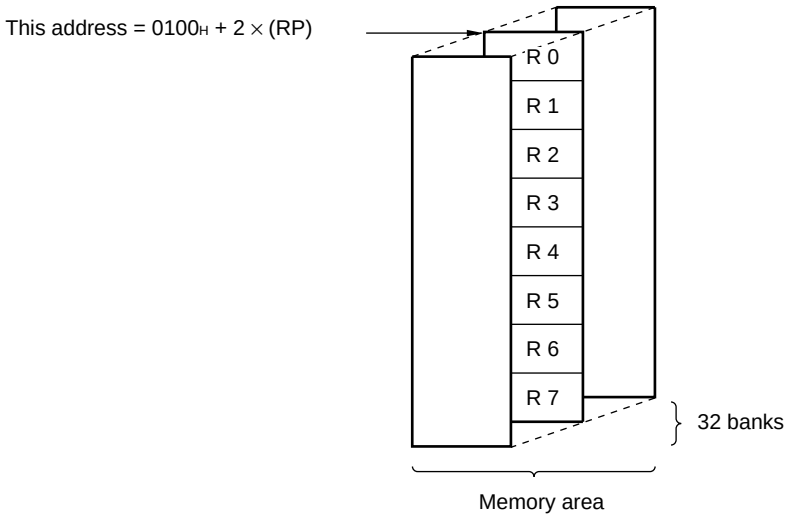
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used. The bank currently in use is indicated by the register bank pointer (RP).

- **Register bank configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(Vacancy)		
06H			
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	SMC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(R/W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(R/W)	BZCR	Buzzer register
10H	(R/W)	PDR5	Port 5 data register
11H	(Vacancy)		
12H	(R/W)	PDR6	Port 6 data register
13H	(R/W)	DDR6	Port 6 data direction register
14H	(R/W)	PDR7	Port 7 data register
15H	(Vacancy)		
16H	(R/W)	PDR8	Port 8 data register
17H	(Vacancy)		
18H	(R/W)	PDR9	Port 9 data register
19H	(R/W)	DDR9	Port 9 data direction register
1AH	(R/W)	PDRA	Port A data register
1BH	(R/W)	DDRA	Port A data direction register
1CH	(Vacancy)		
1DH			
1EH	(R/W)	CNTR	PWM control register
1FH	(W)	COMR	PWM compare register
20H	(Vacancy)		
21H			
22H	(R/W)	SBMR	Serial mode register with 1 byte buffer

(Continued)

(Continued)

Address	Read/write	Register name	Register description
23_H	(R/W)	SBFR	Serial flag register with 1 byte buffer
24_H	(W)	SBUFW	Serial buffer write register
	(R)	SBUFR	Serial buffer read register
25_H	(R)	SBDR	Serial data register with 1 byte buffer
26_H	(R/W)	T2CR	Timer 2 control register
27_H	(R/W)	T1CR	Timer 1 control register
28_H	(R/W)	T2DR	Timer 2 data register
29_H	(R/W)	T1DR	Timer 1 data register
$2A_H$	(R/W)	MODC	Modem output control register
$2B_H$	(R/W)	MODA	Modem output data register
$2C_H$	(Vacancy)		
$2D_H$	(R/W)	ADC1	A/D converter control 1 register
$2E_H$	(R/W)	ADC2	A/D converter control 2 register
$2F_H$	(R/W)	ADCD	A/D converter data register
30_H	(R/W)	EIE1	External interrupt 1 enable register
31_H	(R/W)	EIF1	External interrupt 1 flag register
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H	(R/W)	MDC1	Modem timer control 1 register
35_H	(R/W)	MDC2	Modem timer control 2 register
36_H	(R)	MLDH	Modem timer “H” level data register
37_H	(R)	MLDL	Modem timer “L” level data register
38_H	(R/W)	SMC	UART serial mode control register
39_H	(R/W)	SRC	UART serial rate control register
$3A_H$	(R/W)	SSD	UART serial status and data register
$3B_H$	(R)	SIDR	UART serial input data register
$3C_H$	(W)	SODR	UART serial output data register
$3D_H$	(R/W)	SSEL	Serial I/O port switching register
$3E_H$ to $7B_H$	(Vacancy)		
$7C_H$	(W)	ILR1	Interrupt level 1 setting register
$7D_H$	(W)	ILR2	Interrupt level 2 setting register
$7E_H$	(W)	ILR3	Interrupt level 3 setting register
$7F_H$	(Vacancy)		

Note: Do not use (vacancies).

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	Set V_{CC} = AV_{CC}*
	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed “AV_{CC} + 0.3 V”.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P4, P7, P8
	V_I	V_{SS} – 0.3	V_{SS} + 7.0	V	P4, P7, P8
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	20	mA	Peak value
“L” level average output current	I_{OLAV}	—	10	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	120	mA	Peak value
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	Peak value
“H” level average output current	I_{OHAV}	—	–10	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–60	mA	Peak value
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set to the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}, AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* (MB89689)
	V_{CC}, AV_{CC}	2.7*	6.0*	V	Normal operation assurance range* (MB89P689/W689/PV680)
	V_{CC}, AV_{CC}	1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : This values vary with the operating frequency. See Figure 1.

Figure 1 Operating Voltage vs. Main Clock Operating Frequency

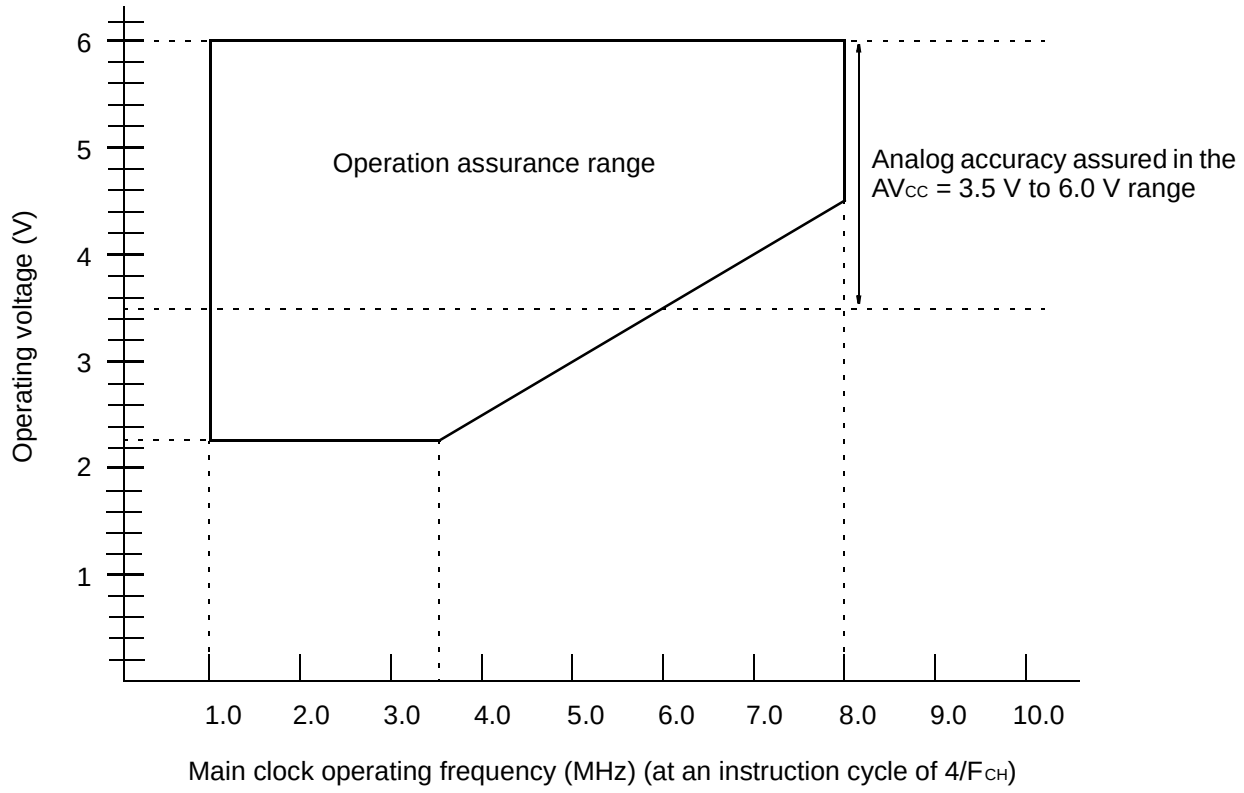


Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent of the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P0, P1	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	P3, P6, P9, PA, $\overline{RST}$, MOD0, MOD1, X0, X0A		0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS2}	P7		0.8 V_{CC}		V_{SS} + 7.0	V	
"L" level input voltage	V_{IL}	P0, P1		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P3, P6, P7, P9, PA, $\overline{RST}$, MOD0, MOD1, X0, X0A		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin applied voltage	V_D	P4, P7, P8		V_{SS} – 0.3	—	V_{SS} + 7.0	V	
		P5		V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P0 to P3, P6, P9, PA	I_{OH} = –2.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P0 to P4, P6 to P9, PA	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P0 to P9, PA, MOD0, MOD1	0.45 V < V_I < V_{CC}	—	—	±5	μA	
Power supply current	I_{CC}	V_{CC}	F_{CH} = 8 MHz V_{CC} = 5.0 V Main clock opration Highest gear speed	—	13	26	mA	
	I_{CCS1}	V_{CC}	F_{CH} = 8 MHz V_{CC} = 5.0 V Main sleep mode Highest gear speed	—	4	8	mA	
	I_{CCS2}	V_{CC}	F_{CH} = 32.768 kHz V_{CC} = 3.0 V Subclock sleep mode	—	25	50	μA	
	I_{CCH1}	V_{CC}	T_A = +25°C Subclock stop mode	—	—	1	μA	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CCH2}	V_{CC}	T_A = +85°C Subclock stop mode	—	1	10	µA	
	I_{CSB}	V_{CC}	F_{CL} = 32.768 kHz V_{CC} = 3.0 V Subclock operation	—	50	100	µA	
	I_{CCT}	V_{CC}	V_{CC} = 3.0 V Watch mode	—	—	15	µA	
	I_A	AV_{CC}	F_{CH} = 8 MHz	—	1.5	3.5	mA	When A/D conversion is activated
	I_{AH}	AV_{CC}		—	1	5	µA	When A/D conversion is stopped
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

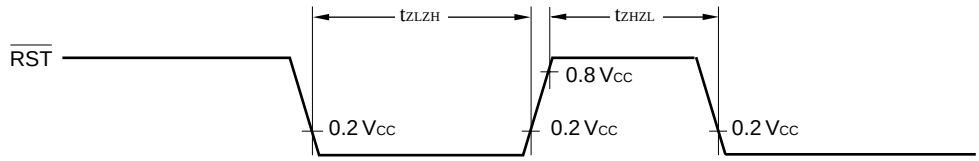
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}*	—	ns	
$\overline{RST}$ "H" pulse width	t_{ZHZL}		24 t_{XCYL}*	—	ns	

* : t_{XCYL} is the oscillation cycle input to the X0.

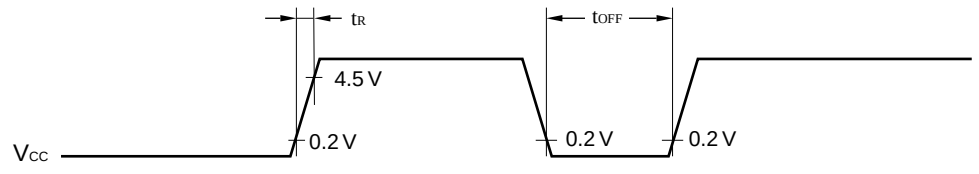


(2) Specifications for Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time selected.
For example, when the main clock is operating at F_{CH} = 8 MHz and the oscillation stabilization time is $2^{12}/F_{CH}$, the oscillation stabilization time is 0.5 ms. Therefore, the maximum value of power supply rising time is about 0.5 ms.
When increasing the supply voltage during operation, voltage variation should be within twice the intended increment so that the voltage rises as smoothly as possible.



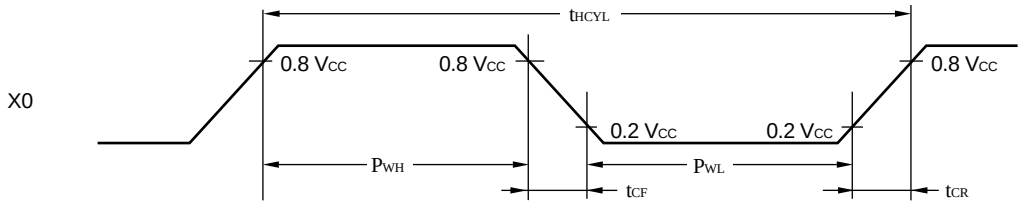
(3) Clock Timing

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

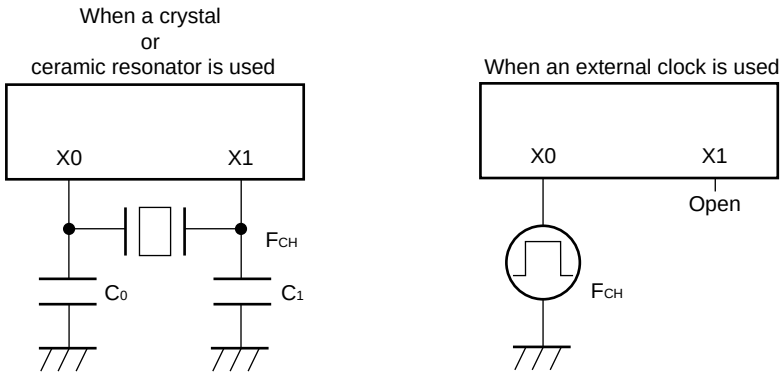
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input clock frequency	F_{CH}	X0, X1	—	1	—	8	MHz	Main clock
	F_{CL}	X0A, X1A		—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1		125	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	Subclock
Input clock duty rate	duty*1	X0		30	—	70	%	External clock
	duty1*2	X1		30	—	70	%	
Input clock rising/falling time	t_{CR1}	X0		—	—	24	ns	
	t_{CF1}	X0		—	—	24	ns	
	t_{CR2}	X0A		—	—	200	ns	
	t_{CF2}	X0A		—	—	200	ns	

*1: duty = P_{WH}/t_{HCYL}
*2: duty1= P_{WHL}/t_{HCYL}

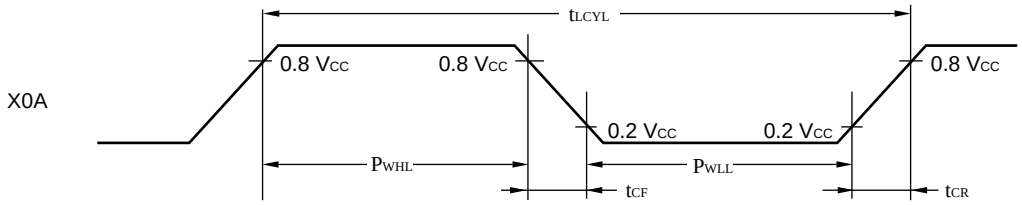
- **Main clock timing conditions**



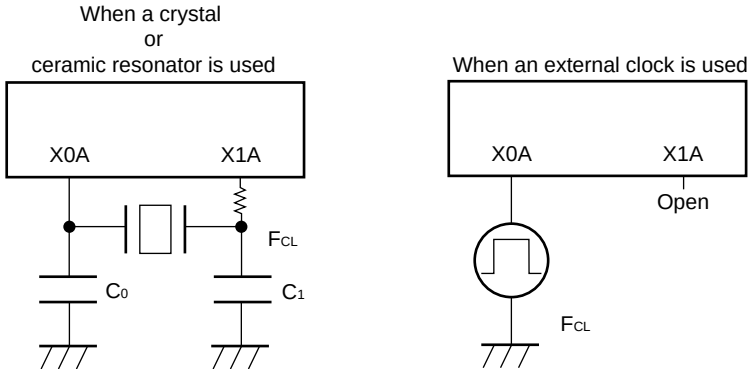
- **Main clock configurations**



• **Subclock timing conditions**



• **Subclock configurations**



(4) Instruction Cycle

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value (typical)	Unit	Remarks
Minimum execution time (instruction cycle)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	($4/F_{CH}$) t_{inst} = 0.5 µs when operating at F_{CH} = 8 MHz
	t_{inst}	$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

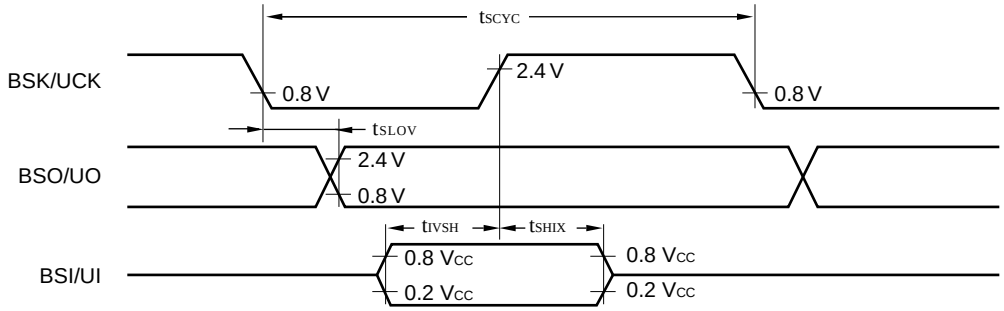
(5) Serial I/O Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

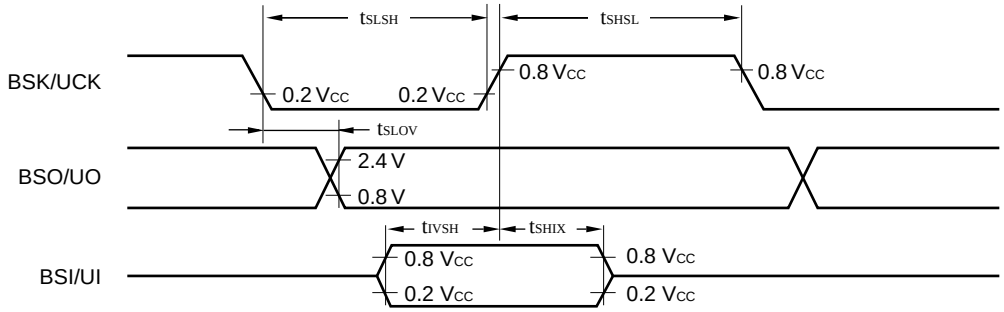
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	BSK/UCK	Internal shift clock mode	2 t_{inst}*	—	µs	
BSK/UCK ↓ → BSO/UO time	t_{SLOV}	BSK/UCK, BSO/UO		–200	200	ns	
Valid BSI/UI → BSK/UCK ↑	t_{IVSH}	BSI/UI, BSK/UCK		1/2 t_{inst}*	—	µs	
BSK/UCK ↑ → valid BSI/UI hold time	t_{SHIX}	BSK/UCK, BSI/UI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	BSK/UCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	BSK/UCK		1 t_{inst}*	—	µs	
BSK/UCK ↓ → BSO/UO time	t_{SLOV}	BSK/UCK, BSO/UO		0	200	ns	
Valid BSI/UI → BSK/UCK ↑	t_{IVSH}	BSI/UI, BSK/UCK		1/2 t_{inst}*	—	µs	
BSK/UCK ↑ → valid BSI/UI hold time	t_{SHIX}	BSK/UCK, BSI/UI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Internal shift clock mode**



• **External shift clock mode**

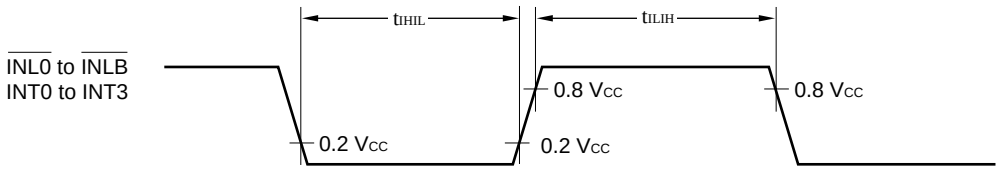


(6) Peripheral Input Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” level pulse width	t_{ILIH}	$\overline{INL0}$ to $\overline{INLB}$, INT0 to INT3	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width	t_{IHIL}	$\overline{INL20}$ to $\overline{INLB}$, INT0 to INT3	2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

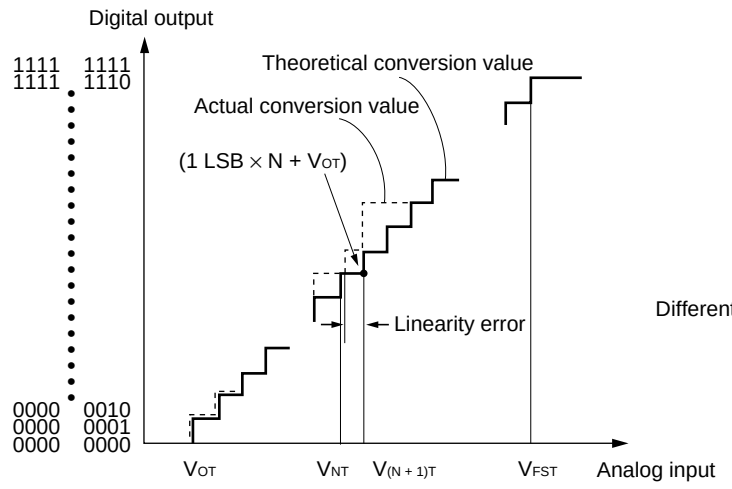
(AV_{CC} = V_{CC} = 3.5 V to 6.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	AVR = AV_{CC} = 5.0 V	—	—	8	bit	
Total error	—	—	AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error	—	—		—	—	±1.0	LSB	
Differential linearity error	—	—		—	—	±0.9	LSB	
Zero transition voltage	V_{0T}	—		AVss –1.0 LSB	AVss +0.5 LSB	AVss +2.0 LSB	mV	1 LSB = AVR/256
Full-scale transition voltage	V_{FST}	—		AVR –3.0 LSB	AVR –1.5 LSB	AVR	mV	
Interchannel disparity	—	—		—	—	0.5	LSB	
A/D mode conversion time	—	—	—	—	44	—	t_{inst}*	
Sense mode conversion time	—	—		—	12	—	t_{inst}*	
Analog port input current	I_{AIN}	AN00 to AN07		—	—	10	µA	
Analog input voltage	—	AN00 to AN07		0.0	—	AVR	V	
Reference voltage	—	AVR		0.0	—	AV_{CC}	V	
Reference voltage supply current	I_R	AVR	AVR = AV_{CC} = 5.0 V	—	100	300	µA	
	I_{RH}	AVR		—	—	1	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable by the A/D converter
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

7. Notes on Using A/D Converter

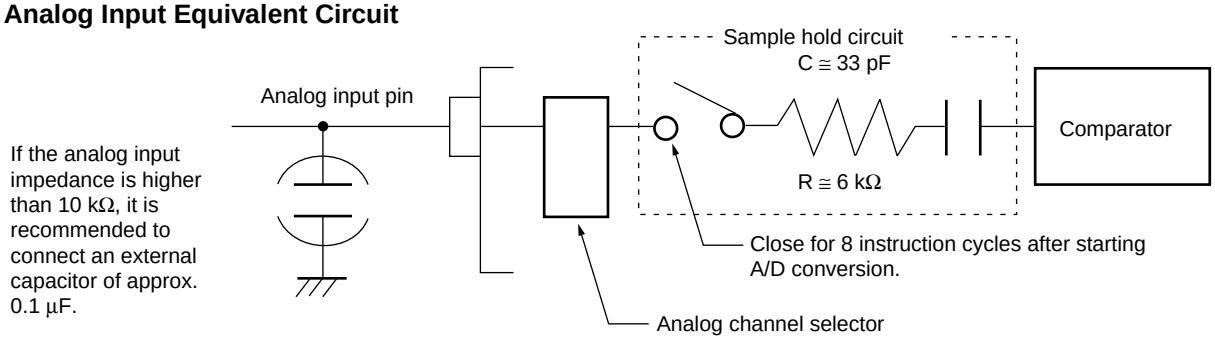
- **Input impedance of the analog input pins**

  The A/D converter used for the MB89890 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after starting A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of approx. 0.1 μF for the analog input pin.

- **Analog Input Equivalent Circuit**



- **Error**

  The smaller the | AVR – AV_{SS} |, the greater the error would become relatively.

■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –

Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

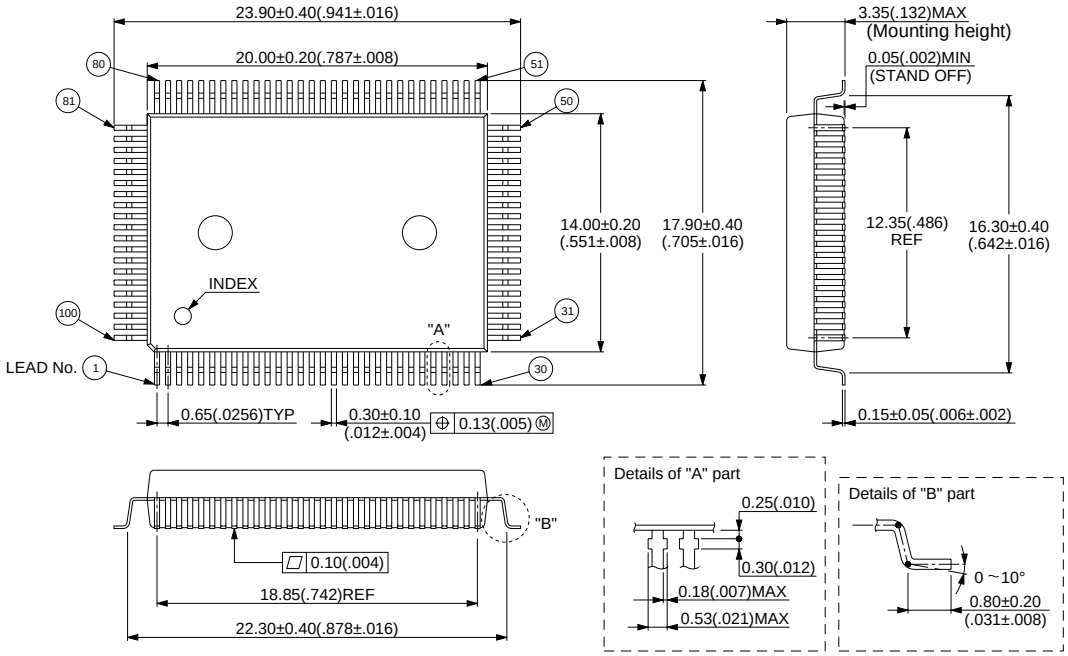
No.	Part number	MB89689	MB89P689 MB89W689	MB89PV680
	Specifying procedure	Spcify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P60 to P67, P90 to P97, PA0 to PA7	Selectable by pin	Selectable by pin	Fixed to without a pull-up resistor
2	Power-on reset (POR) With power-on reset Without power-on reset	Selectable	Selectable	Fixed to with power-on reset
3	Oscillation stabilization time selection (OSC) The initial value of the main clock oscillation stabilization time can be set with WTM1 and WTM0 bit.	Selectable WTM1 WTM0 0 0: $2^3/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Selectable WTM1 WTM0 0 0: $2^3/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{18}/F_{CH}$
4	Reset pin output (RST) With reset output Without reset output	Selectable	Selectable	Fixed to with reset output
5	Clock mode selection (CLK) Dual-clock mode Single-clock mode	Selectable	Selectable	Fixed to dual clock

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89689PF MB89P689PF	100-pin Plastic QFP (FPT-100P-M06)	
MB89W689CF	100-pin Ceramic QFP (FPT-100C-A02)	
MB89PV680CF	100-pin Ceramic MQFP (MQP-100C-P01)	

■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)



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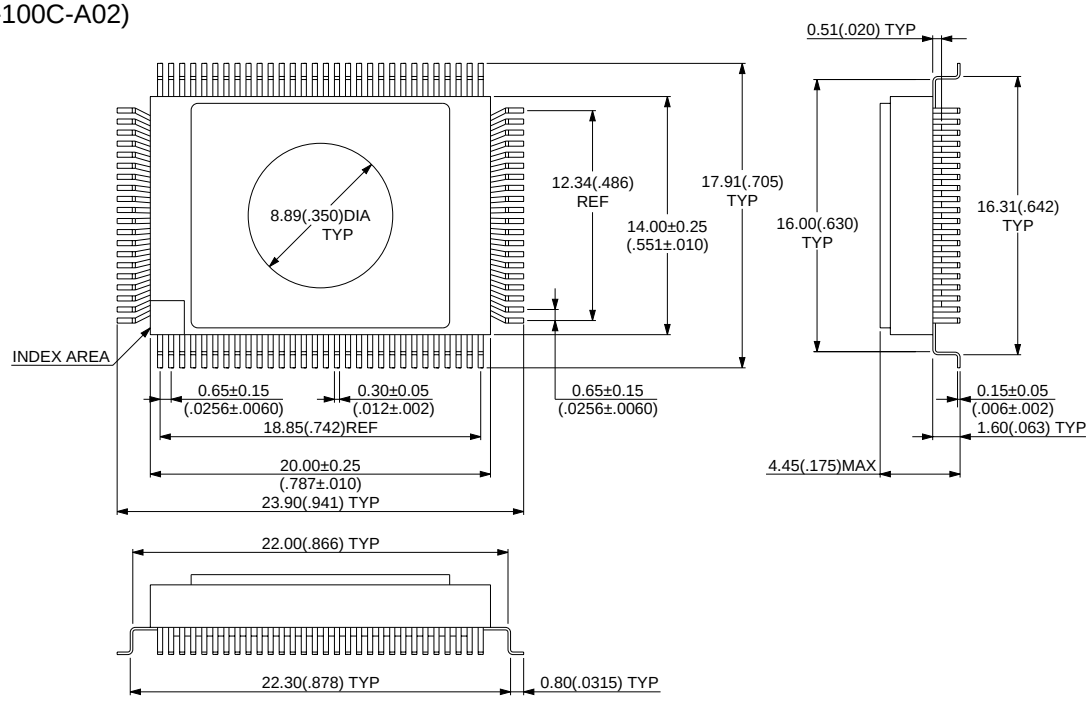
Dimensions in mm (inches)

100-pin Ceramic QFP
(FPT-100C-A02)



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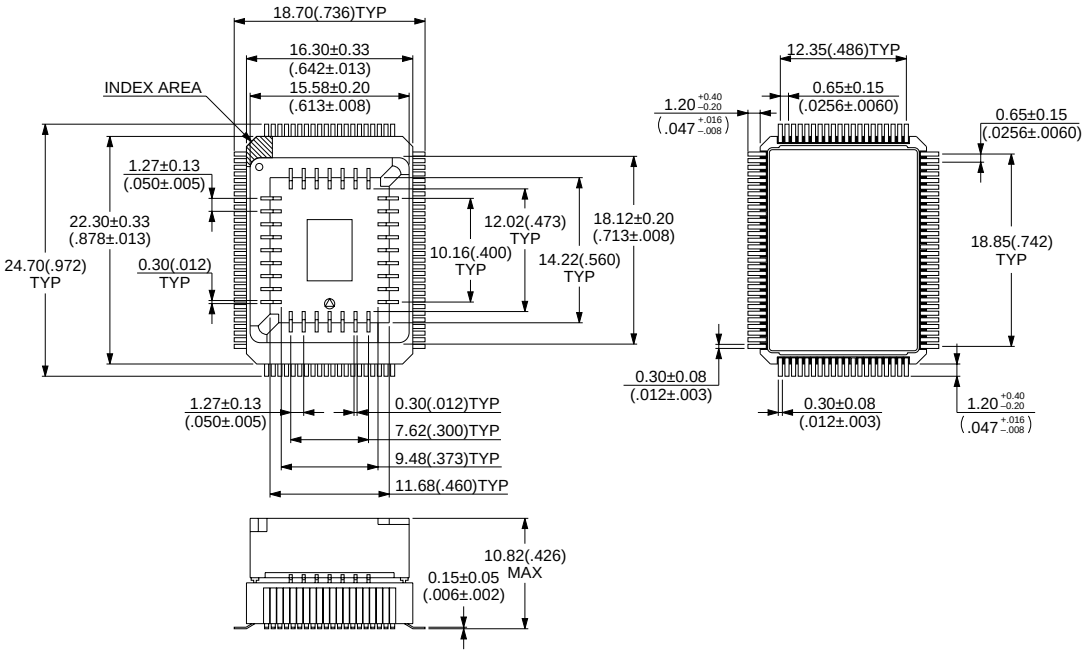
Dimensions in mm (inches)

100-pin Ceramic MQFP
(MQP-100C-P01)



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Dimensions in mm (inches)

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