



**CS4340A**

## 24-Bit, 192 kHz Stereo DAC for Audio

### Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.3 V or +5 V Power Supply
- 50 mW with 3.3 V supply
- Low Clock Jitter Sensitivity
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis for 44.1kHz
- Popguard® Technology for Control of Clicks and Pops
- Up to 200 kHz Sample Rates
- Automatic Mode Detection for Sample Rates between 4 and 200 kHz
- Pin Compatible with the CS4340

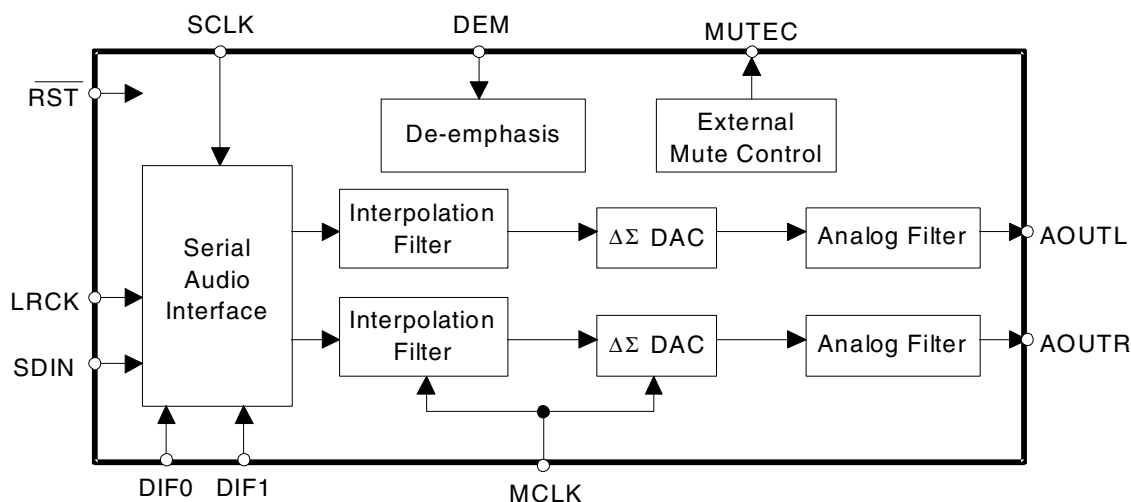
### Description

The CS4340A is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, and a high tolerance to clock jitter.

The CS4340A accepts data at all standard audio sample rates up to 192 kHz, consumes very little power, operates over a wide power supply range and is pin compatible with the CS4340, as described in section 3.1. These features are ideal for DVD audio players.

### ORDERING INFORMATION

|            |                           |
|------------|---------------------------|
| CS4340A-KS | 16-pin SOIC, -10 to 70 °C |
| CDB4340A   | Evaluation Board          |



**Preliminary Product Information**

This document contains information for a new product.  
Cirrus Logic reserves the right to modify this product without notice.

**TABLE OF CONTENTS**

|                                                                  |           |
|------------------------------------------------------------------|-----------|
| <b>1. PIN DESCRIPTION .....</b>                                  | <b>4</b>  |
| <b>2. TYPICAL CONNECTION DIAGRAM .....</b>                       | <b>5</b>  |
| <b>3. APPLICATIONS .....</b>                                     | <b>6</b>  |
| 3.1 Upgrading from the CS4340 to the CS4340A .....               | 6         |
| 3.2 Sample Rate Range/Operational Mode Detect .....              | 6         |
| 3.3 System Clocking .....                                        | 6         |
| 3.4 Digital Interface Format .....                               | 7         |
| 3.5 De-Emphasis .....                                            | 8         |
| 3.6 Power-up Sequence .....                                      | 9         |
| 3.7 Popguard® Transient Control .....                            | 9         |
| 3.7.1 Power-up .....                                             | 9         |
| 3.7.2 Power-down .....                                           | 9         |
| 3.7.3 Discharge Time .....                                       | 9         |
| 3.8 Mute Control .....                                           | 10        |
| 3.9 Grounding and Power Supply Arrangements .....                | 10        |
| <b>4. CHARACTERISTICS AND SPECIFICATIONS .....</b>               | <b>11</b> |
| ANALOG CHARACTERISTICS (CS4340A-KS) .....                        | 11        |
| COMBINED INTERPOLATION<br>& ON-CHIP ANALOG FILTER RESPONSE ..... | 13        |
| SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE .....          | 16        |
| DC ELECTRICAL CHARACTERISTICS .....                              | 17        |
| DIGITAL INTERFACE SPECIFICATIONS .....                           | 17        |
| DIGITAL INPUT CHARACTERISTICS .....                              | 17        |
| THERMAL CHARACTERISTICS AND SPECIFICATIONS .....                 | 17        |
| RECOMMENDED OPERATING SPECIFICATION .....                        | 18        |
| ABSOLUTE MAXIMUM RATINGS .....                                   | 18        |
| <b>5. PARAMETER DEFINITIONS .....</b>                            | <b>19</b> |
| <b>6. REFERENCES .....</b>                                       | <b>19</b> |
| <b>7. PACKAGE DIMENSIONS .....</b>                               | <b>20</b> |

---

**Contacting Cirrus Logic Support**

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find one nearest you go to <http://www.cirrus.com/corporate/contacts/sales.cfm>

**IMPORTANT NOTICE**

"Preliminary" product information describes products that are in production, but for which full characterization data is not yet available. "Advance" product information describes products that are in development and subject to development changes. Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights of the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other parts of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan. An export license and/or quota needs to be obtained from the competent authorities of the Chinese Government if any of the products or technologies described in this material is subject to the PRC Foreign Trade Law and is to be exported or taken out of the PRC.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

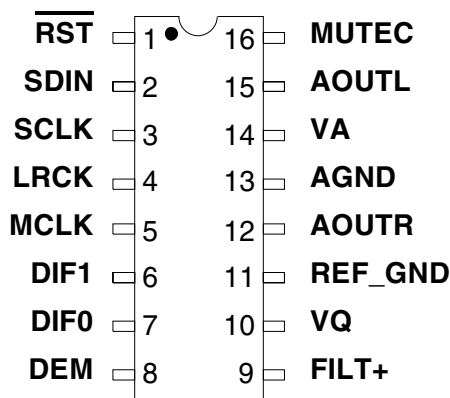
## LIST OF FIGURES

|                                                                       |    |
|-----------------------------------------------------------------------|----|
| Figure 1. Typical Connection Diagram .....                            | 5  |
| Figure 2. CS4340A Format 0 - I <sup>2</sup> S up to 24-Bit Data ..... | 7  |
| Figure 3. CS4340A Format 1 - Left Justified up to 24-Bit Data .....   | 8  |
| Figure 4. CS4340A Format 2 - Right Justified, 24-Bit Data .....       | 8  |
| Figure 5. CS4340A Format 3 - Right Justified, 16-Bit Data .....       | 8  |
| Figure 6. De-Emphasis Curve .....                                     | 8  |
| Figure 7. Output Test Load .....                                      | 12 |
| Figure 8. Maximum Loading .....                                       | 12 |
| Figure 9. Single-Speed Stopband Rejection .....                       | 14 |
| Figure 10. Single-Speed Transition Band .....                         | 14 |
| Figure 11. Single-Speed Transition Band (Detail) .....                | 14 |
| Figure 12. Single-Speed Passband Ripple .....                         | 14 |
| Figure 13. Double-Speed Stopband Rejection .....                      | 14 |
| Figure 14. Double-Speed Transition Band .....                         | 14 |
| Figure 15. Double-Speed Transition Band (Detail) .....                | 15 |
| Figure 16. Double-Speed Passband Ripple .....                         | 15 |
| Figure 17. Serial Input Timing .....                                  | 16 |

## LIST OF TABLES

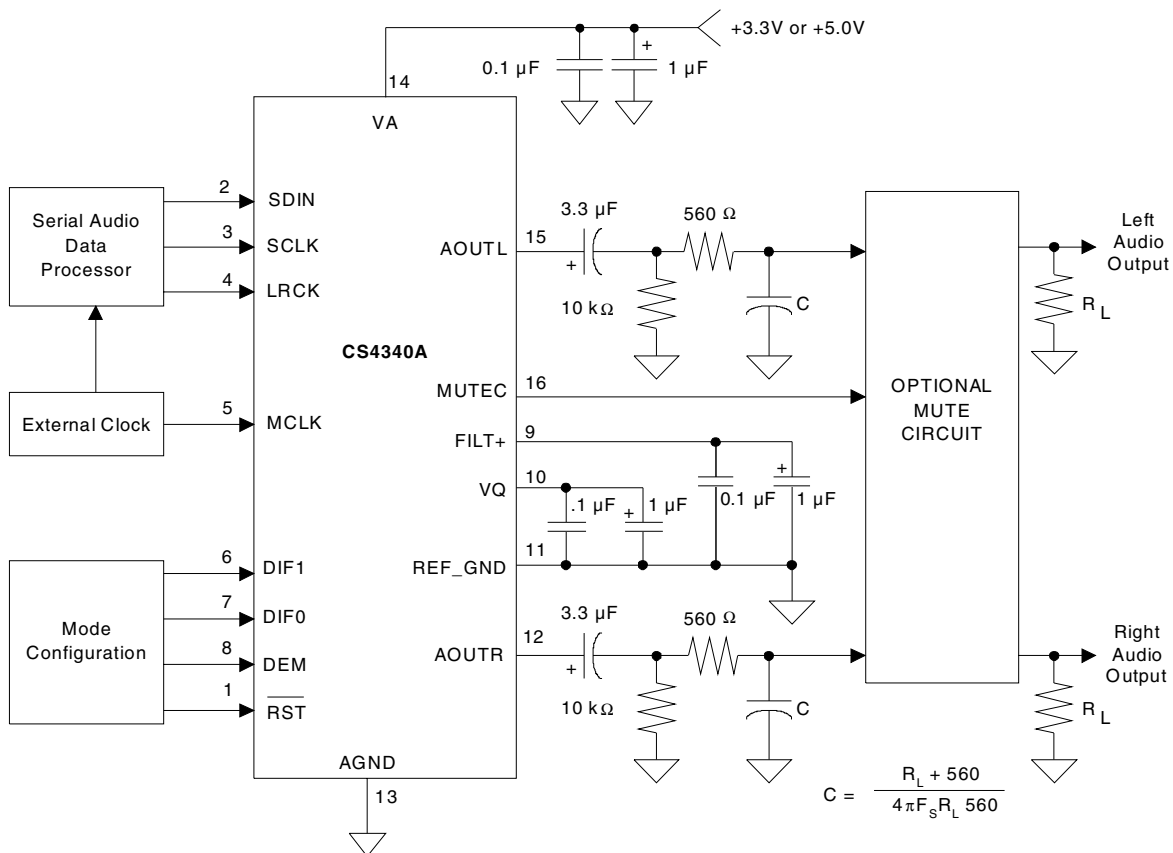
|                                                         |   |
|---------------------------------------------------------|---|
| Table 1. CS4340A Auto-Detect .....                      | 6 |
| Table 2. Single-Speed Mode Standard Frequencies .....   | 7 |
| Table 3. Double-Speed Mode Standard Frequencies .....   | 7 |
| Table 4. Quad-Speed Mode Standard Frequencies .....     | 7 |
| Table 5. Digital Interface Format - DIF1 and DIF0 ..... | 7 |
| Table 6. De-Emphasis Control .....                      | 8 |

## 1. PIN DESCRIPTION



| Pin Name       | #  | Pin Description                                                                                                                               |
|----------------|----|-----------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RST</b>     | 1  | <b>Reset (Input)</b> - Powers down device.                                                                                                    |
| <b>SDIN</b>    | 2  | <b>Serial Audio Data (Input)</b> - Input for two's complement serial audio data.                                                              |
| <b>SCLK</b>    | 3  | <b>Serial Clock (Input)</b> - Serial clock for the serial audio interface.                                                                    |
| <b>LRCK</b>    | 4  | <b>Left Right Clock (Input)</b> - Determines which channel, Left or Right, is currently active on the serial audio data line.                 |
| <b>MCLK</b>    | 5  | <b>Master Clock (Input)</b> - Clock source for the delta-sigma modulator and digital filters.                                                 |
| <b>DIF1</b>    | 6  | <b>Digital Interface Format (Input)</b> - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data. |
| <b>DIF0</b>    | 7  |                                                                                                                                               |
| <b>DEM</b>     | 8  | <b>De-emphasis Control (Input)</b> - Selects the standard 15µs/50µs digital de-emphasis filter response for the 44.1 kHz sample rate.         |
| <b>FILT+</b>   | 9  | <b>Positive Voltage Reference (Output)</b> - Positive voltage reference for the internal sampling circuits.                                   |
| <b>VQ</b>      | 10 | <b>Quiescent Voltage (Output)</b> - Filter connection for internal quiescent reference voltage.                                               |
| <b>REF_GND</b> | 11 | <b>Reference Ground (Input)</b> - Ground reference for the internal sampling circuits.                                                        |
| <b>AOUTR</b>   | 12 | <b>Analog Outputs (Output)</b> - The full scale analog output level is specified in the <i>Analog Characteristics</i> table.                  |
| <b>AOUTL</b>   | 15 |                                                                                                                                               |
| <b>AGND</b>    | 13 | <b>Analog Ground (Input)</b>                                                                                                                  |
| <b>VA</b>      | 14 | <b>Power (Input)</b> - Positive power for the analog, digital and serial audio interface sections.                                            |
| <b>MUTE</b>    | 16 | <b>Mute Control (Output)</b> - Control signal for an optional mute circuit.                                                                   |

## 2. TYPICAL CONNECTION DIAGRAM



**Figure 1. Typical Connection Diagram**

### 3. APPLICATIONS

#### 3.1 Upgrading from the CS4340 to the CS4340A

The CS4340A is pin and functionally compatible with all CS4340 designs, operating at the standard audio sample rates, that use pin 3 as a serial clock input. In addition to the features of the CS4340, the CS4340A supports standard sample rates up to 192 kHz, as well as automatic mode detection for sample rates between 4 and 200 kHz. The automatic mode detection feature allows sample rate changes between single, double and quad-speed modes without external intervention.

The CS4340A does not support an internal serial clock mode, sample rates between 50 kHz and 84 kHz or de-emphasis for 32 and 48 kHz, as does the CS4340.

#### 3.2 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. It will auto-detect the correct mode when the input sample rate ( $F_s$ ), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 1. Sample rates outside the specified range for each mode are not supported.

| Input Sample Rate ( $F_s$ ) | MODE              |
|-----------------------------|-------------------|
| 4 kHz - 50 kHz              | Single-Speed Mode |
| 84 kHz - 100 kHz            | Double-Speed Mode |
| 170 kHz - 200 kHz           | Quad-Speed Mode   |

**Table 1. CS4340A Auto-Detect**

#### 3.3 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The LRCK, defined also as the input sample rate ( $F_s$ ), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2-4.

| Sample Rate<br>(kHz) | MCLK (MHz) |         |         |         |
|----------------------|------------|---------|---------|---------|
|                      | 256x       | 384x    | 512x    | 768x    |
| 32                   | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 44.1                 | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 48                   | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

**Table 2. Single-Speed Mode Standard Frequencies**

| Sample Rate<br>(kHz) | MCLK (MHz) |         |         |         |
|----------------------|------------|---------|---------|---------|
|                      | 128x       | 192x    | 256x    | 384x    |
| 88.2                 | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 96                   | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

**Table 3. Double-Speed Mode Standard Frequencies**

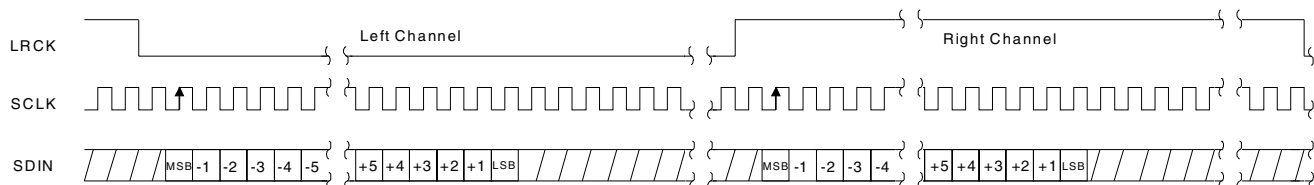
| Sample Rate<br>(kHz) | MCLK (MHz) |         |
|----------------------|------------|---------|
|                      | 128x       | 192x    |
| 176.4                | 22.5792    | 33.8688 |
| 192                  | 24.5760    | 36.8640 |

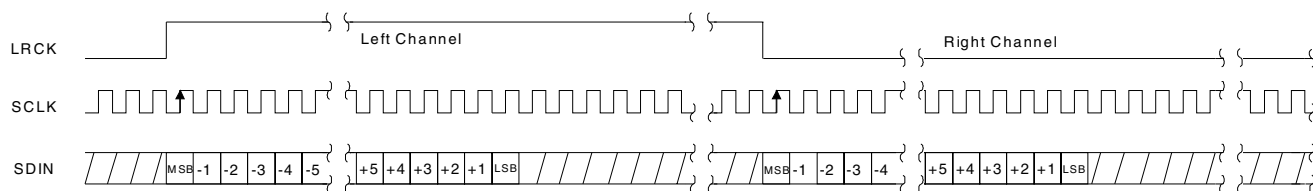
**Table 4. Quad-Speed Mode Standard Frequencies**

### 3.4 Digital Interface Format

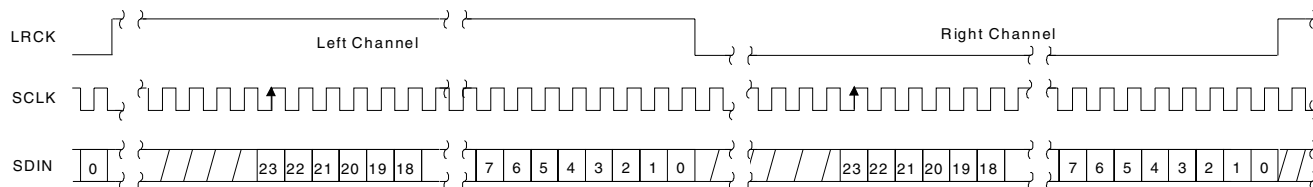
The device will accept audio samples in several digital interface formats as illustrated in Table 5. The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 2-5.

| DIF1 | DIF0 | DESCRIPTION                         | FORMAT | FIGURE |
|------|------|-------------------------------------|--------|--------|
| 0    | 0    | I <sup>2</sup> S, up to 24-bit data | 0      | 2      |
| 0    | 1    | Left Justified, up to 24-bit data   | 1      | 3      |
| 1    | 0    | Right Justified, 24-bit Data        | 2      | 4      |
| 1    | 1    | Right Justified, 16-bit Data        | 3      | 5      |

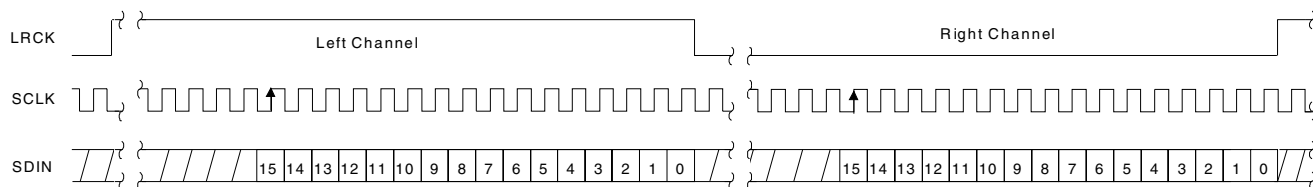
**Table 5. Digital Interface Format - DIF1 and DIF0**

**Figure 2. CS4340A Format 0 - I<sup>2</sup>S up to 24-Bit Data**



**Figure 3. CS4340A Format 1 - Left Justified up to 24-Bit Data**



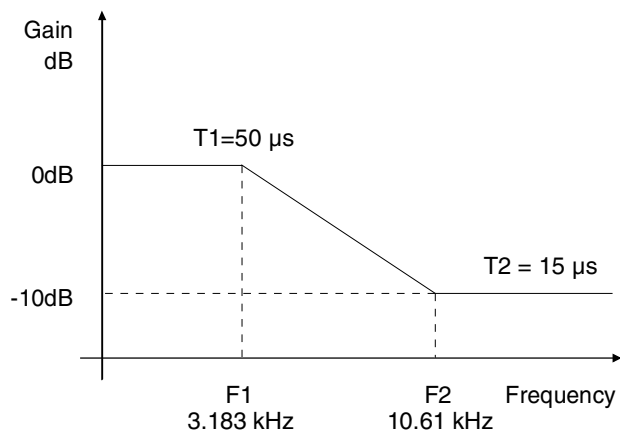
**Figure 4. CS4340A Format 2 - Right Justified, 24-Bit Data**



**Figure 5. CS4340A Format 3 - Right Justified, 16-Bit Data**

### 3.5 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 6 shows the de-emphasis curve for  $F_s$  equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate,  $F_s$ . Please see Table 6 for the desired de-emphasis control.



**Figure 6. De-Emphasis Curve**

| DEM | DESCRIPTION |
|-----|-------------|
| 0   | Disabled    |
| 1   | 44.1 kHz    |

**Table 6. De-Emphasis Control**

### 3.6 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supply and configuration pins are stable, and the clocks are locked to the appropriate frequencies discussed in section 3.3. It is also recommended that reset be enabled if the analog supply drops below the minimum specified operating voltage to prevent power glitch related issues.

### 3.7 Popguard® Transient Control

The CS4340A uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when  $\overline{\text{RST}}$  is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

#### 3.7.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach  $V_Q$  and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

#### 3.7.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by enabling  $\overline{\text{RST}}$ . When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

#### 3.7.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3  $\mu\text{F}$  capacitor, the minimum power-down time will be approximately 0.4 seconds.

### 3.8 Mute Control

The Mute Control pin goes high during power-up initialization, reset, or if the MCLK to LRCK ratio is incorrect. The pin will also go high following the reception of 8192 consecutive audio samples of static 0 or -1 on both the left and right channels. A single sample of non-zero data on either channel will cause the Mute Control pin to go low. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4340A data sheet for a suggested mute circuit.

### 3.9 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4340A requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF\_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1  $\mu$ F, must be positioned to minimize the electrical path from FILT+ and REF\_GND (as well as VQ and REF\_GND), and should also be located on the same layer as the DAC. The CDB4340A evaluation board demonstrates the optimum layout and power supply arrangements.

**4. CHARACTERISTICS AND SPECIFICATIONS** Typical performance characteristics are derived from measurements taken at  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_A = 3.3\text{ V}$  and  $V_A = 5.0\text{ V}$ . Min/Max performance characteristics are guaranteed over the specified operating temperature and voltages.)

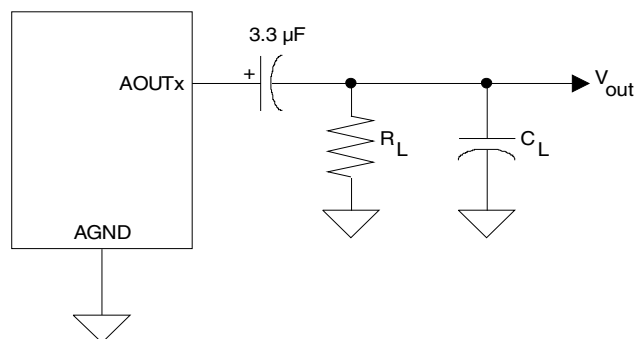
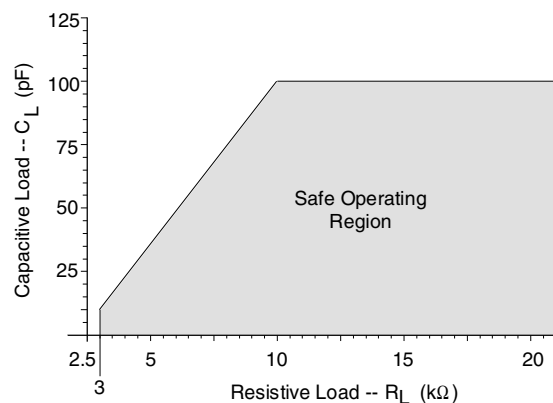
**ANALOG CHARACTERISTICS (CS4340A-KS)** (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; test load  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$  (see Figure 7).)

| Parameter                     |                                   | VA = 5.0V   |     |     | VA = 3.3V |     |     | Unit |
|-------------------------------|-----------------------------------|-------------|-----|-----|-----------|-----|-----|------|
|                               |                                   | Min         | Typ | Max | Min       | Typ | Max |      |
| Single-Speed Mode             |                                   | Fs = 48kHz  |     |     |           |     |     |      |
| Dynamic Range<br>18 to 24-Bit | (Note 1)                          |             |     |     |           |     |     |      |
|                               | unweighted                        | 92          | 98  | -   | 88        | 94  | -   | dB   |
|                               | A-Weighted                        | 95          | 101 | -   | 91        | 97  | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| unweighted                    |                                   | -           | 92  | -   | -         | 92  | -   | dB   |
|                               | A-Weighted                        | -           | 95  | -   | -         | 95  | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |
|                               | Total Harmonic Distortion + Noise | (Note 1)    |     |     |           |     |     |      |
| 18 to 24-Bit                  | 0 dB                              | -           | -91 | -85 | -         | -94 | -88 | dB   |
|                               | -20 dB                            | -           | -78 | -   | -         | -74 | -   | dB   |
|                               | -60 dB                            | -           | -38 | -   | -         | -34 | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| 0 dB                          |                                   | -           | -90 | -   | -         | -91 | -   | dB   |
|                               | -20 dB                            | -           | -72 | -   | -         | -72 | -   | dB   |
|                               | -60 dB                            | -           | -32 | -   | -         | -32 | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |
| Double-Speed Mode             |                                   | Fs = 96kHz  |     |     |           |     |     |      |
| Dynamic Range<br>18 to 24-Bit | (Note 1)                          |             |     |     |           |     |     |      |
|                               | unweighted                        | 92          | 98  | -   | 88        | 94  | -   | dB   |
|                               | A-Weighted                        | 95          | 101 | -   | 91        | 97  | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| unweighted                    |                                   | -           | 92  | -   | -         | 92  | -   | dB   |
|                               | A-Weighted                        | -           | 95  | -   | -         | 95  | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |
|                               | Total Harmonic Distortion + Noise | (Note 1)    |     |     |           |     |     |      |
| 18 to 24-Bit                  | 0 dB                              | -           | -91 | -85 | -         | -94 | -88 | dB   |
|                               | -20 dB                            | -           | -78 | -   | -         | -74 | -   | dB   |
|                               | -60 dB                            | -           | -38 | -   | -         | -34 | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| 0 dB                          |                                   | -           | -90 | -   | -         | -91 | -   | dB   |
|                               | -20 dB                            | -           | -72 | -   | -         | -72 | -   | dB   |
|                               | -60 dB                            | -           | -32 | -   | -         | -32 | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |
| Quad-Speed Mode               |                                   | Fs = 192kHz |     |     |           |     |     |      |
| Dynamic Range<br>18 to 24-Bit | (Note 1)                          |             |     |     |           |     |     |      |
|                               | unweighted                        | 92          | 98  | -   | 88        | 94  | -   | dB   |
|                               | A-Weighted                        | 95          | 101 | -   | 91        | 97  | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| unweighted                    |                                   | -           | 92  | -   | -         | 92  | -   | dB   |
|                               | A-Weighted                        | -           | 95  | -   | -         | 95  | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |
|                               | Total Harmonic Distortion + Noise | (Note 1)    |     |     |           |     |     |      |
| 18 to 24-Bit                  | 0 dB                              | -           | -91 | -85 | -         | -94 | -88 | dB   |
|                               | -20 dB                            | -           | -78 | -   | -         | -74 | -   | dB   |
|                               | -60 dB                            | -           | -38 | -   | -         | -34 | -   | dB   |
|                               | 16-Bit                            |             |     |     |           |     |     |      |
| 0 dB                          |                                   | -           | -90 | -   | -         | -91 | -   | dB   |
|                               | -20 dB                            | -           | -72 | -   | -         | -72 | -   | dB   |
|                               | -60 dB                            | -           | -32 | -   | -         | -32 | -   | dB   |
|                               |                                   |             |     |     |           |     |     |      |

**ANALOG CHARACTERISTICS (CS4340A-KS) (Continued)**

| Parameters                                              | Symbol         | Min    | Typ    | Max    | Units           |
|---------------------------------------------------------|----------------|--------|--------|--------|-----------------|
| <b>Dynamic Performance for All Modes</b>                |                |        |        |        |                 |
| Interchannel Isolation (1 kHz)                          |                | -      | 102    | -      | dB              |
| <b>DC Accuracy</b>                                      |                |        |        |        |                 |
| Interchannel Gain Mismatch                              |                | -      | 0.1    | -      | dB              |
| Gain Drift                                              |                | -      | ±100   | -      | ppm/°C          |
| <b>Analog Output Characteristics and Specifications</b> |                |        |        |        |                 |
| Full Scale Output Voltage                               |                | 0.6•VA | 0.7•VA | 0.8•VA | V <sub>pp</sub> |
| Output Impedance                                        |                | -      | 100    | -      | Ω               |
| Minimum AC-Load Resistance (Note 2)                     | R <sub>L</sub> | -      | 3      | -      | kΩ              |
| Maximum Load Capacitance (Note 2)                       | C <sub>L</sub> | -      | 100    | -      | pF              |

Notes: 1. One-half LSB of triangular PDF dither is added to data.  
2. Refer to Figure 8.

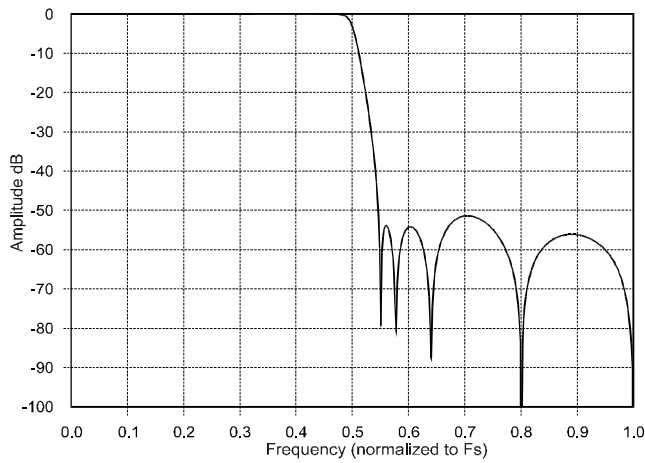

**Figure 7. Output Test Load**

**Figure 8. Maximum Loading**

## COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

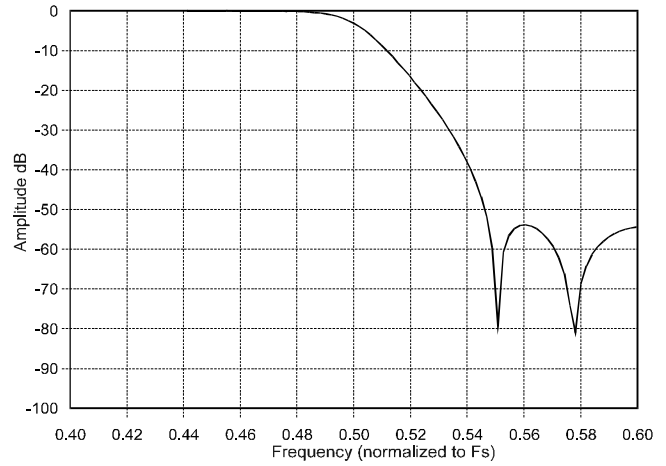
| Parameter                                                    | Min    | Typ      | Max         | Unit |
|--------------------------------------------------------------|--------|----------|-------------|------|
| <b>Single-Speed Mode - (4 kHz to 50 kHz sample rates)</b>    |        |          |             |      |
| Passband                                                     |        |          |             |      |
| to -0.05 dB corner                                           | 0      | -        | 0.4535      | Fs   |
| to -3 dB corner                                              | 0      | -        | 0.4998      | Fs   |
| Frequency Response 10 Hz to 20 kHz                           | -0.02  | -        | +0.08       | dB   |
| StopBand                                                     | 0.5465 | -        | -           | Fs   |
| StopBand Attenuation (Note 3)                                | 50     | -        | -           | dB   |
| Group Delay                                                  | -      | 9/Fs     | -           | s    |
| Passband Group Delay Deviation 0 - 20 kHz                    | -      | ±0.36/Fs | -           | s    |
| De-emphasis Error (Relative to 1 kHz) (Note 4) Fs = 44.1 kHz | -      | -        | +0.05/-0.14 | dB   |
| <b>Double-Speed Mode - (84 kHz to 100 kHz sample rates)</b>  |        |          |             |      |
| Passband                                                     |        |          |             |      |
| to -0.1 dB corner                                            | 0      | -        | 0.4621      | Fs   |
| to -3 dB corner                                              | 0      | -        | 0.4982      | Fs   |
| Frequency Response 10 Hz to 20 kHz                           | -0.06  | -        | +0.2        | dB   |
| StopBand                                                     | 0.577  | -        | -           | Fs   |
| StopBand Attenuation (Note 3)                                | 55     | -        | -           | dB   |
| Group Delay                                                  | -      | 4/Fs     | -           | s    |
| Passband Group Delay Deviation 0 - 40 kHz                    | -      | ±1.39/Fs | -           | s    |
| 0 - 20 kHz                                                   | -      | ±0.23/Fs | -           | s    |
| <b>Quad-Speed Mode - (170 kHz to 200 kHz sample rates)</b>   |        |          |             |      |
| Frequency Response 10 Hz to 20 kHz                           | -1     | -        | 0           | dB   |
| Group Delay                                                  | -      | 3/Fs     | -           | s    |

Notes: 3. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.  
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

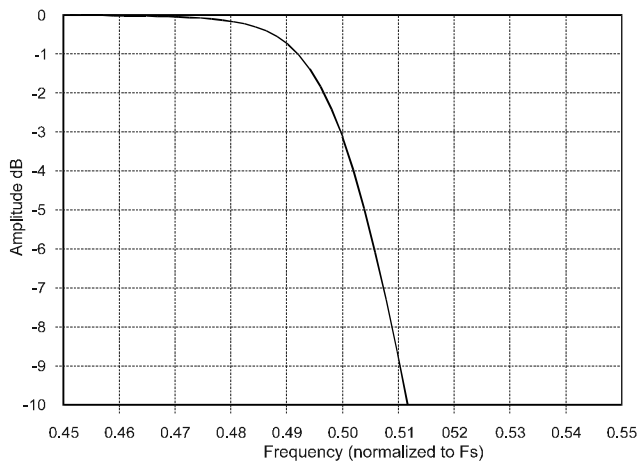
4. De-emphasis is only available in Single-Speed Mode.



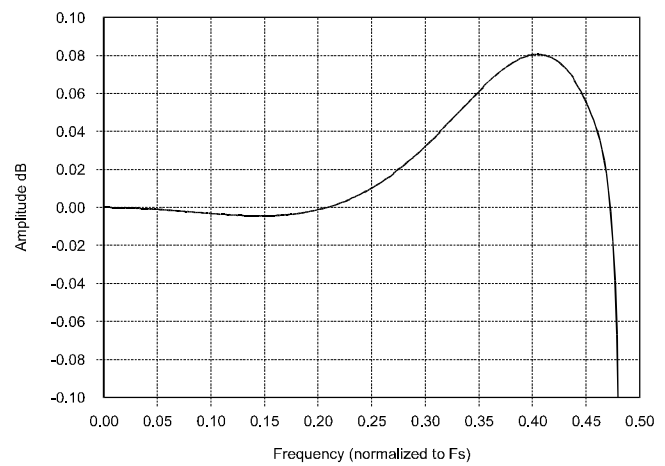
**Figure 9. Single-Speed Stopband Rejection**



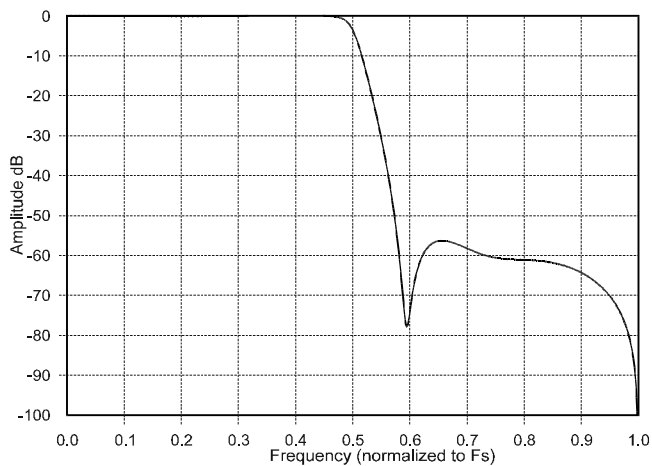
**Figure 10. Single-Speed Transition Band**



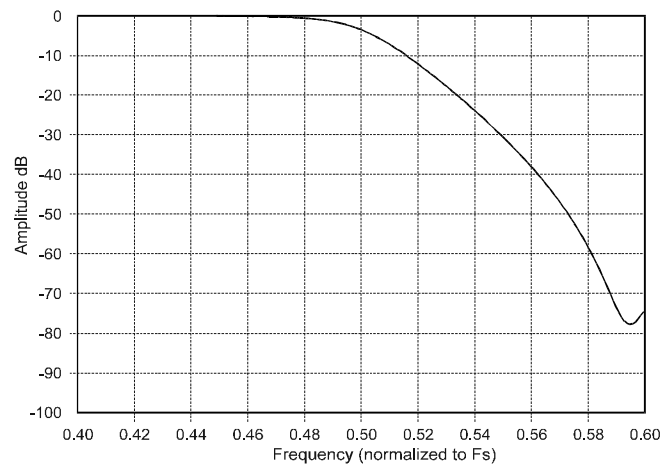
**Figure 11. Single-Speed Transition Band (Detail)**



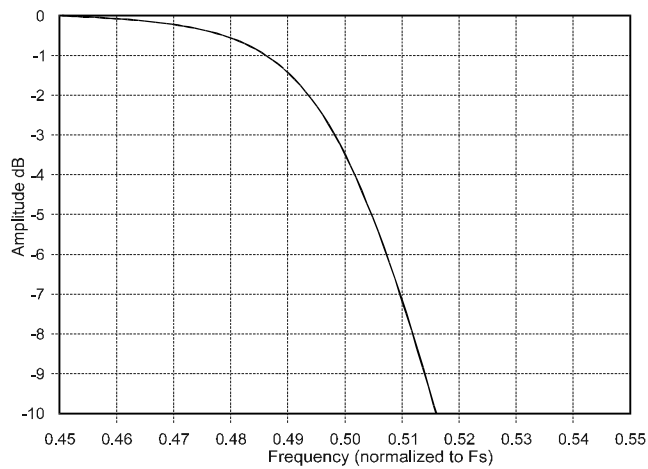
**Figure 12. Single-Speed Passband Ripple**



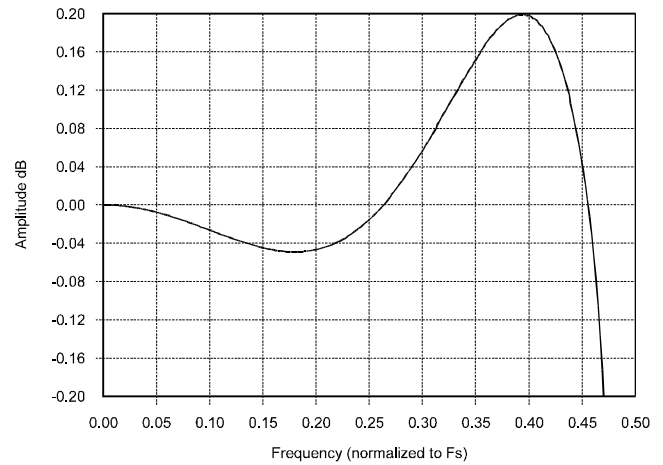
**Figure 13. Double-Speed Stopband Rejection**



**Figure 14. Double-Speed Transition Band**



**Figure 15. Double-Speed Transition Band (Detail)**

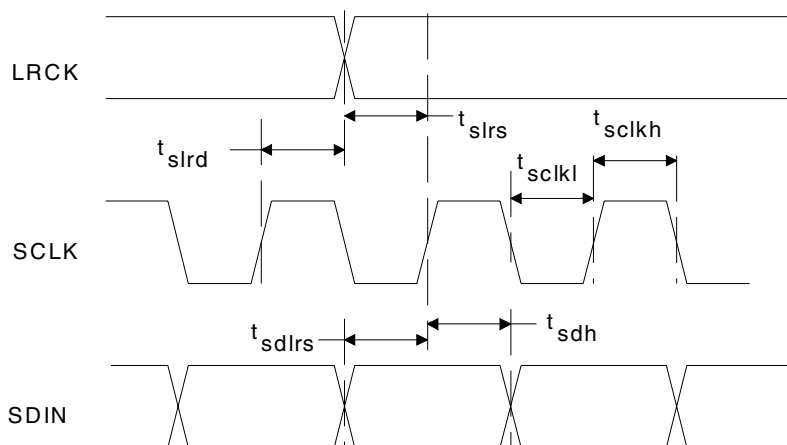


**Figure 16. Double-Speed Passband Ripple**

## SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

| Parameters                           | Symbol                     | Min   | Max              | Units |
|--------------------------------------|----------------------------|-------|------------------|-------|
| MCLK Frequency                       |                            | 1.024 | 38.4             | MHz   |
| MCLK Duty Cycle                      |                            | 45    | 55               | %     |
| Input Sample Rate<br>(Note 5)        | Single-Speed Mode<br>$F_s$ | 4     | 50               | kHz   |
|                                      | Double-Speed Mode<br>$F_s$ | 84    | 100              | kHz   |
|                                      | Quad-Speed Mode<br>$F_s$   | 170   | 200              | kHz   |
| LRCK Duty Cycle                      |                            | 40    | 60               | %     |
| SCLK Frequency                       | Single-Speed Mode          | -     | $128 \times F_s$ | Hz    |
|                                      | Double-Speed Mode          | -     | $64 \times F_s$  | Hz    |
|                                      | Quad-Speed Mode            | -     | $\frac{MCLK}{2}$ | Hz    |
| SCLK Pulse Width Low                 | $t_{sckl}$                 | 20    | -                | ns    |
| SCLK Pulse Width High                | $t_{sckh}$                 | 20    | -                | ns    |
| SCLK rising to LRCK edge delay       | $t_{slrd}$                 | 20    | -                | ns    |
| SCLK rising to LRCK edge setup time  | $t_{slrs}$                 | 20    | -                | ns    |
| SDIN valid to SCLK rising setup time | $t_{sdls}$                 | 20    | -                | ns    |
| SCLK rising to SDIN hold time        | $t_{sdh}$                  | 20    | -                | ns    |

Notes: 5. Speed mode is detected automatically, based on the input sample rate.



**Figure 17. Serial Input Timing**

**DC ELECTRICAL CHARACTERISTICS** (AGND = 0V; all voltages with respect to AGND.)

| Parameters                               |           | Symbol         | Min | Typ    | Max | Units |
|------------------------------------------|-----------|----------------|-----|--------|-----|-------|
| <b>Normal Operation</b> (Note 6)         |           |                |     |        |     |       |
| Power Supply Current                     | VA = 5.0V | I <sub>A</sub> | -   | 18     | 25  | mA    |
|                                          | VA = 3.3V |                | -   | 15     | 20  | mA    |
| Power Dissipation                        | VA = 5.0V |                | -   | 90     | 125 | mW    |
|                                          | VA = 3.3V |                | -   | 50     | 100 | mW    |
| <b>Power-down Mode</b> (Note 7)          |           |                |     |        |     |       |
| Power Supply Current                     | VA = 5.0V | I <sub>A</sub> | -   | 60     | -   | μA    |
|                                          | VA = 3.3V |                | -   | 35     | -   | μA    |
| Power Dissipation                        | VA = 5.0V |                | -   | 0.3    | -   | mW    |
|                                          | VA = 3.3V |                | -   | 0.1    | -   | mW    |
| <b>All Modes of Operation</b>            |           |                |     |        |     |       |
| Power Supply Rejection Ratio (Note 8)    | 1 kHz     | PSRR           | -   | 60     | -   | dB    |
|                                          | 60 Hz     |                | -   | 40     | -   | dB    |
| V <sub>Q</sub> Nominal Voltage           |           |                | -   | 0.5•VA | -   | V     |
| Output Impedance                         |           |                | -   | 250    | -   | kΩ    |
| Maximum allowable DC current source/sink |           |                | -   | 0.01   | -   | mA    |
| Filt+ Nominal Voltage                    |           |                | -   | VA     | -   | V     |
| Output Impedance                         |           |                | -   | 250    | -   | kΩ    |
| Maximum allowable DC current source/sink |           |                | -   | 0.01   | -   | mA    |
| MUTEC Low-Level Output Voltage           |           |                | -   | 0      | -   | V     |
| MUTEC High-Level Output Voltage          |           |                | -   | VA     | -   | V     |
| Maximum MUTEC Drive Current              |           |                | -   | 3      | -   | mA    |

**DIGITAL INTERFACE SPECIFICATIONS** (GND = 0 V; all voltages with respect to GND.)

| Parameters                                    | Symbol          | Min | Max | Units |
|-----------------------------------------------|-----------------|-----|-----|-------|
| <b>3.3 V Logic</b> (2.7 V to 3.6 V DC Supply) |                 |     |     |       |
| High-Level Input Voltage                      | V <sub>IH</sub> | 2.0 | -   | V     |
| Low-Level Input Voltage                       | V <sub>IL</sub> | -   | 0.8 | V     |
| <b>5.0 V Logic</b> (4.5 V to 5.5 V DC Supply) |                 |     |     |       |
| High-Level Input Voltage                      | V <sub>IH</sub> | 2.0 | -   | V     |
| Low-Level Input Voltage                       | V <sub>IL</sub> | -   | 0.8 | V     |

**DIGITAL INPUT CHARACTERISTICS** (AGND = 0V; all voltages with respect to AGND.)

| Parameters            | Symbol          | Min | Typ | Max | Units |
|-----------------------|-----------------|-----|-----|-----|-------|
| Input Leakage Current | I <sub>in</sub> | -   | -   | ±10 | μA    |
| Input Capacitance     |                 | -   | 8   | -   | pF    |

**THERMAL CHARACTERISTICS AND SPECIFICATIONS**

| Parameters                                      | Symbol          | Min | Typ | Max | Units   |
|-------------------------------------------------|-----------------|-----|-----|-----|---------|
| Package Thermal Resistance (multi-layer boards) | θ <sub>JA</sub> | -   | 74  | -   | °C/Watt |
| Ambient Operating Temperature (Power Applied)   | T <sub>A</sub>  | -10 | -   | +70 | °C      |

## RECOMMENDED OPERATING SPECIFICATION

| Parameters             | Symbol | Min | Typ | Max | Units |
|------------------------|--------|-----|-----|-----|-------|
| <b>DC Power Supply</b> |        |     |     |     |       |
| 3.3 V Nominal          | VA     | 2.7 | 3.3 | 3.6 | V     |
| 5.0 V Nominal          |        | 4.5 | 5   | 5.5 | V     |

**ABSOLUTE MAXIMUM RATINGS** (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

| Parameters                                    | Symbol    | Min  | Max    | Units |
|-----------------------------------------------|-----------|------|--------|-------|
| DC Power Supply                               | VA        | -0.3 | 6.0    | V     |
| Input Current (Note 9)                        | $I_{in}$  | -    | ±10    | mA    |
| Digital Input Voltage                         | $V_{IND}$ | -0.3 | VA+0.4 | V     |
| Ambient Operating Temperature (power applied) | $T_A$     | -55  | 125    | °C    |
| Storage Temperature                           | $T_{stg}$ | -65  | 150    | °C    |

- Notes:
- Normal operation is defined as  $\overline{RST} = HI$  with a 997 Hz, 0dBFS input sampled at the highest  $F_s$  for each speed mode, and open outputs, unless otherwise specified.
  - Power Down Mode is defined as  $\overline{RST} = LO$  with all clocks and data lines held static.
  - Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.
  - Any pin except supplies.

## 5. PARAMETER DEFINITIONS

### Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

### Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

### Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

### Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

### Gain Drift

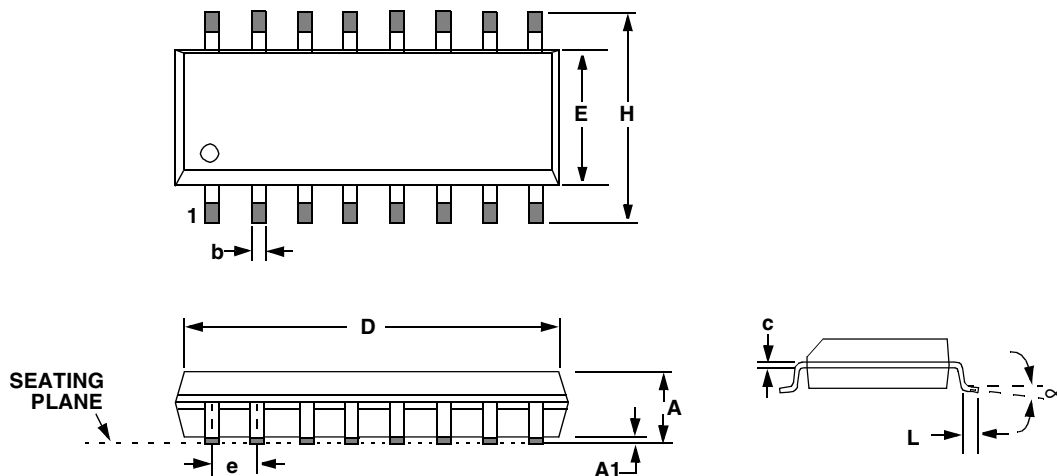
The change in gain value with temperature. Units in ppm/°C.

## 6. REFERENCES

- 1) CDB4340A Evaluation Board Datasheet

## 7. PACKAGE DIMENSIONS

### 16L SOIC (150 MIL BODY) PACKAGE DRAWING



| DIM      | INCHES |       |       | MILLIMETERS |      |       |
|----------|--------|-------|-------|-------------|------|-------|
|          | MIN    | NOM   | MAX   | MIN         | NOM  | MAX   |
| A        | 0.053  | 0.064 | 0.069 | 1.35        | 1.63 | 1.75  |
| A1       | 0.004  | 0.006 | 0.010 | 0.10        | 0.15 | 0.25  |
| b        | 0.013  | 0.016 | 0.020 | 0.33        | 0.41 | 0.51  |
| C        | 0.0075 | 0.008 | 0.010 | 0.19        | 0.20 | 0.25  |
| D        | 0.386  | 0.390 | 0.394 | 9.80        | 9.91 | 10.00 |
| E        | 0.150  | 0.154 | 0.157 | 3.80        | 3.90 | 4.00  |
| e        | 0.040  | 0.050 | 0.060 | 1.02        | 1.27 | 1.52  |
| H        | 0.228  | 0.236 | 0.244 | 5.80        | 6.0  | 6.20  |
| L        | 0.016  | 0.025 | 0.050 | 0.40        | 0.64 | 1.27  |
| $\infty$ | 0°     | 4°    | 8°    | 0°          | 4°   | 8°    |

**JEDEC #: MS-012**

Controlling Dimension is Millimeters