24LC32A MODULE

32K I²C™ Serial EEPROM in ISO Micromodule

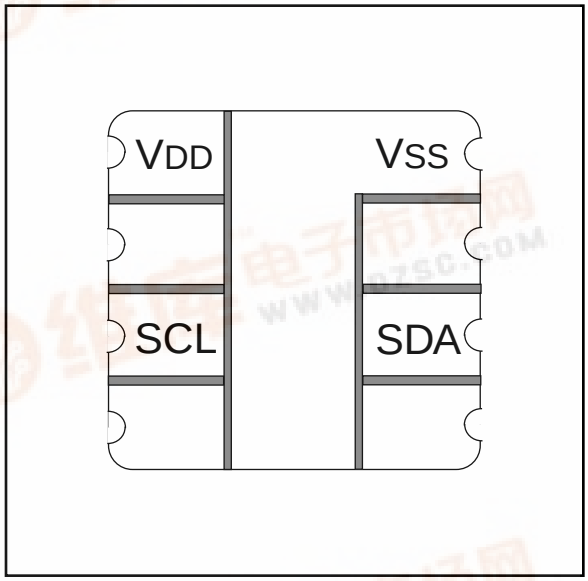
FEATURES

- ISO 7816 compliant contact locations
- Single supply with operation down to 2.5V
  - Maximum write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA max at 2.5V
- Two wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles guaranteed
- 32 byte page or byte write modes available
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C

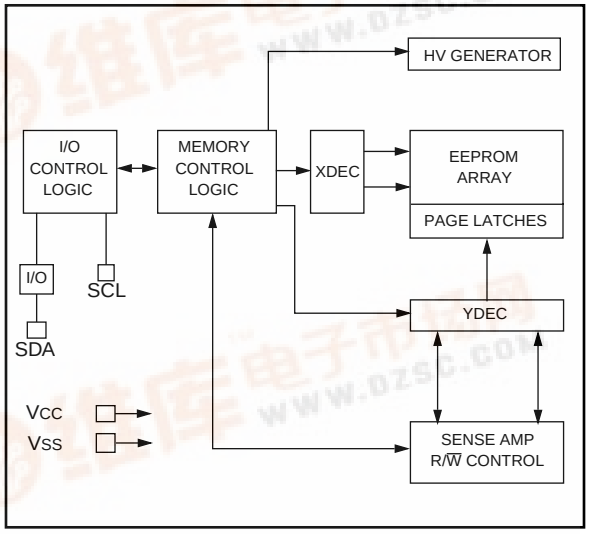
DESCRIPTION

The Microchip Technology Inc. 24LC32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM in an ISO micromodule for use in smart card applications. The device has a page-write capability of up to 32 bytes.

ISO MODULE LAYOUT



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

24LC32A MODULE

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature ..... -65˚C to +150˚C
Ambient temp. with power applied..... -65˚C to +125˚C
Soldering temperature of leads (10 seconds) .. +300˚C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTIONS

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+2.5V to 6.0V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +2.5V to 6.0V Commercial (C):Tamb = 0˚C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
SCL and SDA pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC		—	V	Note 1
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN,COUT	—		10	pF	VCC = 5.0V (Note 1) Tamb = 25˚C, f_c = 1 MHz
Operating current	ICC Write	—		3	mA	VCC = 6.0V
	ICC Read	—		400	µA	VCC = 6.0V, SCL = 400Khz
Standby current	ICCS	—	1µA	5	µA	SCL = SDA = VCC = 5.0V
	ICCS			1	µA	VCC = 2.5V (Note 1)

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

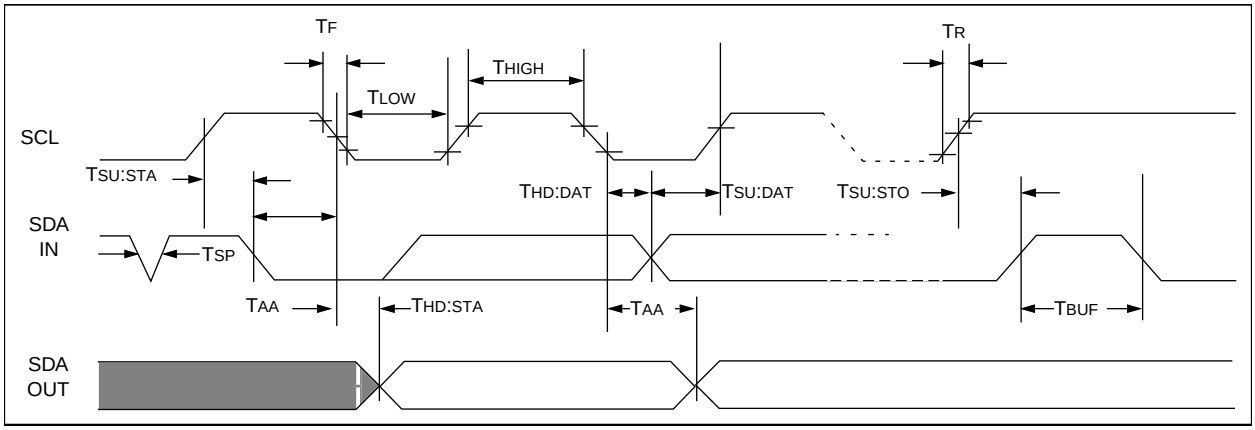
Parameter	Symbol	Vcc = 2.5 - 6.0V STD. MODE		Vcc = 4.5 - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms	Byte or Page mode

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

FIGURE 1-1: BUS TIMING DATA



24LC32A MODULE

2.0 PIN DESCRIPTIONS

2.1 SDA (Serial Data)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL (Serial Clock)

This input is used to synchronize the data transfer from and to the device.

3.0 FUNCTIONAL DESCRIPTION

The 24LC32A supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC32A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (See Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC32A does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC32A) will leave the data line HIGH to enable the master to generate the STOP condition. (See Figure 4-2)

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

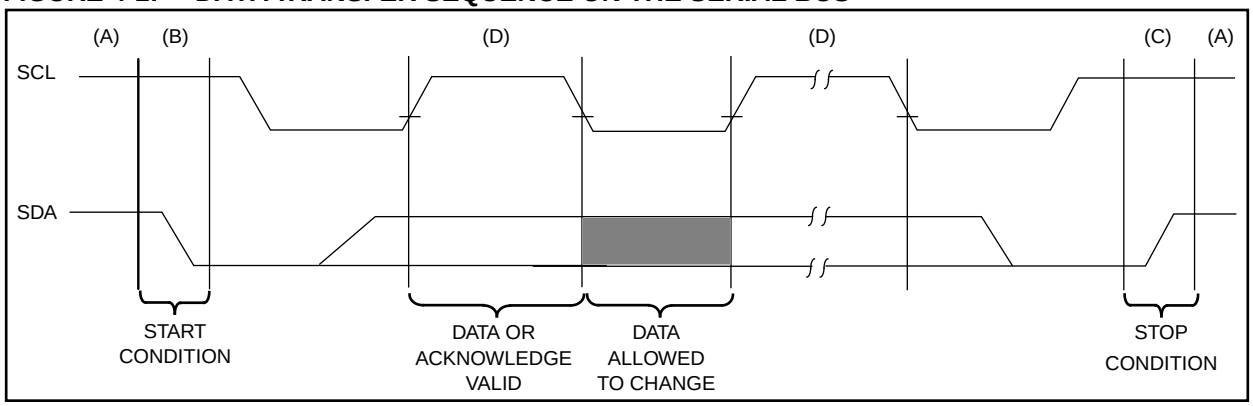
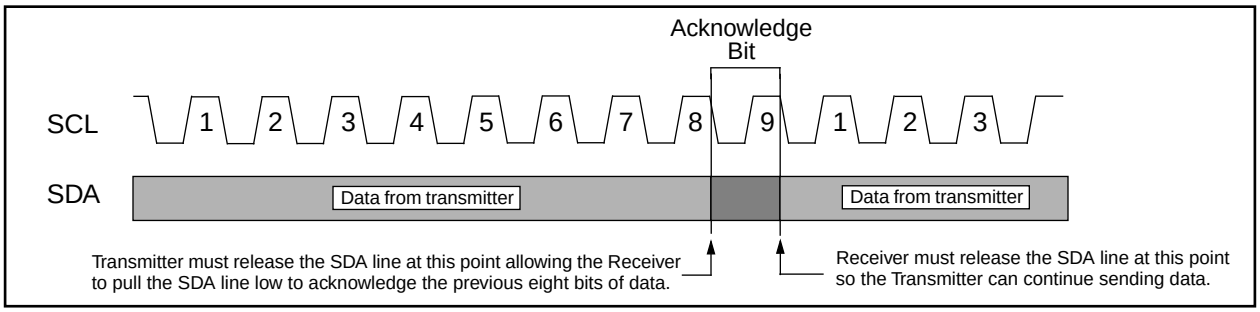


FIGURE 4-2: ACKNOWLEDGE TIMING



5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device. (See Figure 5-1) The control byte consists of a four bit control code; for the 24LC32A this is set as 1010 binary for read and write operations. The next three bits are device select bits on standard devices, however, for micromodules, these must be zeros. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5-2). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

Following the start condition, the 24LC32A monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a valid control byte, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC32A will select a read or write operation

FIGURE 5-1: CONTROL BYTE FORMAT

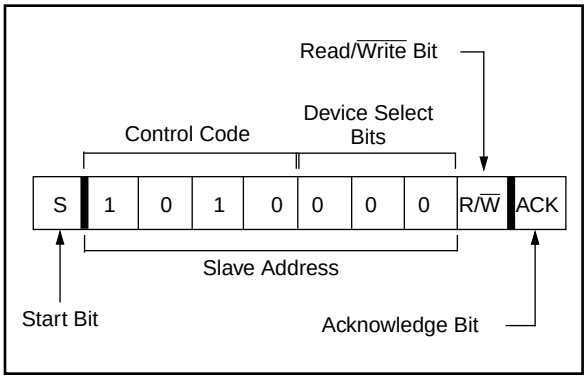
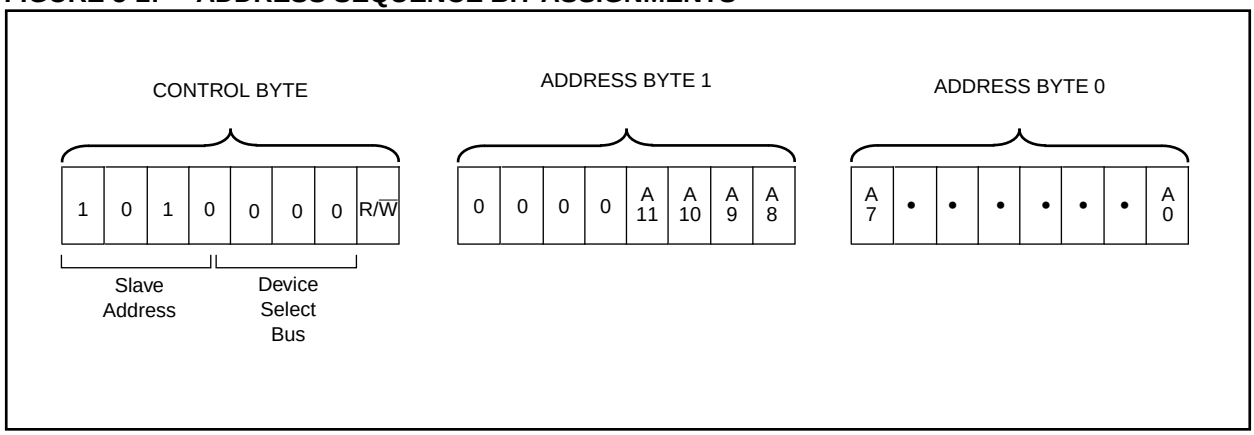


FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC32A MODULE. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC32A the master device will transmit the data word to be written into the addressed memory location.

The 24LC32A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC32A will not generate acknowledge signals (see Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC32A in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 32 bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin. (see Figure 6-2).

FIGURE 6-1: BYTE WRITE

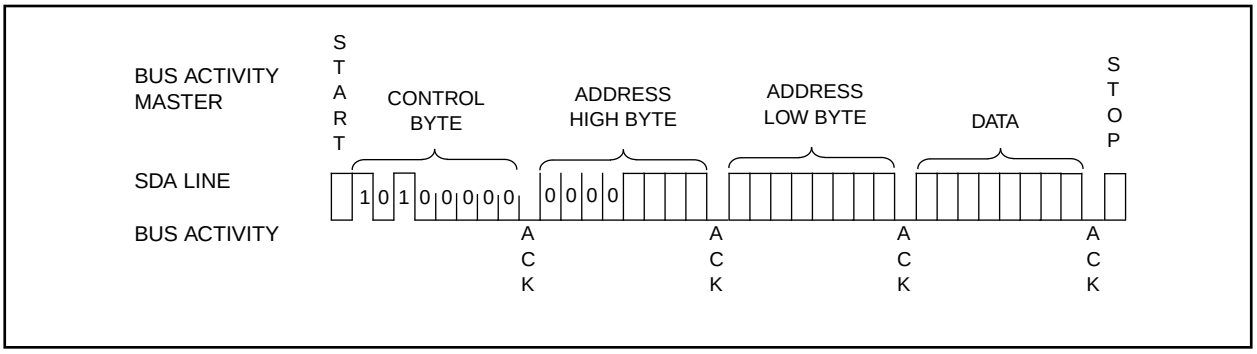
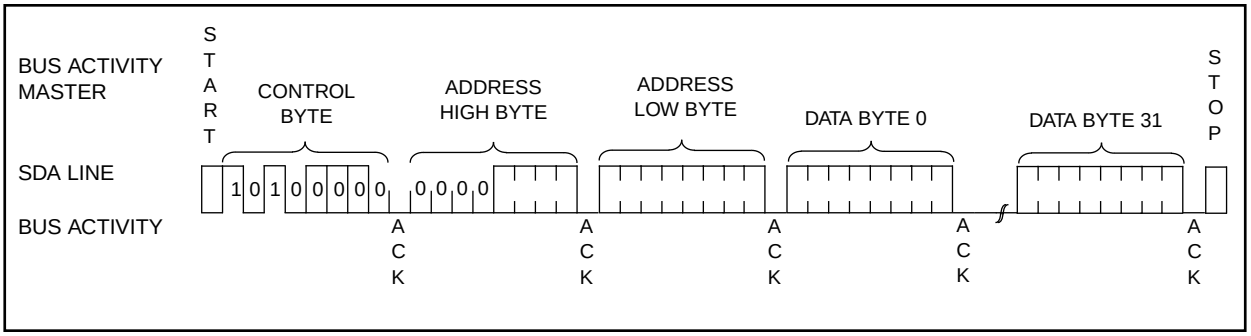


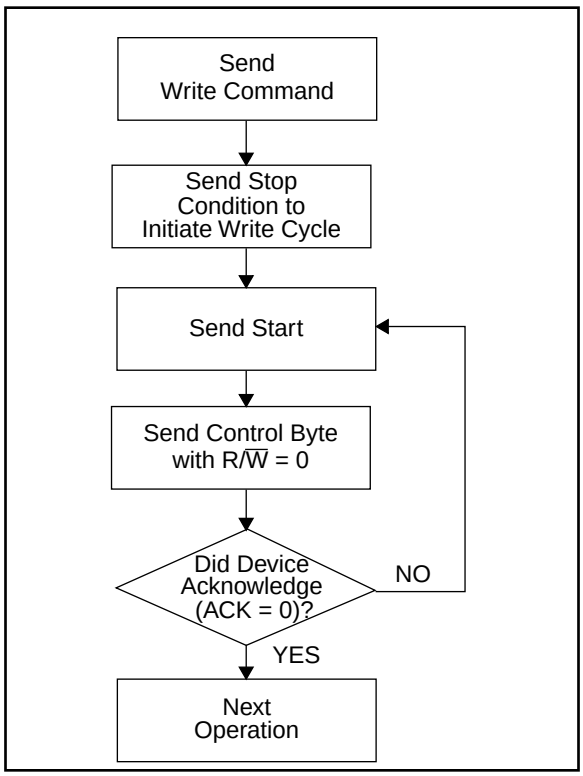
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

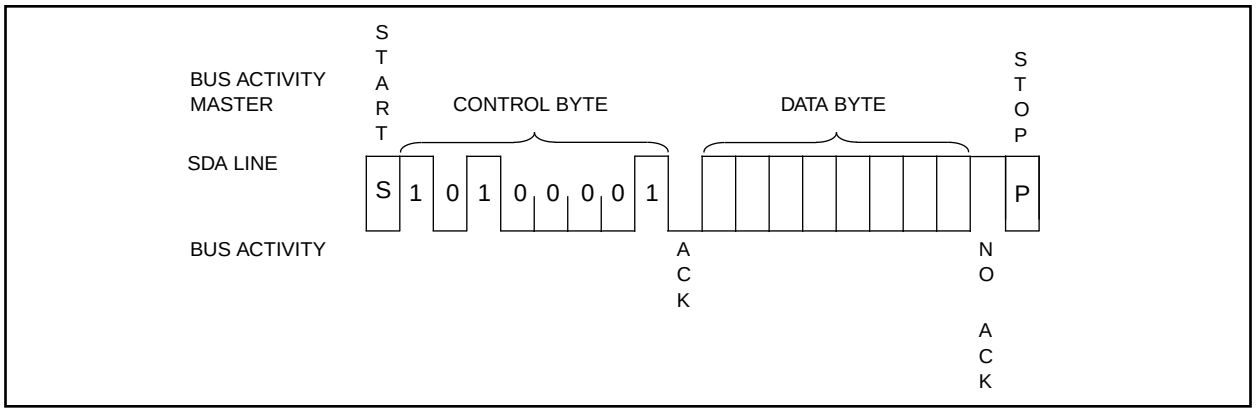
8.1 Current Address Read

The 24LC32A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC32A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC32A discontinues transmission (see Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC32A as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC32A will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC32A to discontinue transmission (see Figure 8-2).

FIGURE 8-1: CURRENT ADDRESS READ



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC32A transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC32A to transmit the next sequentially addressed 8 bit word (see Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC32A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFF to address 000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 8-2: RANDOM READ

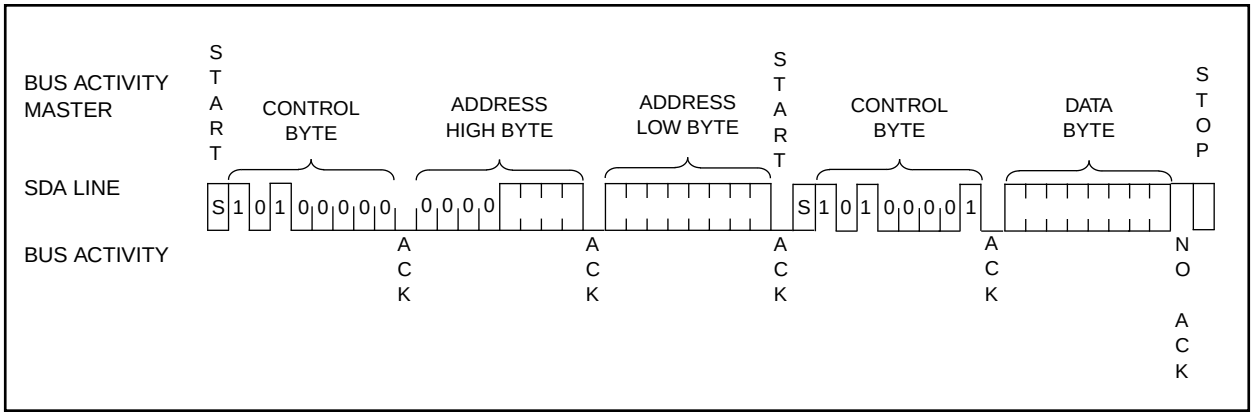
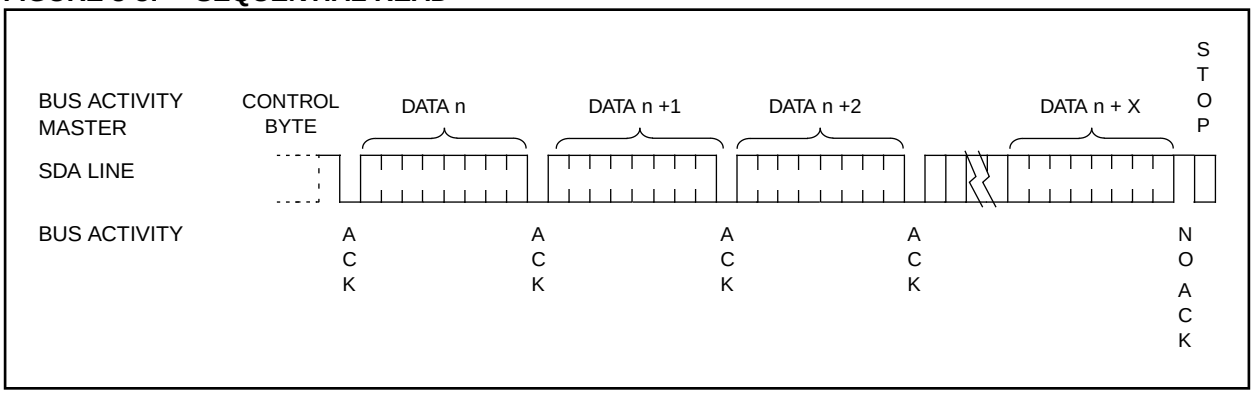


FIGURE 8-3: SEQUENTIAL READ



9.0 SHIPPING METHOD

The micromodules will be shipped to customers in clear plastic trays. Each tray holds 150 modules, and the trays can be stacked in a manner similar to shipping die in waffle packs. A tray drawing with dimensions is shown in Figure 9-1.

FIGURE 9-1: TRAY DIMENSIONS

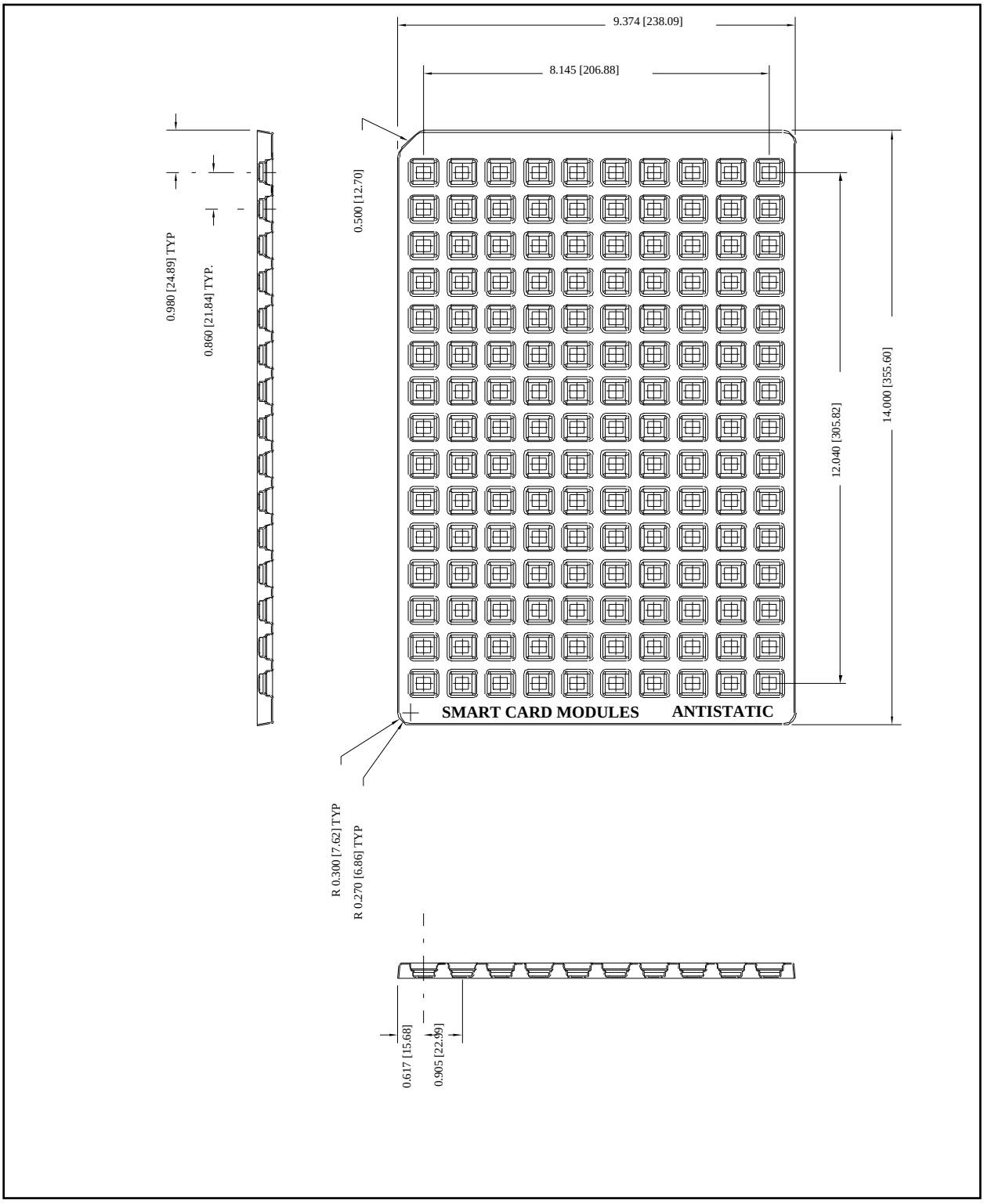
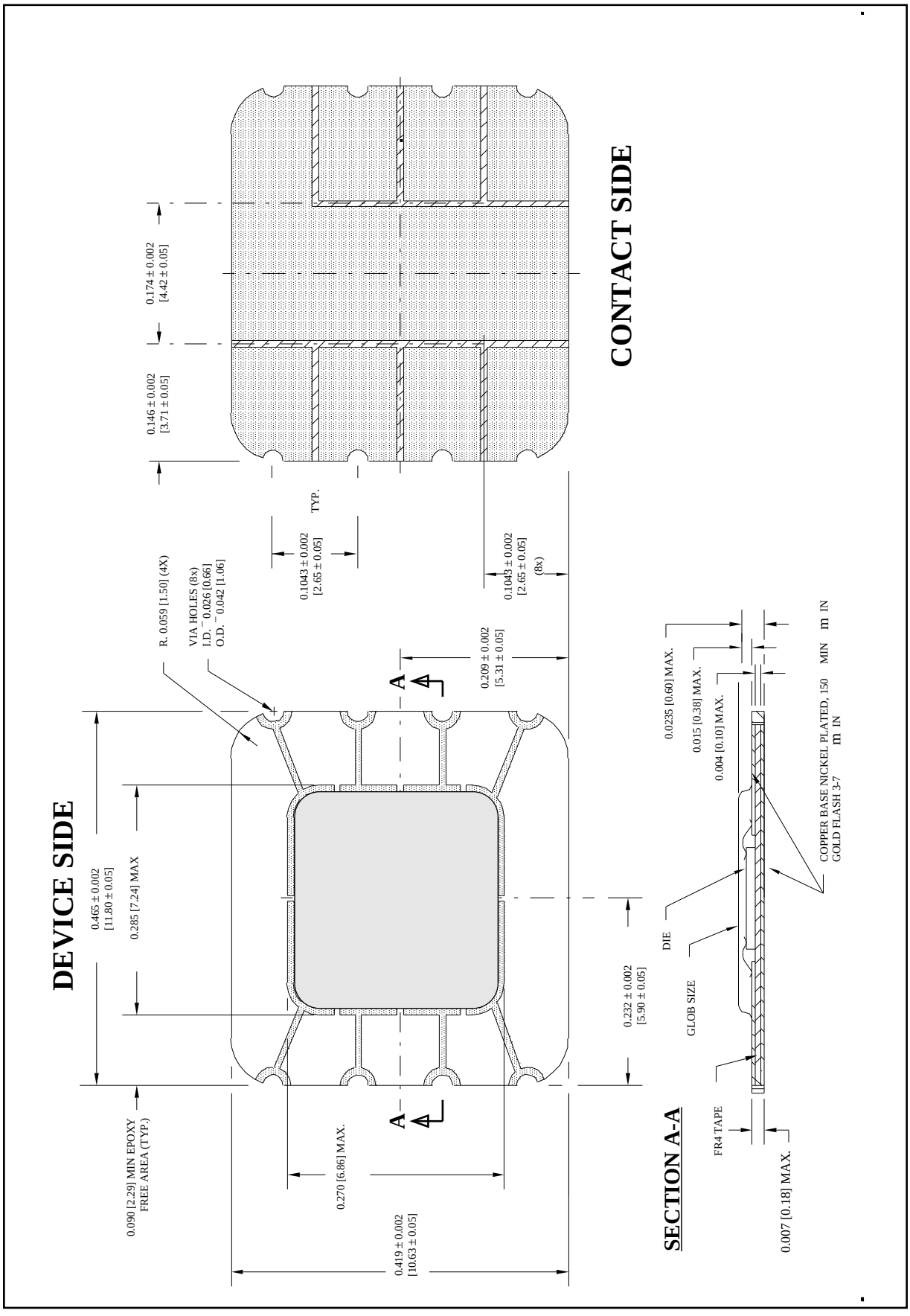


FIGURE 9-2: MODULE DIMENSIONS



24LC32A MODULE

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24LC32A MODULE

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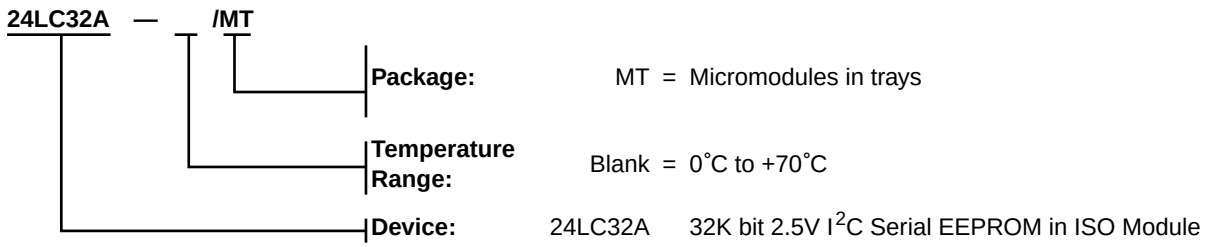
24LC32A MODULE PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277.
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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