S71PL129JC0/S71PL129JB0/S71PL129JA0

Stacked Multi-Chip Product (MCP) Flash Memory and pSRAM 128 Megabit (8M x 16-bit) CMOS 3.0 Volt-only Simultaneous Operation, Page Mode Flash Memory with 64/32/16 Megabit (4M/2M/1M x 16-bit) Pseudo-Static RAM

S P A N S I O N™

ADVANCE INFORMATION

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
    - 65ns (65ns Flash, 70ns pSRAM)

- **Package**
    - 8 x 11.6 x 1.2 mm 64 ball FBGA
- **Operating Temperature**
    - −25°C to +85°C (Wireless)
    - −40°C to +85°C (Industrial)
- **Dual CE# Flash memory**

General Description

The S71PL129J series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One S29PL129J Flash memory die

- One 16M, 32M, or 64M pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheets for further details.

		Flash Memory Density
		128Mb
pSRAM Density	64Mb	S71PL129JC0
	32Mb	S71PL129JB0
	16Mb	S71PL129JA0

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Product Selector Guide

128 Mb Flash Memory

Device-Model#	pSRAM density	Flash Access time (ns)	(p)SRAM Access time (ns)	pSRAM type	Package
S71PL129JA0-9P	16M pSRAM	65	70	Type 7	TLA064
S71PL129JB0-9Z	32M pSRAM	65	70	Type 7	TLA064
S71PL129JB0-9B	32M pSRAM	65	70	Type 2	TLA064
S71PL129JB0-9U	32M pSRAM	65	70	Type 6	TLA064
S71PL129JC0-9Z	64M pSRAM	65	70	Type 7	TLA064
S71PL129JC0-9U	64M pSRAM	65	70	Type 6	TLA064

S7IPL129JC0/S7IPL129JB0/S7IPL129JA0

S29PL129J for MCP

Revision Summary

MCP Block Diagram

Connection Diagram

64-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)
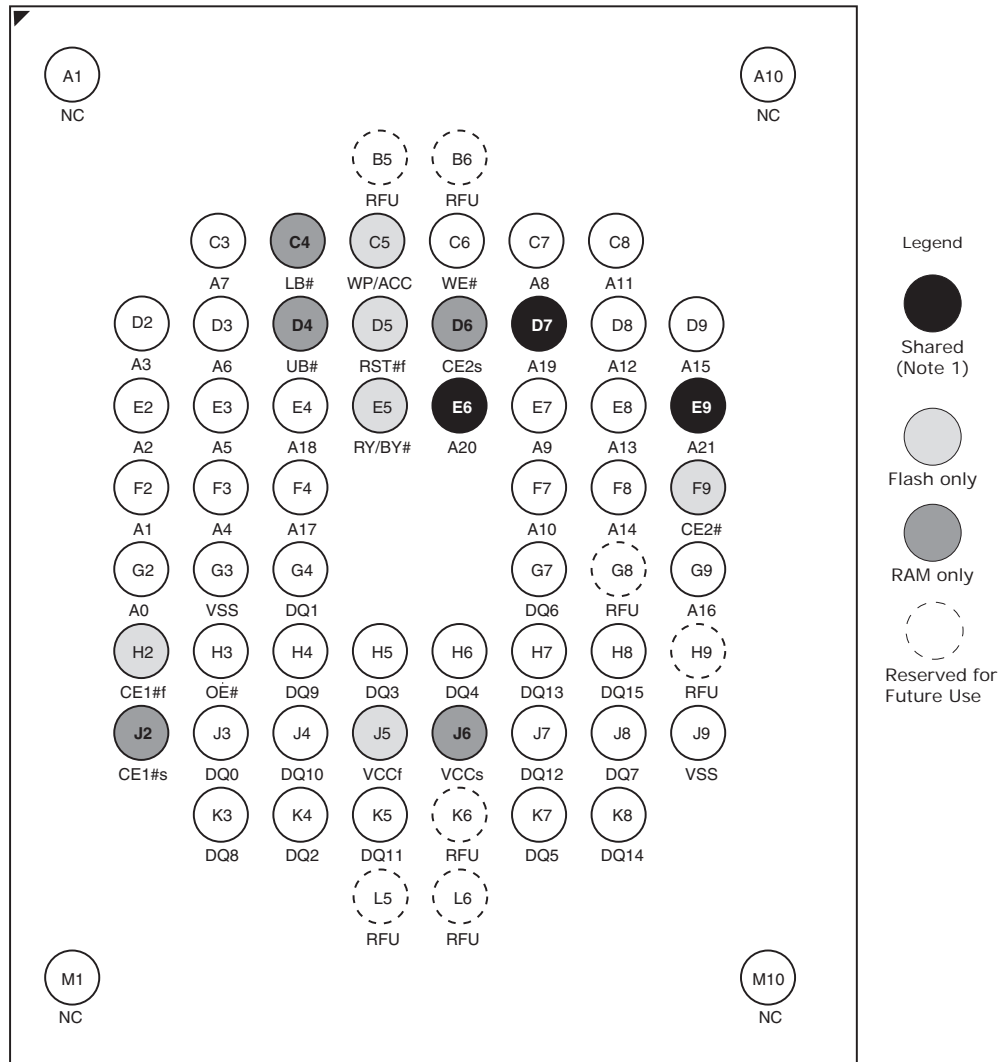
Note: *May be shared depending on density:*

— A21 is shared for the 64M pSRAM configuration.
— A20 is shred for the 32M pSRAM configuration.
— A19 is shared for the 16M pSRAM configuration.

MCP	Flash-only Addresses	Shared Addresses
S71PL129JC0	A22	A21-A0
S71PL129JB0	A22-A21	A20-A0
S71PL129JA0	A22-A20	A19-A0

Note: *It is advised to tie J5 and L5 together on the board.*

Input/Output Description

Pin Description

A21–A0	=	22 Address Inputs (Common)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE1#f	=	Chip Enable 1 (Flash)
CE2#f	=	Chip Enable 2 (Flash)
CE1#ps	=	Chip Enable 1 (pSRAM)
CE2ps	=	Chip Enable 2 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output
UB#	=	Upper Byte Control (pSRAM)
LB#	=	Lower Byte Control (pSRAM)
RESET#	=	Hardware Reset Pin, Active Low (Flash 1)
WP#/ACC	=	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}ps$	=	pSRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

Logic Symbol
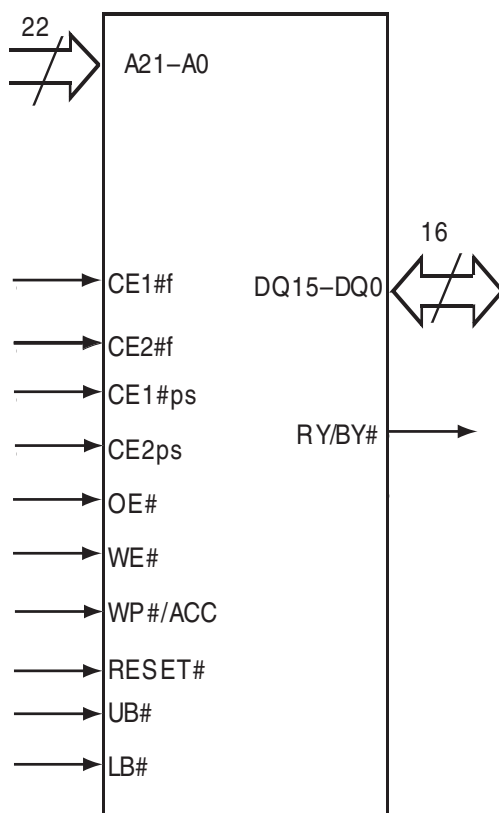
Ordering Information

The order number is formed by a valid combinations of the following:

S71PL   129   J   B0   BA   W   9   Z   0

PACKING TYPE

0	=	Tray
2	=	7″ Tape and Reel
3	=	13″ Tape and Reel

MODEL NUMBER

See valid combinations table.

PACKAGE MODIFIER

9	=	8 x 11.6 mm, 1.2 mm height, 64 balls (TLA064)

TEMPERATURE RANGE

W	=	Wireless (-25°C to +85°C)
I	=	Industrial (-40°C to +85°C)

PACKAGE TYPE

BA	=	Fine-pitch BGA Lead (Pb)-free compliant package
BF	=	Fine-pitch BGA Lead (Pb)-free package

pSRAM DENSITY

C0	=	64 Mb pSRAM
B0	=	32 Mb pSRAM
A0	=	16 Mb pSRAM

PROCESS TECHNOLOGY

J	=	110 nm, Floating Gate Technology

FLASH DENSITY

129	=	128Mb, dual CE#

PRODUCT FAMILY

S71PL Multi-chip Product (MCP)
3.0-volt Simultaneous Read/Write, Page Mode Flash Memory and RAM

S71PL129J Valid Combinations				Speed Options (ns)	(p)SRAM Type/Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type			
S71PL129JA0	BAW	9P	0, 2, 3 (Note 1)	65	pSRAM 7 / 70	(Note 2)
S71PL129JB0		9Z			pSRAM 7 / 70	
S71PL129JB0		9B			pSRAM 2 / 70	
S71PL129JB0		9U			pSRAM 6 / 70	
S71PL129JC0		9Z			pSRAM 7 / 70	
S71PL129JC0		9U			pSRAM 6 / 70	
S71PL129JA0	BFW	9P	0, 2, 3 (Note 1)	65	pSRAM 7 / 70	
S71PL129JB0		9Z			pSRAM 7 / 70	
S71PL129JB0		9B			pSRAM 2 / 70	
S71PL129JB0		9U			pSRAM 6 / 70	
S71PL129JC0		9Z			pSRAM 7 / 70	
S71PL129JC0		9U			pSRAM 6 / 70	
S71PL129JA0	BAI	9P	0, 2, 3 (Note 1)	65	pSRAM 7 / 70	
S71PL129JB0		9Z			pSRAM 7 / 70	
S71PL129JB0		9B			pSRAM 2 / 70	
S71PL129JB0		9U			pSRAM 6 / 70	
S71PL129JC0		9Z			pSRAM 7 / 70	
S71PL129JC0		9U			pSRAM 6 / 70	
S71PL129JA0	BFI	9P	0, 2, 3 (Note 1)	65	pSRAM 7 / 70	
S71PL129JB0		9Z			pSRAM 7 / 70	
S71PL129JB0		9B			pSRAM 2 / 70	
S71PL129JB0		9U			pSRAM 6 / 70	
S71PL129JC0		9Z			pSRAM 7 / 70	
S71PL129JC0		9U			pSRAM 6 / 70	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

3. *Contact factory for availability of any of the above OPNs. RAM type availability may vary over time.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

TLA064—64-ball Fine-Pitch Ball Grid Array (FBGA)
8 x 11.6 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE	TLA 064			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	64			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. e REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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S29PL129J for MCP

128 Megabit (8 M x 16-Bit)
CMOS 3.0 Volt-only, Simultaneous Read/Write
Flash Memory with Enhanced VersatileIO™ Control

S P A N S I O N™

Datasheet

Distinctive Characteristics

Architectural Advantages

- **128 Mbit Page Mode devices**
  - Page size of 8 words: Fast page read access from random locations within the page

- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.6 volt read, erase, and program operations for battery-powered applications

- **Dual Chip Enable inputs (only in PL129J)**
  - Two CE# inputs control selection of each half of the memory space

- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations

- **FlexBank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - CE#1 controlled banks:
    Bank 1A:
    - 16Mbit (4Kw x 8 and 32Kw x 31)
    Bank 1B:
    - 48Mbit (32Kw x 96)
  - CE#2 controlled banks:
    Bank 2A:
    - 48 Mbit (32Kw x 96)
    Bank 2B:
    - 16Mbit (4Kw x 8 and 32Kw x 31)

- **Enhanced VersatileI/O™ (V_{IO}) Control**
  - Output voltage generated and input voltages tolerated on all control inputs and I/Os is determined by the voltage on the V_{IO} pin

- **Secured Silicon Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words

- **Both top and bottom boot blocks in one device**

- **Manufactured on 110 nm process technology**

- **Data Retention: 20 years typical**

- **Cycling Endurance: 1 million cycles per sector typical**

Performance Characteristics

- **High Performance**
  - Page access times as fast as 20 ns
  - Random access times as fast as 55 ns

- **Power consumption (typical values at 10 MHz)**
  - 45 mA active read current
  - 17 mA program/erase current
  - 0.2 µA typical standby mode current

Software Features

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F, Am29LV, Am29DL, and AM29PDL families and MBM29QM/RM, MBM29LV, MBM29DL, MBM29PDL families

- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices

- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank

- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion

- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data

- **WP#/ ACC (Write Protect/Acceleration) input**
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{IH}, allows removal of sector protection
  - At V_{HH}, provides accelerated programming in a factory setting

- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups

to prevent program or erase operations within that sector

— Sectors can be locked and unlocked in-system at V_{CC} level

■ **Password Sector Protection**

— A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password

General Description

The PL129J is a 128 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8 Mwords.

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 20 to 30 ns, with corresponding random access times of 55 to 70 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Note: Device PL129J has 2 chip enable inputs (CE1#, CE2#).

Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Bank	PLI29J Sectors	CE# Control
1A	16 Mbit (4 Kw x 8 and 32 Kw x 31)	CE1#
1B	48 Mbit (32 Kw x 96)	CE1#
2A	48 Mbit (32 Kw x 96)	CE2#
2B	16 Mbit (4 Kw x 8 and 32 Kw x 31)	CE2#

Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two

write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Block Diagram
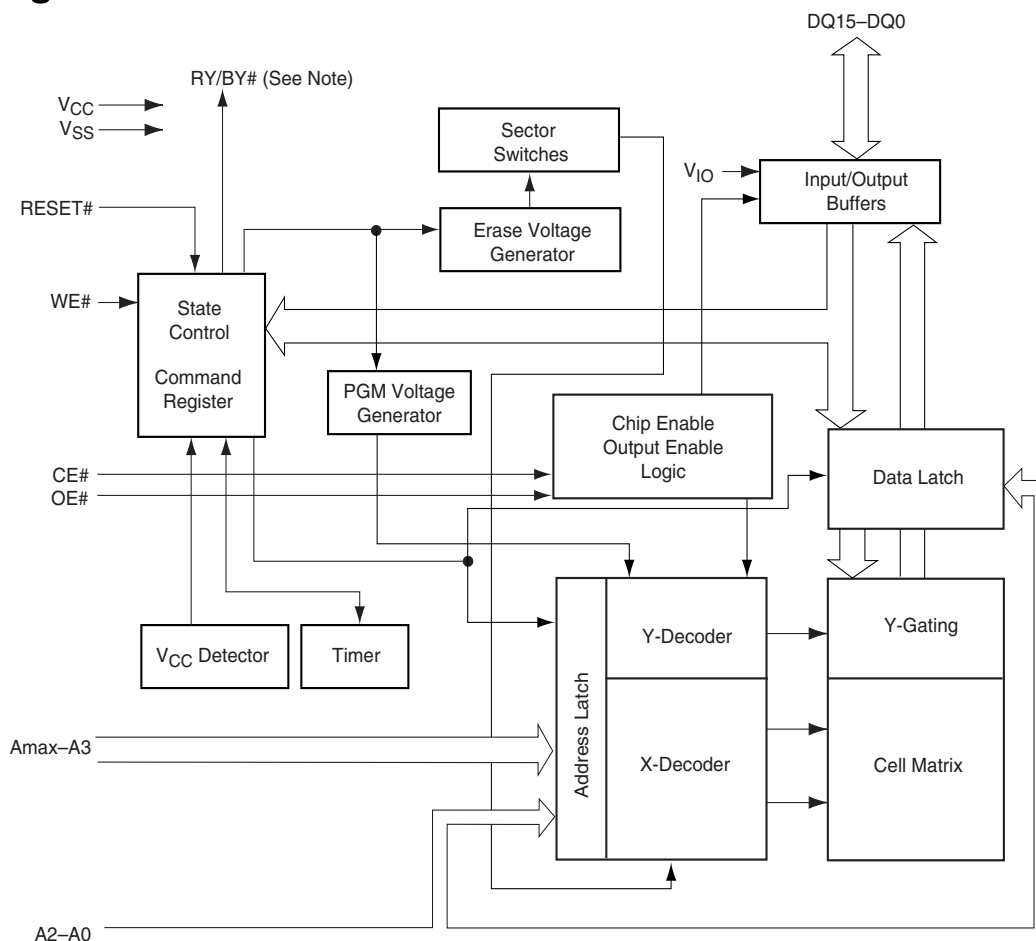
Notes:

1. RY/BY# is an open drain output.
2. For PL129J there are two CE# (CE1# and CE2#)

Simultaneous Read/Write Block Diagram (PLI29J)
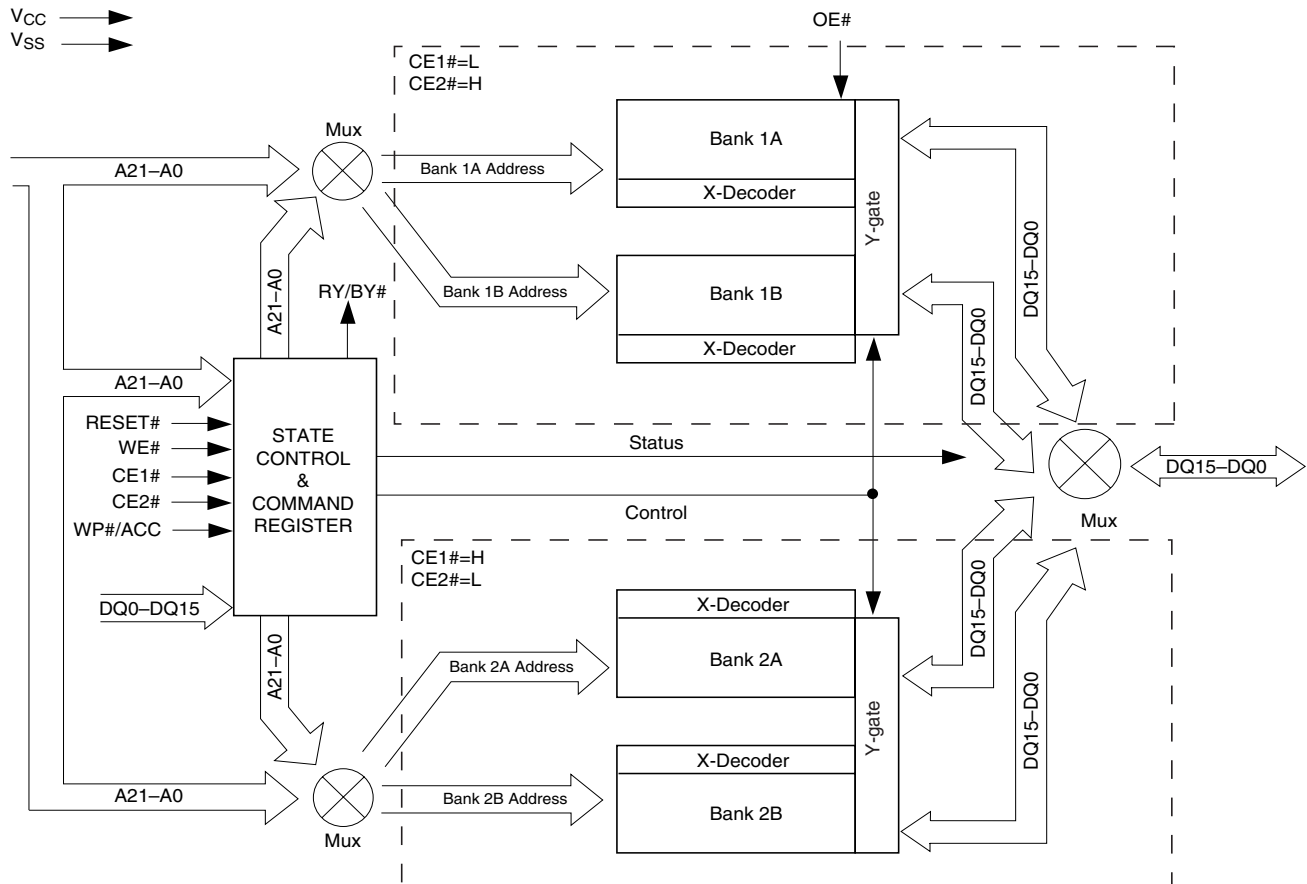
Notes:
1. Amax = A21 (PL129J)

Pin Description

Amax–A0	=	Address bus
DQ15–DQ0	=	16-bit data inputs/outputs/float
CE#	=	Chip Enable Inputs
OE#	=	Output Enable Input
WE#	=	Write Enable
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
RY/BY#	=	Ready/Busy output and open drain. When RY/BY# = V_{IH}, the device is ready to accept read operations and commands. When RY/BY# = V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
WP#/ACC	=	Write Protect/Acceleration Input. When WP#/ACC = V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC = V_{IH}, these sector are unprotected unless the DYB or PPB is programmed. When WP#/ACC = 12V, program and erase operations are accelerated.
V_{IO}	=	Input/Output Buffer Power Supply 2.7 V to 3.6 V
V_{CC}	=	Chip Power Supply (2.7 V to 3.6 V or 2.7 to 3.3 V)
RESET#	=	Hardware Reset Pin
CE1#, CE2#	=	Chip Enable Inputs. CE1# controls the 64Mb in Banks 1A and 1B. CE2# controls the 64 Mb in Banks 2A and 2B.

Notes:
1. *Amax = A21*

Logic Symbol
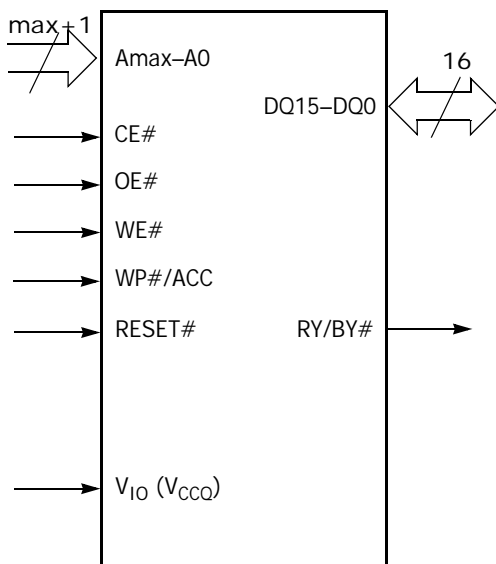
Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table I.   PLI29J Device Bus Operations

Operation	CEI#	CE2#	OE#	WE#	RESET#	WP#/ACC	Addresses (A2I–A0)	DQI5–DQ0
Read	L	H	L	H	H	X	A_{IN}	D_{OUT}
	H	L						
Write	L	H	H	L	H	X (Note 2)	A_{IN}	D_{IN}
	H	L						
Standby	$V_{IO}\pm$ 0.3 V	$V_{IO} \pm$ 0.3 V	X	X	$V_{IO} \pm$ 0.3 V	X	X	High-Z
Output Disable	L	L	H	H	H	X	X	High-Z
Reset	X	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 8.5–9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:
1. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See ""High Voltage Sector Protection" on page 37."*
2. *WP#/ACC must be high when writing to upper two and lower two sectors.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins to V_{IL}. In PL129J, CE1# and CE2# are the power control and select the lower (CE1#) or upper (CE2#) halves of the device. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See Table 24 for timing specifications and Figure 11 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

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Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A3 select an 8 word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE1# and CE#2 are deasserted (=V_{IH}), the reassertion of CE1# or CE#2 for subsequent access has access time of t_{ACC} or t_{CE}. Here again, CE1#/CE#2 selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A3 constant and changing A2–A0 to select the specific word within that page.

Table 2.   Page Select

Word	A2	AI	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, and erase-suspend program), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (A21–A19) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Bank	CEI#	CE2#	PLI29J: A2I–A20
Bank 1A	0	1	00
Bank 1B	0	1	01, 10, 11

Bank 2A	1	0	00, 01, 10
Bank 2B	1	0	11

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE1# or CE#2 to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. "Word Program Command Sequence" on page 46 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the set of address space that each sector occupies. A "bank address" is the set of address bits required to uniquely select a bank. Similarly, a "sector address" refers to the address bits required to uniquely select a sector. "Command Definitions" on page 45 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. See the timing specification tables and timing diagrams in "Reset" for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to V_{CC} when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. See "Secured Silicon Sector Addresses" on page 29 and "Autoselect Command Sequence" on page 46 for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE1# or CE#2 and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE1# or CE#2 and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device is in standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in "DC Characteristics" represents the CMOS standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in "DC Characteristics" represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS}\pm0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS}\pm0.3$ V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 13 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 3.   S29PL129J Sector Architecture (Sheet 1 of 7)

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
	SA1-0	0	1	0000000000	4	000000h–000FFFh
	SA1-1	0	1	0000000001	4	001000h–001FFFh
	SA1-2	0	1	0000000010	4	002000h–002FFFh
	SA1-3	0	1	0000000011	4	003000h–003FFFh
	SA1-4	0	1	0000000100	4	004000h–004FFFh
	SA1-5	0	1	0000000101	4	005000h–005FFFh
	SA1-6	0	1	0000000110	4	006000h–006FFFh
	SA1-7	0	1	0000000111	4	007000h–007FFFh
	SA1-8	0	1	0000001XXX	32	008000h–00FFFFh
	SA1-9	0	1	0000010XXX	32	010000h–017FFFh
	SA1-10	0	1	0000011XXX	32	018000h–01FFFFh
	SA1-11	0	1	0000100XXX	32	020000h–027FFFh
	SA1-12	0	1	0000101XXX	32	028000h–02FFFFh
	SA1-13	0	1	0000110XXX	32	030000h–037FFFh
	SA1-14	0	1	0000111XXX	32	038000h–03FFFFh
	SA1-15	0	1	0001000XXX	32	040000h–047FFFh
	SA1-16	0	1	0001001XXX	32	048000h–04FFFFh
	SA1-17	0	1	0001010XXX	32	050000h–057FFFh
	SA1-18	0	1	0001011XXX	32	058000h–05FFFFh
Bank 1A	SA1-19	0	1	0001100XXX	32	060000h–067FFFh
	SA1-20	0	1	0001101XXX	32	068000h–06FFFFh
	SA1-21	0	1	0001110XXX	32	070000h–077FFFh
	SA1-22	0	1	0001111XXX	32	078000h–07FFFFh
	SA1-23	0	1	0010000XXX	32	080000h–087FFFh
	SA1-24	0	1	0010001XXX	32	088000h–08FFFFh
	SA1-25	0	1	0010010XXX	32	090000h–097FFFh
	SA1-26	0	1	0010011XXX	32	098000h–09FFFFh
	SA1-27	0	1	0010100XXX	32	0A0000h–0A7FFFh
	SA1-28	0	1	0010101XXX	32	0A8000h–0AFFFFh
	SA1-29	0	1	0010110XXX	32	0B0000h–0B7FFFh
	SA1-30	0	1	0010111XXX	32	0B8000h–0BFFFFh
	SA1-31	0	1	0011000XXX	32	0C0000h–0C7FFFh
	SA1-32	0	1	0011001XXX	32	0C8000h–0CFFFFh
	SA1-33	0	1	0011010XXX	32	0D0000h–0D7FFFh
	SA1-34	0	1	0011011XXX	32	0D8000h–0DFFFFh
	SA1-35	0	1	0011100XXX	32	0E0000h–0E7FFFh
	SA1-36	0	1	0011101XXX	32	0E8000h–0EFFFFh
	SA1-37	0	1	0011110XXX	32	0F0000h–0F7FFFh
	SA1-38	0	1	0011111XXX	32	0F8000h–0FFFFFh

Table 3.   S29PLI29J Sector Architecture (Sheet 2 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank 1B	SA1-39	0	1	0100000XXX	32	100000h–107FFFh
	SA1-40	0	1	0100001XXX	32	108000h–10FFFFh
	SA1-41	0	1	0100010XXX	32	110000h–117FFFh
	SA1-42	0	1	0100011XXX	32	118000h–11FFFFh
	SA1-43	0	1	0100100XXX	32	120000h–127FFFh
	SA1-44	0	1	0100101XXX	32	128000h–12FFFFh
	SA1-45	0	1	0100110XXX	32	130000h–137FFFh
	SA1-46	0	1	0100111XXX	32	138000h–13FFFFh
	SA1-47	0	1	0101000XXX	32	140000h–147FFFh
	SA1-48	0	1	0101001XXX	32	148000h–14FFFFh
	SA1-49	0	1	0101010XXX	32	150000h–157FFFh
	SA1-50	0	1	0101011XXX	32	158000h–15FFFFh
	SA1-51	0	1	0101100XXX	32	160000h–167FFFh
	SA1-52	0	1	0101101XXX	32	168000h–16FFFFh
	SA1-53	0	1	0101110XXX	32	170000h–177FFFh
	SA1-54	0	1	0101111XXX	32	178000h–17FFFFh
	SA1-55	0	1	0110000XXX	32	180000h–187FFFh
	SA1-56	0	1	0110001XXX	32	188000h–18FFFFh
	SA1-57	0	1	0110010XXX	32	190000h–197FFFh
	SA1-58	0	1	0110011XXX	32	198000h–19FFFFh
	SA1-59	0	1	0110100XXX	32	1A0000h–1A7FFFh
	SA1-60	0	1	0110101XXX	32	1A8000h–1AFFFFh
	SA1-61	0	1	0110110XXX	32	1B0000h–1B7FFFh
	SA1-62	0	1	0110111XXX	32	1B8000h–1BFFFFh
	SA1-63	0	1	0111000XXX	32	1C0000h–1C7FFFh
	SA1-64	0	1	0111001XXX	32	1C8000h–1CFFFFh
	SA1-65	0	1	0111010XXX	32	1D0000h–1D7FFFh
	SA1-66	0	1	0111011XXX	32	1D8000h–1DFFFFh
	SA1-67	0	1	0111100XXX	32	1E0000h–1E7FFFh
	SA1-68	0	1	0111101XXX	32	1E8000h–1EFFFFh
	SA1-69	0	1	0111110XXX	32	1F0000h–1F7FFFh
	SA1-70	0	1	0111111XXX	32	1F8000h–1FFFFFh
	SA1-71	0	1	1000000XXX	32	200000h–207FFFh
	SA1-72	0	1	1000001XXX	32	208000h–20FFFFh
	SA1-73	0	1	1000010XXX	32	210000h–217FFFh
	SA1-74	0	1	1000011XXX	32	218000h–21FFFFh
	SA1-75	0	1	1000100XXX	32	220000h–227FFFh
	SA1-76	0	1	1000101XXX	32	228000h–22FFFFh
	SA1-77	0	1	1000110XXX	32	230000h–237FFFh
	SA1-78	0	1	1000111XXX	32	238000h–23FFFFh
	SA1-79	0	1	1001000XXX	32	240000h–247FFFh
	SA1-80	0	1	1001001XXX	32	248000h–24FFFFh
	SA1-81	0	1	1001010XXX	32	250000h–257FFFh
	SA1-82	0	1	1001011XXX	32	258000h–25FFFFh

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Table 3.   S29PLI29J Sector Architecture (Sheet 3 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
	SA1-83	0	1	1001100XXX	32	260000h–267FFFFh
	SA1-84	0	1	1001101XXX	32	268000h–26FFFFh
	SA1-85	0	1	1001110XXX	32	270000h–277FFFFh
	SA1-86	0	1	1001111XXX	32	278000h–27FFFFh
	SA1-87	0	1	1010000XXX	32	280000h–287FFFFh
	SA1-88	0	1	1010001XXX	32	288000h–28FFFFh
	SA1-89	0	1	1010010XXX	32	290000h–297FFFFh
	SA1-90	0	1	1010011XXX	32	298000h–29FFFFh
	SA1-91	0	1	1010100XXX	32	2A0000h–2A7FFFh
	SA1-92	0	1	1010101XXX	32	2A8000h–2AFFFFh
	SA1-93	0	1	1010110XXX	32	2B0000h–2B7FFFh
	SA1-94	0	1	1010111XXX	32	2B8000h–2BFFFFh
	SA1-95	0	1	1011000XXX	32	2C0000h–2C7FFFh
	SA1-96	0	1	1011001XXX	32	2C8000h–2CFFFFh
	SA1-97	0	1	1011010XXX	32	2D0000h–2D7FFFh
	SA1-98	0	1	1011011XXX	32	2D8000h–2DFFFFh
	SA1-99	0	1	1011100XXX	32	2E0000h–2E7FFFh
	SA1-100	0	1	1011101XXX	32	2E8000h–2EFFFFh
	SA1-101	0	1	1011110XXX	32	2F0000h–2F7FFFh
	SA1-102	0	1	1011111XXX	32	2F8000h–2FFFFFh
Bank 1B	SA1-103	0	1	1100000XXX	32	300000h–307FFFFh
	SA1-104	0	1	1100001XXX	32	308000h–30FFFFh
	SA1-105	0	1	1100010XXX	32	310000h–317FFFFh
	SA1-106	0	1	1100011XXX	32	318000h–31FFFFh
	SA1-107	0	1	1100100XXX	32	320000h–327FFFFh
	SA1-108	0	1	1100101XXX	32	328000h–32FFFFh
	SA1-109	0	1	1100110XXX	32	330000h–337FFFFh
	SA1-110	0	1	1100111XXX	32	338000h–33FFFFh
	SA1-111	0	1	1101000XXX	32	340000h–347FFFFh
	SA1-112	0	1	1101001XXX	32	348000h–34FFFFh
	SA1-113	0	1	1101010XXX	32	350000h–357FFFFh
	SA1-114	0	1	1101011XXX	32	358000h–35FFFFh
	SA1-115	0	1	1101100XXX	32	360000h–367FFFFh
	SA1-116	0	1	1101101XXX	32	368000h–36FFFFh
	SA1-117	0	1	1101110XXX	32	370000h–377FFFFh
	SA1-118	0	1	1101111XXX	32	378000h–37FFFFh
	SA1-119	0	1	1110000XXX	32	380000h–387FFFFh
	SA1-120	0	1	1110001XXX	32	388000h–38FFFFh
	SA1-121	0	1	1110010XXX	32	390000h–397FFFFh
	SA1-122	0	1	1110011XXX	32	398000h–39FFFFh
	SA1-123	0	1	1110100XXX	32	3A0000h–3A7FFFh
	SA1-124	0	1	1110101XXX	32	3A8000h–3AFFFFh
	SA1-125	0	1	1110110XXX	32	3B0000h–3B7FFFh
	SA1-126	0	1	1110111XXX	32	3B8000h–3BFFFFh

Table 3.   S29PLI29J Sector Architecture (Sheet 4 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank 1B	SA1-127	0	1	1111000XXX	32	3C0000h–3C7FFFh
	SA1-128	0	1	1111001XXX	32	3C8000h–3CFFFFh
	SA1-129	0	1	1111010XXX	32	3D0000h–3D7FFFh
	SA1-130	0	1	1111011XXX	32	3D8000h–3DFFFFh
	SA1-131	0	1	1111100XXX	32	3E0000h–3E7FFFh
	SA1-132	0	1	1111101XXX	32	3E8000h–3EFFFFh
	SA1-133	0	1	1111110XXX	32	3F0000h–3F7FFFh
	SA1-134	0	1	1111111XXX	32	3F8000h–3FFFFFh
Bank 2A	SA2-0	1	0	0000000XXX	32	000000h–007FFFh
	SA2-1	1	0	0000001XXX	32	008000h–00FFFFh
	SA2-2	1	0	0000010XXX	32	010000h–017FFFh
	SA2-3	1	0	0000011XXX	32	018000h–01FFFFh
	SA2-4	1	0	0000100XXX	32	020000h–027FFFh
	SA2-5	1	0	0000101XXX	32	028000h–02FFFFh
	SA2-6	1	0	0000110XXX	32	030000h–037FFFh
	SA2-7	1	0	0000111XXX	32	038000h–03FFFFh
	SA2-8	1	0	0001000XXX	32	040000h–047FFFh
	SA2-9	1	0	0001001XXX	32	048000h–04FFFFh
	SA2-10	1	0	0001010XXX	32	050000h–057FFFh
	SA2-11	1	0	0001011XXX	32	058000h–05FFFFh
	SA2-12	1	0	0001100XXX	32	060000h–067FFFh
	SA2-13	1	0	0001101XXX	32	068000h–06FFFFh
	SA2-14	1	0	0001110XXX	32	070000h–077FFFh
	SA2-15	1	0	0001111XXX	32	078000h–07FFFFh
	SA2-16	1	0	0010000XXX	32	080000h–087FFFh
	SA2-17	1	0	0010001XXX	32	088000h–08FFFFh
	SA2-18	1	0	0010010XXX	32	090000h–097FFFh
	SA2-19	1	0	0010011XXX	32	098000h–09FFFFh
	SA2-20	1	0	0010100XXX	32	0A0000h–0A7FFFh
	SA2-21	1	0	0010101XXX	32	0A8000h–0AFFFFh
	SA2-22	1	0	0010110XXX	32	0B0000h–0B7FFFh
	SA2-23	1	0	0010111XXX	32	0B8000h–0BFFFFh
	SA2-24	1	0	0011000XXX	32	0C0000h–0C7FFFh
	SA2-25	1	0	0011001XXX	32	0C8000h–0CFFFFh
	SA2-26	1	0	0011010XXX	32	0D0000h–0D7FFFh
	SA2-27	1	0	0011011XXX	32	0D8000h–0DFFFFh
	SA2-28	1	0	0011100XXX	32	0E0000h–0E7FFFh
	SA2-29	1	0	0011101XXX	32	0E8000h–0EFFFFh
	SA2-30	1	0	0011110XXX	32	0F0000h–0F7FFFh
	SA2-31	1	0	0011111XXX	32	0F8000h–0FFFFFh
	SA2-32	1	0	0100000XXX	32	100000h–107FFFh
	SA2-33	1	0	0100001XXX	32	108000h–10FFFFh
	SA2-34	1	0	0100010XXX	32	110000h–117FFFh
	SA2-35	1	0	0100011XXX	32	118000h–11FFFFh

Table 3.   S29PLI29J Sector Architecture (Sheet 5 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank 2A	SA2-36	1	0	0100100XXX	32	120000h–127FFFh
	SA2-37	1	0	0100101XXX	32	128000h–12FFFFh
	SA2-38	1	0	0100110XXX	32	130000h–137FFFh
	SA2-39	1	0	0100111XXX	32	138000h–13FFFFh
	SA2-40	1	0	0101000XXX	32	140000h–147FFFh
	SA2-41	1	0	0101001XXX	32	148000h–14FFFFh
	SA2-42	1	0	0101010XXX	32	150000h–157FFFh
	SA2-43	1	0	0101011XXX	32	158000h–15FFFFh
Bank 2A	SA2-44	1	0	0101100XXX	32	160000h–167FFFh
	SA2-45	1	0	0101101XXX	32	168000h–16FFFFh
	SA2-46	1	0	0101110XXX	32	170000h–177FFFh
	SA2-47	1	0	0101111XXX	32	178000h–17FFFFh
	SA2-48	1	0	0110000XXX	32	180000h–187FFFh
	SA2-49	1	0	0110001XXX	32	188000h–18FFFFh
	SA2-50	1	0	0110010XXX	32	190000h–197FFFh
	SA2-51	1	0	0110011XXX	32	198000h–19FFFFh
	SA2-52	1	0	0110100XXX	32	1A0000h–1A7FFFh
	SA2-53	1	0	0110101XXX	32	1A8000h–1AFFFFh
	SA2-54	1	0	0110110XXX	32	1B0000h–1B7FFFh
	SA2-55	1	0	0110111XXX	32	1B8000h–1BFFFFh
	SA2-56	1	0	0111000XXX	32	1C0000h–1C7FFFh
	SA2-57	1	0	0111001XXX	32	1C8000h–1CFFFFh
	SA2-58	1	0	0111010XXX	32	1D0000h–1D7FFFh
	SA2-59	1	0	0111011XXX	32	1D8000h–1DFFFFh
	SA2-60	1	0	0111100XXX	32	1E0000h–1E7FFFh
	SA2-61	1	0	0111101XXX	32	1E8000h–1EFFFFh
	SA2-62	1	0	0111110XXX	32	1F0000h–1F7FFFh
	SA2-63	1	0	0111111XXX	32	1F8000h–1FFFFFh
	SA2-64	1	0	1000000XXX	32	200000h–207FFFh
	SA2-65	1	0	1000001XXX	32	208000h–20FFFFh
	SA2-66	1	0	1000010XXX	32	210000h–217FFFh
	SA2-67	1	0	1000011XXX	32	218000h–21FFFFh
	SA2-68	1	0	1000100XXX	32	220000h–227FFFh
	SA2-69	1	0	1000101XXX	32	228000h–22FFFFh
	SA2-70	1	0	1000110XXX	32	230000h–237FFFh
	SA2-71	1	0	1000111XXX	32	238000h–23FFFFh
	SA2-72	1	0	1001000XXX	32	240000h–247FFFh
	SA2-73	1	0	1001001XXX	32	248000h–24FFFFh
	SA2-74	1	0	1001010XXX	32	250000h–257FFFh
	SA2-75	1	0	1001011XXX	32	258000h–25FFFFh
	SA2-76	1	0	1001100XXX	32	260000h–267FFFh
	SA2-77	1	0	1001101XXX	32	268000h–26FFFFh
	SA2-78	1	0	1001110XXX	32	270000h–277FFFh
	SA2-79	1	0	1001111XXX	32	278000h–27FFFFh

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Table 3. S29PLI29J Sector Architecture (Sheet 6 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank 2A	SA2-80	1	0	1010000XXX	32	280000h–287FFFh
	SA2-81	1	0	1010001XXX	32	288000h–28FFFFh
	SA2-82	1	0	1010010XXX	32	290000h–297FFFh
	SA2-83	1	0	1010011XXX	32	298000h–29FFFFh
	SA2-84	1	0	1010100XXX	32	2A0000h–2A7FFFh
	SA2-85	1	0	1010101XXX	32	2A8000h–2AFFFFh
	SA2-86	1	0	1010110XXX	32	2B0000h–2B7FFFh
	SA2-87	1	0	1010111XXX	32	2B8000h–2BFFFFh
	SA2-88	1	0	1011000XXX	32	2C0000h–2C7FFFh
	SA2-89	1	0	1011001XXX	32	2C8000h–2CFFFFh
	SA2-90	1	0	1011010XXX	32	2D0000h–2D7FFFh
	SA2-91	1	0	1011011XXX	32	2D8000h–2DFFFFh
	SA2-92	1	0	1011100XXX	32	2E0000h–2E7FFFh
	SA2-93	1	0	1011101XXX	32	2E8000h–2EFFFFh
	SA2-94	1	0	1011110XXX	32	2F0000h–2F7FFFh
	SA2-95	1	0	1011111XXX	32	2F8000h–2FFFFFh
Bank 2B	SA2-96	1	0	1100000XXX	32	300000h–307FFFh
	SA2-97	1	0	1100001XXX	32	308000h–30FFFFh
	SA2-98	1	0	1100010XXX	32	310000h–317FFFh
	SA2-99	1	0	1100011XXX	32	318000h–31FFFFh
	SA2-100	1	0	1100100XXX	32	320000h–327FFFh
	SA2-101	1	0	1100101XXX	32	328000h–32FFFFh
	SA2-102	1	0	1100110XXX	32	330000h–337FFFh
	SA2-103	1	0	1100111XXX	32	338000h–33FFFFh
	SA2-104	1	0	1101000XXX	32	340000h–347FFFh
	SA2-105	1	0	1101001XXX	32	348000h–34FFFFh
	SA2-106	1	0	1101010XXX	32	350000h–357FFFh
	SA2-107	1	0	1101011XXX	32	358000h–35FFFFh
	SA2-108	1	0	1101100XXX	32	360000h–367FFFh
	SA2-109	1	0	1101101XXX	32	368000h–36FFFFh
	SA2-110	1	0	1101110XXX	32	370000h–377FFFh
	SA2-111	1	0	1101111XXX	32	378000h–37FFFFh
	SA2-112	1	0	1110000XXX	32	380000h–387FFFh
	SA2-113	1	0	1110001XXX	32	388000h–38FFFFh
	SA2-114	1	0	1110010XXX	32	390000h–397FFFh
	SA2-115	1	0	1110011XXX	32	398000h–39FFFFh
	SA2-116	1	0	1110100XXX	32	3A0000h–3A7FFFh
	SA2-117	1	0	1110101XXX	32	3A8000h–3AFFFFh
	SA2-118	1	0	1110110XXX	32	3B0000h–3B7FFFh
	SA2-119	1	0	1110111XXX	32	3B8000h–3BFFFFh
	SA2-120	1	0	1111000XXX	32	3C0000h–3C7FFFh
	SA2-121	1	0	1111001XXX	32	3C8000h–3CFFFFh
	SA2-122	1	0	1111010XXX	32	3D0000h–3D7FFFh
	SA2-123	1	0	1111011XXX	32	3D8000h–3DFFFFh

Table 3. S29PLI29J Sector Architecture (Sheet 7 of 7)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xl6)
Bank 2B	SA2-124	1	0	1111100XXX	32	3E0000h–3E7FFFh
	SA2-125	1	0	1111101XXX	32	3E8000h–3EFFFFh
	SA2-126	1	0	1111110XXX	32	3F0000h–3F7FFFh
	SA2-127	1	0	1111111000	4	3F8000h–3F8FFFh
	SA2-128	1	0	1111111001	4	3F9000h–3F9FFFh
	SA2-129	1	0	1111111010	4	3FA000h–3FAFFFh
	SA2-130	1	0	1111111011	4	3FB000h–3FBFFFh
	SA2-131	1	0	1111111100	4	3FC000h–3FCFFFh
	SA2-132	1	0	1111111101	4	3FD000h–3FDFFFh
	SA2-133	1	0	1111111110	4	3FE000h–3FEFFFh
	SA2-134	1	0	1111111111	4	3FF000h–3FFFFFh

Table 4. Secured Silicon Sector Addresses

	Sector Size	Address Range
Factory-Locked Area	64 words	000000h-00003Fh
Customer-Lockable Area	64 words	000040h-00007Fh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 5. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 12. **Note:** *If a Bank Address (BA) (on address bits A21–A19) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12. This method does not require V_{ID}. See "Autoselect Command Sequence" on page 46 for more information.

Table 5.   Autoselect Codes for PLI29J

Description		CE1#	CE2#	OE#	WE#	A21 to A12	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: Spansion products		L	H	L	H	X	X	V$_{ID}$	X	L	L	X	L	L	L	L	0001h
		H	L														
Device ID	Read Cycle 1	L	H	L	H	X	X	V$_{ID}$	X	L	L	L	L	L	L	H	227Eh
		H	L														
	Read Cycle 2	L	H										H	H	H	L	2221h
		H	L														
	Read Cycle 3	L	H										H	H	H	H	2200h
		H	L														
Sector Protection Verification		L	H	L	H	SA	X	V$_{ID}$	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
		H	L														
Secured Silicon Indicator Bit (DQ7, DQ6)		L	H	L	H	X	X	V$_{ID}$	X	X	L	X	L	L	H	H	DQ7=1 (factory locked), DQ6=1 (factory and customer locked)
		H	L														

Legend: L = Logic Low = V$_{IL}$, H = Logic High = V$_{IH}$, BA = Bank Address, SA = Sector Address, X = Don't care.

Note: The autoselect codes may also be accessed in-system via command sequences

Table 6.   PLI29J Boot Sector/Sector Block Addresses for Protection/Unprotection

CEI# Control			CE2# Control		
Sector Group	A2I-I2	Sector/Sector Block Size	Sector Group	A2I-I2	Sector/Sector Block Size
SA1-0	0000000000	4 Kwords	SA2-0–SA2-3	00000XXXXX	128 (4x32) Kwords
SA1-1	0000000001	4 Kwords	SA2-4–SA2-7	00001XXXXX	128 (4x32) Kwords
SA1-2	0000000010	4 Kwords	SA2-8–SA2-11	00010XXXXX	128 (4x32) Kwords
SA1-3	0000000011	4 Kwords	SA2-12–SA2-15	00011XXXXX	128 (4x32) Kwords
SA1-4	0000000100	4 Kwords	SA2-16–SA2-19	00100XXXXX	128 (4x32) Kwords
SA1-5	0000000101	4 Kwords	SA2-20–SA2-23	00101XXXXX	128 (4x32) Kwords
SA1-6	0000000110	4 Kwords	SA2-24–SA2-27	00110XXXXX	128 (4x32) Kwords
SA1-7	0000000111	4 Kwords	SA2-28–SA2-31	00111XXXXX	128 (4x32) Kwords
SA1-8	0000001XXX	32 Kwords	SA2-32–SA2-35	01000XXXXX	128 (4x32) Kwords
SA1-9	0000010XXX	32 Kwords	SA2-36–SA2-39	01001XXXXX	128 (4x32) Kwords
SA1-10	0000011XXX	32 Kwords	SA2-40–SA2-43	01010XXXXX	128 (4x32) Kwords
SA1-11 - SA1-14	00001XXXXX	128 (4x32) Kwords	SA2-44–SA2-47	01011XXXXX	128 (4x32) Kwords
SA1-15 - SA1-18	00010XXXXX	128 (4x32) Kwords	SA2-48–SA2-51	01100XXXXX	128 (4x32) Kwords
SA1-19 - SA1-22	00011XXXXX	128 (4x32) Kwords	SA2-52–SA2-55	01101XXXXX	128 (4x32) Kwords
SA1-23 - SA1-26	00100XXXXX	128 (4x32) Kwords	SA2-56–SA2-59	01110XXXXX	128 (4x32) Kwords
SA1-27 - SA1-30	00101XXXXX	128 (4x32) Kwords	SA2-60–SA2-63	01111XXXXX	128 (4x32) Kwords
SA1-31 - SA1-34	00110XXXXX	128 (4x32) Kwords	SA2-64–SA2-67	10000XXXXX	128 (4x32) Kwords
SA1-35 - SA1-38	00111XXXXX	128 (4x32) Kwords	SA2-68–SA2-71	10001XXXXX	128 (4x32) Kwords
SA1-39 - SA1-42	01000XXXXX	128 (4x32) Kwords	SA2-72–SA2-75	10010XXXXX	128 (4x32) Kwords
SA1-43 - SA1-46	01001XXXXX	128 (4x32) Kwords	SA2-76–SA2-79	10011XXXXX	128 (4x32) Kwords
SA1-47 - SA1-50	01010XXXXX	128 (4x32) Kwords	SA2-80–SA2-83	10100XXXXX	128 (4x32) Kwords
SA1-51 - SA1-54	01011XXXXX	128 (4x32) Kwords	SA2-84–SA2-87	10101XXXXX	128 (4x32) Kwords
SA1-55 - SA1-58	01100XXXXX	128 (4x32) Kwords	SA2-88–SA2-91	10110XXXXX	128 (4x32) Kwords
SA1-59 - SA1-62	01101XXXXX	128 (4x32) Kwords	SA2-92–SA2-95	10111XXXXX	128 (4x32) Kwords
SA1-63 - SA1-66	01110XXXXX	128 (4x32) Kwords	SA2-96–SA2-99	11000XXXXX	128 (4x32) Kwords
SA1-67 - SA1-70	01111XXXXX	128 (4x32) Kwords	SA2-100–SA2-103	11001XXXXX	128 (4x32) Kwords
SA1-71 - SA1-74	10000XXXXX	128 (4x32) Kwords	SA2-104–SA2-107	11010XXXXX	128 (4x32) Kwords
SA1-75 - SA1-78	10001XXXXX	128 (4x32) Kwords	SA2-108–SA2-111	11011XXXXX	128 (4x32) Kwords
SA1-79 - SA1-82	10010XXXXX	128 (4x32) Kwords	SA2-112–SA2-115	11100XXXXX	128 (4x32) Kwords
SA1-83 - SA1-86	10011XXXXX	128 (4x32) Kwords	SA2-116–SA2-119	11101XXXXX	128 (4x32) Kwords
SA1-87 - SA1-90	10100XXXXX	128 (4x32) Kwords	SA2-120–SA2-123	11110XXXXX	128 (4x32) Kwords
SA1-91 - SA1-94	10101XXXXX	128 (4x32) Kwords	SA2-124	1111100XXX	32 Kwords
SA1-95 - SA1-98	10110XXXXX	128 (4x32) Kwords	SA2-125	1111101XXX	32 Kwords
SA1-99 - SA1-102	10111XXXXX	128 (4x32) Kwords	SA2-126	1111110XXX	32 Kwords
SA1-103 - SA1-106	11000XXXXX	128 (4x32) Kwords	SA2-127	1111111000	4 Kwords
SA1-107 - SA1-110	11001XXXXX	128 (4x32) Kwords	SA2-128	1111111001	4 Kwords
SA1-111 - SA1-114	11010XXXXX	128 (4x32) Kwords	SA2-129	1111111010	4 Kwords
SA1-115 - SA1-118	11011XXXXX	128 (4x32) Kwords	SA2-130	1111111011	4 Kwords
SA1-119 - SA1-122	11100XXXXX	128 (4x32) Kwords	SA2-131	1111111100	4 Kwords
SA1-123 - SA1-126	11101XXXXX	128 (4x32) Kwords	SA2-132	1111111101	4 Kwords
SA1-127 - SA1-130	11110XXXXX	128 (4x32) Kwords	SA2-133	1111111110	4 Kwords
SA1-131 - SA1-134	11111XXXXX	128 (4x32) Kwords	SA2-134	1111111111	4 Kwords

Selecting a Sector Protection Mode

The device is shipped with all sectors unprotected. Optional Spansion programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See "Secured Silicon Sector Addresses" on page 29 for details.

Table 7.   Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	Protected—PPB and DYB are changeable
1	1	0	Protected—PPB and DYB are changeable
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	Protected—PPB not changeable, DYB is changeable
1	1	1	Protected—PPB not changeable, DYB is changeable

Sector Protection

The PL129J features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors SA1-133, SA1-134, SA2-0 and SA2-1.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method is used. If the Persistent Sector Protection method is desired, programming the Persistent Sector Protection Mode Locking Bit permanently sets the device to the Persistent Sector Protection mode. If the Password Sector Protection method is desired, programming the Password Mode Locking Bit permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set. One of the two modes must be selected when the device is first

programmed. This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Optional Spansion programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous flash devices. This new method provides three different sector protection states:

- Persistently Locked—The sector is protected and cannot be changed.
- Dynamically Locked—The sector is protected and can be changed by a simple command.
- Unlocked—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of "bits" are used:

- Persistent Protection Bit
- Persistent Protection Bit Lock
- Persistent Sector Protection Mode Locking Bit

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of

the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs are set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. These states are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because the PPBs are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors SA1-133, SA1-134, SA2-0 and SA2-1. When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently protect a given sector or sector group, the PPBs associated with that sector need to be set to "1". Once all PPBs are programmed to the desired settings, the PPB Lock should be set to "1". Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock "freezes" the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = VIL.

Table 17 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device. There is an alternative means of reading the protection status. Take RESET# to VIL and hold WE# at VIH.(The high voltage A9 Autoselect Mode also works for reading the status of the PPBs). Scanning the addresses (A18–A11) while (A6, A1, A0) = (0, 1, 0) produces a logical '1" code at device output DQ0 for a protected sector or a "0" for an unprotected sector. In this mode, the other addresses are don't cares. Address location with A1 = VIL are reserved for autoselect manufacturer and device codes.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the locked state, rather than cleared to the unlocked state.

The only means to clear the PPB Lock bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Advance Information

SPANSION™

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.

Disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there is not any way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the upper two and lower two sectors(PL127J: 0, 1, 268, and 269, PL064J: 0, 1, 140, and 141, PL032J: 0, 1, 76, and 77, PL129J: SA1-133, SA1-134,SA2-0 and SA2-1) without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed method, "High Voltage Sector Protection" on page 37.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts the upper two and lower two sectors to whether they were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in "High Voltage Sector Protection" on page 37.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

Sector Protect Algorithm:

START → PLSCNT = 1 → RESET# = V_{ID} → Wait 4 µs → First Write Cycle = 60h?

No → Temporary Sector Unprotect Mode

Yes → Set up sector address → Sector Protect: Write 60h to sector address with A7-A0 = 00000010 → Wait 100 µs → Verify Sector Protect: Write 40h to sector address with A7-A0 = 00000010 → Read from sector address with A7-A0 = 00000010 → Data = 01h?

No → PLSCNT = 25?
- No → Increment PLSCNT → Sector Protect: Write 60h...
- Yes → Remove V_{ID} from RESET# → Write reset command → Sector Protect complete → Device failed

Data = 01h? Yes → Protect another sector?
- Yes → Reset PLSCNT = 1 → Set up sector address
- No → Remove V_{ID} from RESET# → Write reset command → Sector Protect complete

Sector Protect Algorithm

Protect all sectors: The indicated portion of the sector protect algorithm must be performed for all unprotected sectors prior to issuing the first sector unprotect address

Sector Unprotect Algorithm:

START → PLSCNT = 1 → RESET# = V_{ID} → Wait 4 µs → First Write Cycle = 60h?

No → Temporary Sector Unprotect Mode

Yes → All sectors protected?
- No → Set up sector address (protect all sectors loop)
- Yes → Set up first sector address → Sector Unprotect: Write 60h to sector address with A7-A0 = 01000010 → Wait 1.2 ms → Verify Sector Unprotect: Write 40h to sector address with A7-A0 = 00000010 → Read from sector address with A7-A0 = 00000010 → Data = 00h?

Data = 00h?
- No → PLSCNT = 1000?
  - No → Increment PLSCNT
  - Yes → Remove V_{ID} from RESET# → Write reset command → Sector Unprotect complete → Device failed
- Yes → Last sector verified?
  - No → Set up next sector address → Verify Sector Unprotect
  - Yes → Remove V_{ID} from RESET# → Write reset command → Sector Unprotect complete

Sector Unprotect Algorithm

Figure I.   In-System Sector Protection/Sector Unprotection Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 21 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.
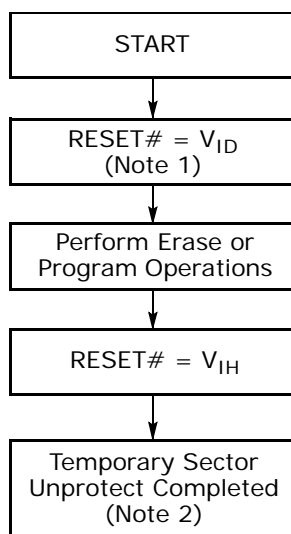
Notes:
1. All protected sectors are unprotected (If WP#/ACC = V_{IL}, upper two and lower two sectors remain protected).
2. All previously protected sectors are protected once again

Figure 2.   Temporary Sector Unprotect Operation

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word Secured Silicon sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The Secured Silicon sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. Indicator bits DQ6 and DQ7 are used to indicate the factory-locked and customer locked status of the part.

The system accesses the Secured Silicon Sector through a command sequence (see "Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence" on page 46). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

Factory-Locked Area (64 words)

The factory-locked area of the Secured Silicon Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The Secured Silicon Sector Factory-locked Indicator Bit (DQ7) is permanently set to a "1". Optional Spansion programming services can program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only FASL can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact your local sales office for details on using Spansion's programming services. Note that the ACC function and unlock bypass modes are not available when the Secured Silicon sector is enabled.

Customer-Lockable Area (64 words)

The customer-lockable area of the Secured Silicon Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The Secured Silicon Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the Secured Silicon Protection Bit Program Command. The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Sector.

The Customer-lockable Secured Silicon Sector area can be protected using one of the following procedures:

■ Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 1, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.

■ To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 3.

Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

Secured Silicon Sector Protection Bits

The Secured Silicon Sector Protection Bits prevent programming of the Secured Silicon Sector memory area. Once set, the Secured Silicon Sector memory area contents are non-modifiable.
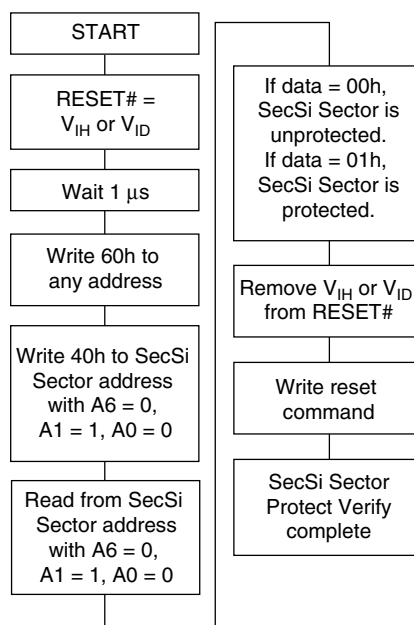
Figure 3.   Secured Silicon Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on OE#, CE1#, CE2# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE1# = CE2# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE1# / CE2# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# (CE1#, CE2# in PL129J) = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 8, Table 9, Table 10, and Table 11. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 8, Table 9, Table 10, and Table 11. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

Table 8.   CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9.   System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N μs
20h	0000h	Typical timeout for Min. size buffer write 2^N μs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10.   Device Geometry Definition

Addresses	Data	Description
27h	0018h (PL129J)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	00FDh (PL129J) 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 11.   Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"

Table II.   Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	**TBD**	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h (PLxxxJ)	Sector Protect/Unprotect scheme 07 = Advanced Sector Protection
4Ah	00E7h (PL129J)	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h (PLxxxJ)	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = Both top and bottom boot with write protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0027h (PL129J)	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0060h (PL129J)	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0060h (PL129J)	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0027h (PL129J)	Bank 4 Region Information X = Number of Sectors in Bank 4

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE# (CE1# / CE2# in PL129J), whichever happens later. All data is latched on the rising edge of WE# or CE# (CE1# / CE2# in PL129J), whichever happens first. See AC Characteristics for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" on page 50 for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See "Reset Command," for more information.

See "Requirements for Reading Array Data" on page 19 in "Device Bus Operations" for more information. The AC Characteristics table provides the read parameters, and Figure 12 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 12 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 12 shows the address and data requirements for both command sequences. Also see, "Secured Silicon Sector Flash Memory Region" on page 39 for further information. *Note:* The ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 12 shows the address and data requirements for the program command sequence. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" on page 56 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. Note that the Secured Silicon Sector, autoselect and CFI functions are unavailable when the Secured Silicon Sector is enabled.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (Table 13)

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 4 illustrates the algorithm for the program operation. See the Erase/Program Operations table in AC Characteristics for parameters, and Figure 14 for timing diagrams.

SPANSION™

START

Write Program
Command Sequence

Data Poll
from System

Embedded
Program
algorithm
in progress

Verify Data?   No

Yes

Increment Address ◄── No   Last Address?

Yes

Programming
Completed
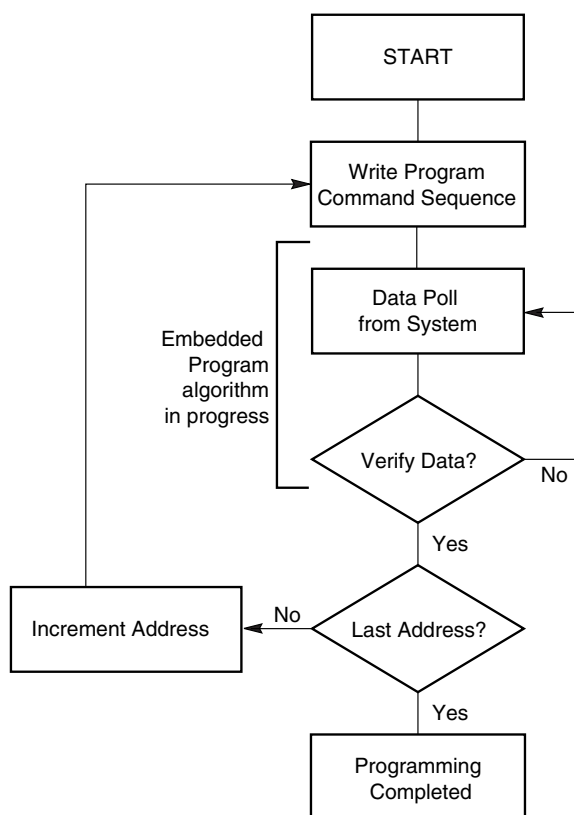
Note: See Table 12 for program command sequence.

Figure 4.   Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is ini-
tiated by writing two unlock cycles, followed by a set-up command. Two
additional unlock write cycles are then followed by the chip erase command,
which in turn invokes the Embedded Erase algorithm. The device does *not* require
the system to preprogram prior to erase. The Embedded Erase algorithm auto-
matically preprograms and verifies the entire memory for an all zero data pattern
prior to electrical erase. The system is not required to provide any controls or tim-
ings during these operations. Table 12 shows the address and data requirements
for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read
mode and addresses are no longer latched. The system can determine the status
of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to "Write Op-
eration Status" on page 56 for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that Se-
cured Silicon Sector, autoselect, and CFI functions are unavailable when a
[program/erase] operation is in progress.* However, note that a **hardware reset**
immediately terminates the erase operation. If that occurs, the chip erase com-
mand sequence should be reinitiated once that bank has returned to reading
array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. See the Erase/Program
Operations tables in AC Characteristics for parameters, and Figure 16 for timing
diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **If any command other than 30h, B0h, F0h is input during the time-out period, the normal operation cannot be guaranteed.** The system must rewrite the command sequence and any additional addresses and commands. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/ erase] operation is in progress.*

The system can monitor DQ3 to determine if the sector erase timer has timed out (See "DQ3: Sector Erase Timer" on page 61). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. See "Write Operation Status" on page 56 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in AC Characteristics for parameters, and Figure 16 for timing diagrams.
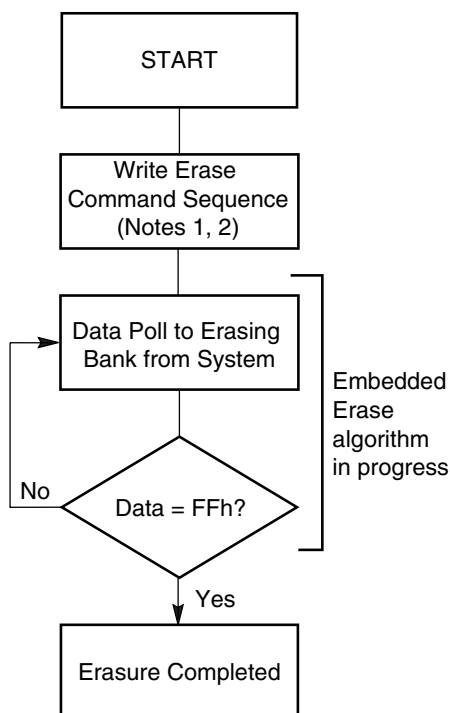
Notes:
1. See *Table 12* for erase command sequence.
2. See *"DQ3: Sector Erase Timer"* on page 61 for information on the sector erase timer.

Figure 5.   Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *"Write Operation Status"* on page 56 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program

operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. See "Write Operation Status" on page 56 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Secured Silicon Sector Addresses" on page 29 and "Autoselect Command Sequence" on page 46 for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don't care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Four Password Program commands are required to program the password. The system must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all ones when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

The Password Verify command is permitted if the Secured Silicon sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1-A0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program

command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. *If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin.* By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

Secured Silicon Sector Protection Bit Program Command

The Secured Silicon Sector Protection Bit Program Command programs the Secured Silicon Sector Protection Bit, which prevents the Secured Silicon sector memory from being cleared. *If the Secured Silicon Sector Protection Bit is verified as programmed without margin, the Secured Silicon Sector Protection Bit Program Command should be reissued to improve program margin.* Exiting the V_{CC}-level Secured Silicon Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command (only in the Persistent Protection Mode).

DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits (Amax–A12) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset.Exiting the DYB Write command is accomplished by writing the Read/Reset command.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through all 64-bit combinations in an attempt

to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

Once the Password Unlock command is entered, the RY/BY# indicates that the device is busy. Approximately 1 µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/BY# is not low or DQ6 does not toggle when read), the next part of the password is written. The system must thus monitor RY/BY# or the status bits to confirm when to write the next portion of the password. Seven cycles are required to successfully clear the PPB Lock Bit.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A22–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

DYB Write Command

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

PPB Lock Bit Set Command

The PPB Lock Bit set command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the

DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

Command

The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

Command Definitions Tables

Table 12.   Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	01				
	Device ID (Note 10)	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA) X0E	(Note 10)	(BA) X0F	(Note 10)
	Secured Silicon Sector Factory Protect (Note 8)	4	555	AA	2AA	55	(BA) 555	90	X03	(Note 8)				
	Sector Group Protect Verify (Note 9)	4	555	AAA	2AA	55	(BA) 555	90	(SA) X02	XX00/ XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 11)		1	BA	B0										
Program/Erase Resume (Note 12)		1	BA	30										
CFI Query (Note 13)		1	55	98										
Accelerated Program (Note 15)		2	XX	A0	PA	PD								
Unlock Bypass Entry (Note 15)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 15)		2	XX	A0	PA	PD								
Unlock Bypass Erase (Note 15)		2	XX	80	XX	10								
Unlock Bypass CFI (Notes 13, 15)		1	XX	98										
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by Amax:A19.

PA = Program Address (Amax:A0). Addresses latch on falling edge of WE# or CE1#/CE2# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE1#/CE2# pulse, whichever happens first.

RA = Read Address (Amax:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (Amax:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. See Table 1 for description of bus operations.

2. All values are in hexadecimal.

3. Shaded cells in table denote read cycles. All other cycles are write operations.

4. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.

5. No unlock or command cycles required when bank is reading array data.

6. The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).

7. Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See *"Autoselect Command Sequence"* on page 46 for more information.

8. The data is DQ6=1 for factory and customer locked and DQ7=1 for factory locked.

9. The data is 00h for an unprotected sector group and 01h for a protected sector group.

10. Device ID must be read across cycles 4, 5, and 6. PL129J (X0Eh = 2221h, X0Fh = 2200h).

11. System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.

12. Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.

13. Command is valid when device is ready to read array data or when device is in autoselect mode.

14. WP#/ACC must be at V_{ID} during the entire operation of command.

15. Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.

Table 13.   Sector Protection Command Definitions

Command (Notes)	Cycles	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
		Bus Cycles (Notes 1-4)
Reset	1	XXX	F0												
Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88								
Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
Secured Silicon Protection Bit Program (Notes 5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD (0)		
Secured Silicon Protection Bit Status	5	555	AA	2AA	55	555	60	OW	48	OW	RD (0)				
Password Program (Notes 5, 7, 8)	4	555	AA	2AA	55	555	38	XX [0-3]	PD [0-3]						
Password Verify (Notes 6, 8, 9)	4	555	AA	2AA	55	555	C8	PWA [0-3]	PWD [0-3]						
Password Unlock (Notes 7, 10, 11)	7	555	AA	2AA	55	555	28	PWA [0]	PWD [0]	PWA [1]	PWD [1]	PWA [2]	PWD [2]	PWA [3]	PWD [3]
PPB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	(SA) WP	68	(SA) WP	48	(SA) WP	RD (0)		
PPB Status	4	555	AA	2AA	55	555	90	(SA) WP	RD (0)						
All PPB Erase (Notes 5, 6, 13, 14)	6	555	AA	2AA	55	555	60	WP	60	(SA)	40	(SA) WP	RD (0)		
PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
PPB Lock Bit Status (Note 15)	4	555	AA	2AA	55	555	58	SA	RD (1)						
DYB Write (Note 7)	4	555	AA	2AA	55	555	48	SA	X1						
DYB Erase (Note 7)	4	555	AA	2AA	55	555	48	SA	X0						
DYB Status (Note 6)	4	555	AA	2AA	55	555	58	SA	RD (0)						
PPMLB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD (0)		
PPMLB Status (Note 5)	5	555	AA	2AA	55	555	60	PL	48	PL	RD (0)				
SPMLB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD (0)		
SPMLB Status (Note 5)	5	555	AA	2AA	55	555	60	SL	48	SL	RD (0)				

Legend:

DYB = Dynamic Protection Bit

OW = Address (A7:A0) is (00011010)

PD[3:0] = Password Data (1 of 4 portions)

PPB = Persistent Protection Bit

PWA = Password Address. A1:A0 selects portion of password.

PWD = Password Data being verified.

PL = Password Protection Mode Lock Address (A7:A0) is (00001010)

RD(0) = Read Data DQ0 for protection indicator bit.

RD(1) = Read Data DQ1 for PPB Lock status.

SA = Sector Address where security command applies. Address bits Amax:A12 uniquely select any sector.

SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)

WP = PPB Address (A7:A0) is (00000010)

X = Don't care

PPMLB = Password Protection Mode Locking Bit

SPMLB = Persistent Protection Mode Locking Bit

Notes:

1. See *Table 1* for description of bus operations.
2. All values are in hexadecimal.
3. Shaded cells in table denote read cycles. All other cycles are write operations.
4. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
5. The reset command returns device to reading array.
6. Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
7. Data is latched on the rising edge of WE#.
8. Entire command sequence must be entered for each portion of password.
9. Command sequence returns FFh if PPMLB is set.
10. The password is written over four consecutive cycles, at addresses 0-3.
11. A 2 µs timeout is required between any two portions of password.
12. A 100 µs timeout is required between cycles 4 and 5.
13. A 1.2 ms timeout is required between cycles 4 and 5.
14. Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.
15. DQ1 = 1 if PPB locked, 0 if unlocked.

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 14 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400 μs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 appears on successive read cycles.

Table 14 shows the outputs for Data# Polling on DQ7. 6 shows the Data# Polling algorithm. Figure 18 in AC Characteristics shows the Data# Polling timing diagram.
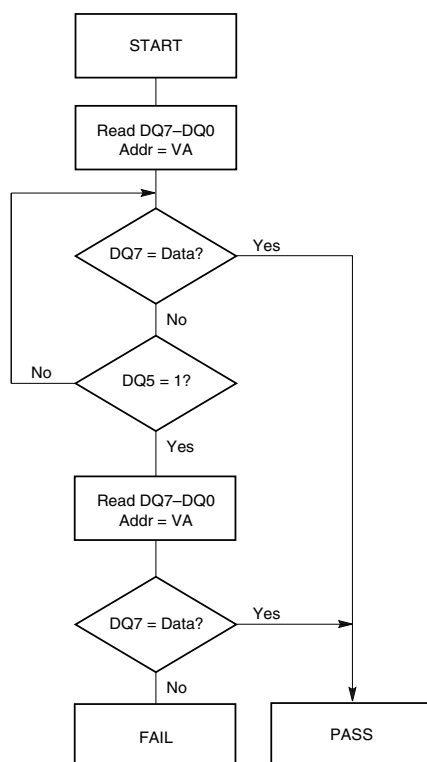
Notes:
1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 6.   Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 14 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see "DQ7: Data# Polling" on page 56).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 μs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 14 shows the outputs for Toggle Bit I on DQ6. Figure 7 shows the toggle bit algorithm. Figure 19 in "Read Operation Timings" shows the toggle bit timing diagrams. Figure 20 shows the differences between DQ2 and DQ6 in graphical form. See also "DQ2: Toggle Bit II".
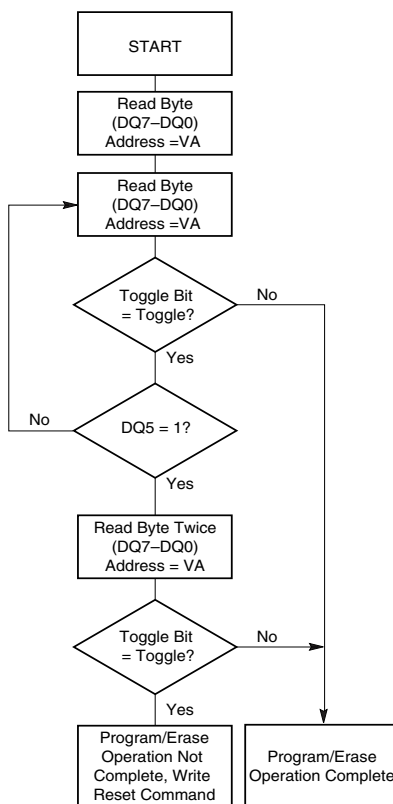

Figure 7.   Toggle Bit Algorithm

Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See* "DQ6: Toggle Bit I" *and* "DQ2: Toggle Bit II" *for more information.*

Figure 7.   Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE1# / CE2# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. See Table 14 to compare outputs for DQ2 and DQ6.

Figure 7 shows the toggle bit algorithm in flowchart form, and the "DQ2: Toggle Bit II" explains the algorithm. See also "DQ6: Toggle Bit I." Figure 19 shows the toggle bit timing diagram. Figure 20 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see "DQ5: Exceeded Timing Limits"). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can**

change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." See also "Sector Erase Command Sequence" on page 49.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device accepts additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 14 shows the status of DQ3 relative to the other status bits.

Table 14. Write Operation Status

Status		DQ7 (Note 2)	DQ6	DQ5 (Note I)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read — Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Erase-Suspend-Read — Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. "DQ5: Exceeded Timing Limits" for more information.

2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

Absolute Maximum Ratings

Storage Temperature Plastic Packages . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . –0.5 V to +4.0 V

A9, OE#, and RESET# (Note 2) . . . . –0.5 V to +13.0 V

WP#/ACC (Note 2) . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3). . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*

2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*

3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

4. *Stresses above those listed under "Absolute Maximum Ratings" may cause perma-nent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute max-imum rating conditions for extended periods may affect device reliability.*
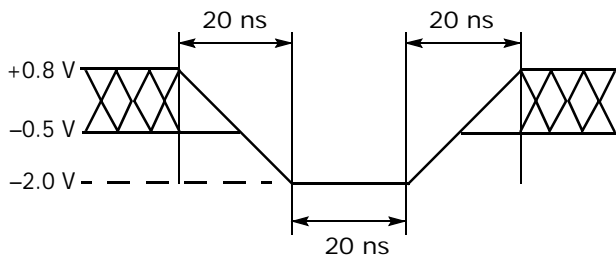
Maximum Negative Overshoot Waveform   Maximum Positive Overshoot Waveform
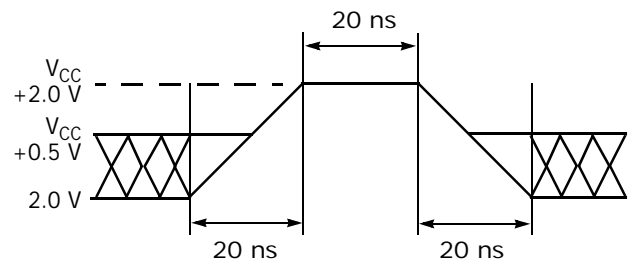
Figure 8.   Maximum Overshoot Waveforms

Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

Industrial (I) Devices

Ambient Temperature (T_A) . . . . −40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . −55°C to +125°C

Supply Voltages

V_{CC} . . . . .2.7–3.6 V

V_{IO} or 2.7–3.6 V

Notes:

For all AC and DC specifications, V_{IO} = V_{CC}; contact your local sales office for other V_{IO} options.

DC Characteristics

Table I5.   CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; $V_{ID} = 12.5$ V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; $V_{ID} = 12.5$ V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	OE# = V_{IH}, $V_{CC} = V_{CC\ max}$ (Note 1)	5 MHz		20	30	mA
			10 MHz		45	55	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	OE# = V_{IH}, WE# = V_{IL}			15	25	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET#, WP#/ACC $= V_{IO} \pm 0.3$ V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = $V_{SS} \pm 0.3$ V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{IO} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	OE# = V_{IH}			17	25	mA
I_{CC9}	V_{CC} Active Page Read Current (Note 2)	OE# = V_{IH}, 8 word Page Read			10	15	mA
V_{IL}	Input Low Voltage	$V_{IO} = 2.7$–3.6 V		−0.5		0.8	V
V_{IH}	Input High Voltage	$V_{IO} = 2.7$–3.6 V		2.0		$V_{CC}+0.3$	V
V_{HH}	Voltage for ACC Program Acceleration	$V_{CC} = 3.0$ V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	$V_{CC} = 3.0$ V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.0$ mA, $V_{CC} = V_{CC\ min}$, $V_{IO} = 2.7$–3.6 V				0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC\ min}$, $V_{IO} = 2.7$–3.6 V		2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 5 mA/MHz, with OE# at V_{IH}.*

2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*

3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*

4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 1 mA.*

5. *Not 100% tested.*

6. *In S29PL129J there are two CE# (CE1#, CE2#).*

7. *Valid CE1#/CE2# conditions: (CE1# = V_{IL}, CE2# = V_{IH},) or (CE1# = V_{IH}, CE2# = V_{IL}) or (CE1# = V_{IH}, CE2# = V_{IH})*

AC Characteristics

Test Conditions
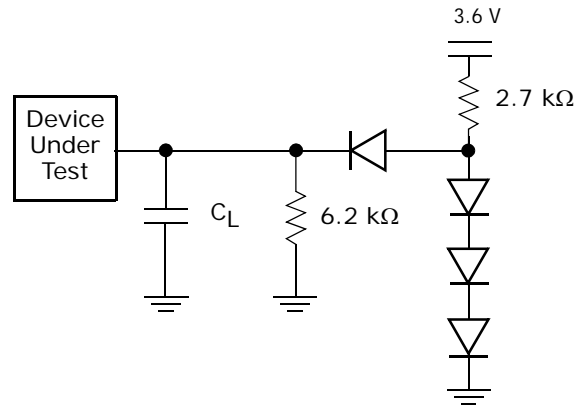
V$_{IO}$ = 3.0 V

Note: Diodes are IN3064 or equivalent

Figure 9.   Test Setups

Table 16.   Test Specifications

Test Condition		All Speeds	Unit
Output Load		1 TTL gate	
Output Load Capacitance, C$_L$ (including jig capacitance)		30	pF
Input Rise and Fall Times	V$_{IO}$ = 3.0 V	5	ns
Input Pulse Levels	V$_{IO}$ = 3.0 V	0.0–3.0	V
Input timing measurement reference levels		V$_{IO}$/2	V
Output timing measurement reference levels		V$_{IO}$/2	V

Switching Waveforms

Table 17.   Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

VIO

In   VIO/2   ⟨─ Measurement Level ─⟩   VIO/2   Output

0.0 V
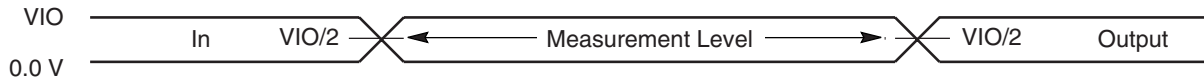
Figure 10.   Input Waveforms and Measurement Levels

VCC RampRate

All DC characteristics are specified for a V_{CC} ramp rate > 1V/100 µs and V_{CC} >=V_{CCQ} - 100 mV. If the V_{CC} ramp rate is < 1V/100 µs, a hardware reset required. +
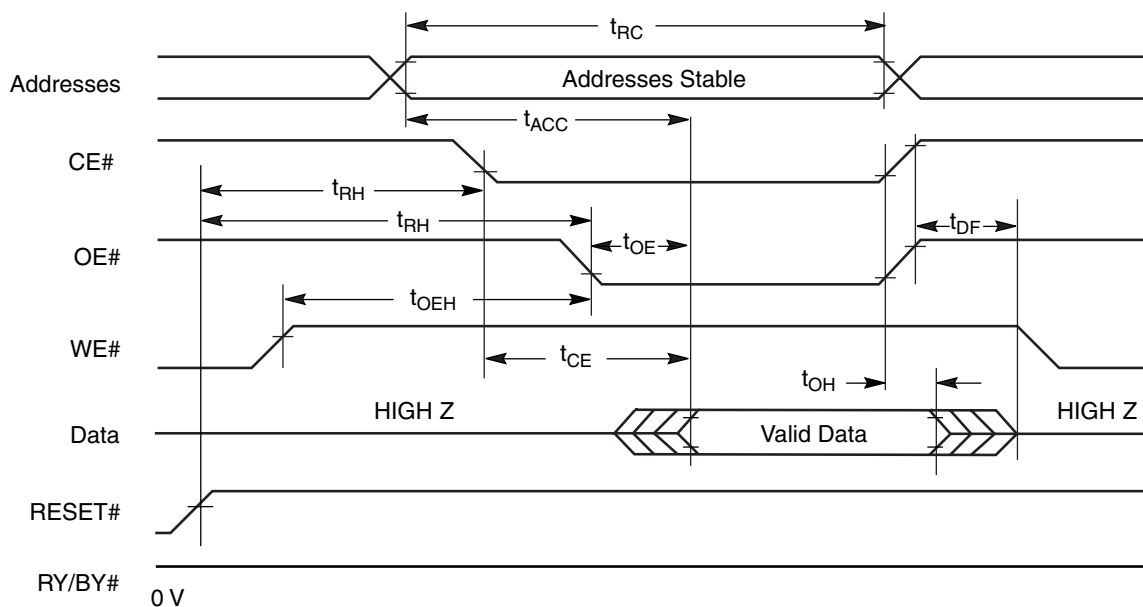
Read Operations

Table 18.   Read-Only Operations

Parameter						Speed Options				
JEDEC	Std.	Description	Test Setup			55	60	65	70	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	55	60	65	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}		Max	55	60	65	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}		Max	55	60	65	70	ns
	t_{PACC}	Page Access Time			Max	20	25	25	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	20	25	30		ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 3)			Max	16				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	16				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 3)			Min	5				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns

Notes:

1. Not 100% tested.

2. See Figure 9 and Table 16 for test specifications

3. Measurements performed by placing a 50 ohm termination on the data pin with a bias of V_{CC} /2. The time from OE# high to the data bus driven to V_{CC} /2 is taken as t_{DF}.

4. S29PL129J has two CE# (CE1#, CE2#).

5. Valid CE1# / CE2# conditions: (CE1# = V_{IL},CE2# = V_{IH}) or (CE1# = V_{IH},CE2# = V_{IL}) or (CE1# = V_{IH}, CE2# = V_{IH})

6. Valid CE1# / CE2# transitions: (CE1# = V_{IL},CE2# = V_{IH}) or (CE1# = V_{IH},CE2# = V_{IL}) to (CE1# = CE2# = V_{IH})

7. Valid CE1# / CE2# transitions: (CE1# = CE2# = V_{IH}) to (CE1# = V_{IL},CE2# = V_{IH}) or (CE1# = V_{IH},CE2# = V_{IL})

8. For 70pF Output Load Capacitance, 2 ns is added to the above t_{ACC},t_{CE},t_{PACC},t_{OE} values for all speed grades

Notes:
1. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
2. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#

Figure I1.   Read Operation Timings
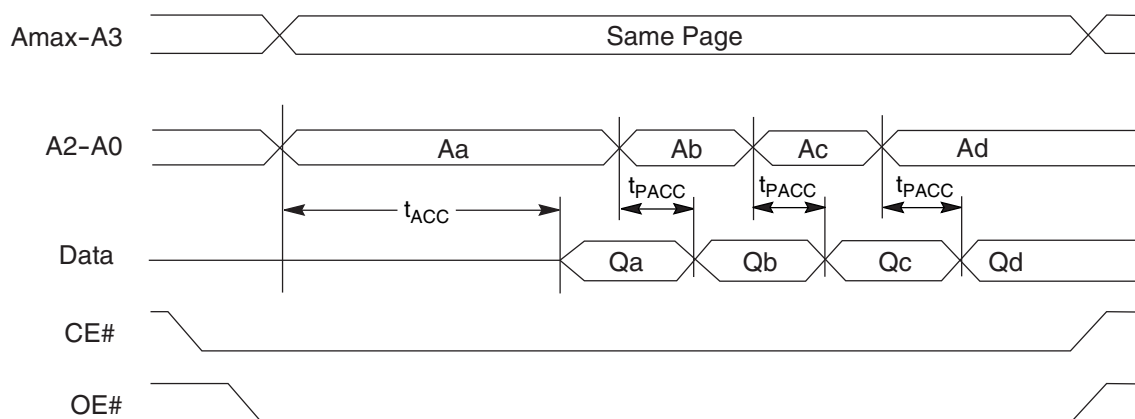
Notes:
1. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
2. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#

Figure I2.   Page Read Operation Timings

Reset

Table I9.   Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: Not 100% tested.

Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms

Notes:
1. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
2. S29PL129J - There are two CE# (CE1#, CE2#). In the below waveform CE# = CE1# or CE2#
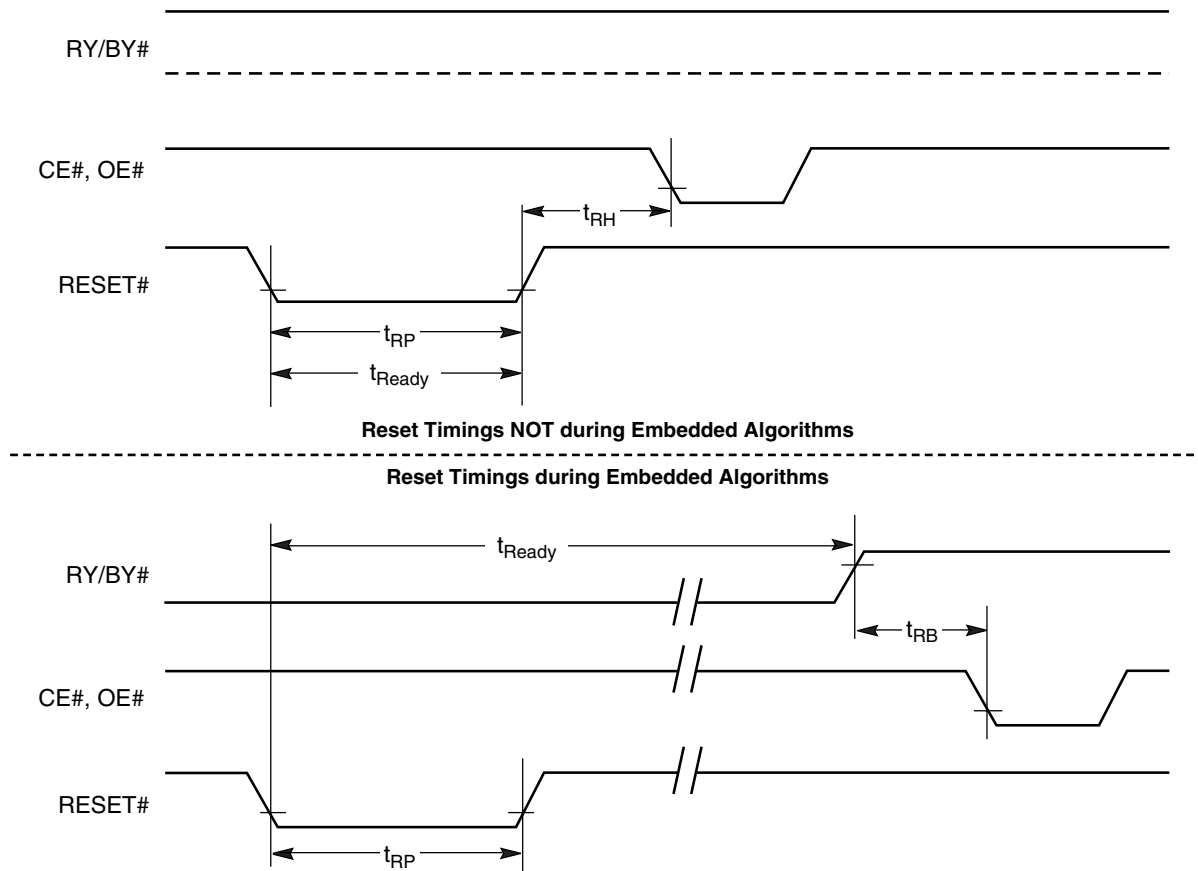
Figure I3.   Reset Timings

S29PLI29J for MCP

Erase/Program Operations

Table 20.   Erase and Program Operations

Parameter				Speed Options				
JEDEC	Std	Description		55	60	65	70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	60	65	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	30	35			ns
	t_{AHT}	Address Hold Time From CE1#, CE#2 or OE# high during toggle bit polling	Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	10				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE1# or CE#2 Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE1# or CE#2 Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	25			ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 4)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 4)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 4)	Typ	0.5				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50				µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90				ns
			Min	35				ns

Notes:

1. *Not 100% tested.*

2. *S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}*

3. *S29PL129J - There are two CE# (CE1#, CE2#).*

4. *See Table 25, "Erase And Programming Performance," on page 78 for more information.*

Timing Diagrams

Program Command Sequence (last two cycles)   Read Status Data (last two cycles)

Notes:
1. PA = program address, PD = program data, D_{OUT} is the true data at the program address
2. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
3. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#
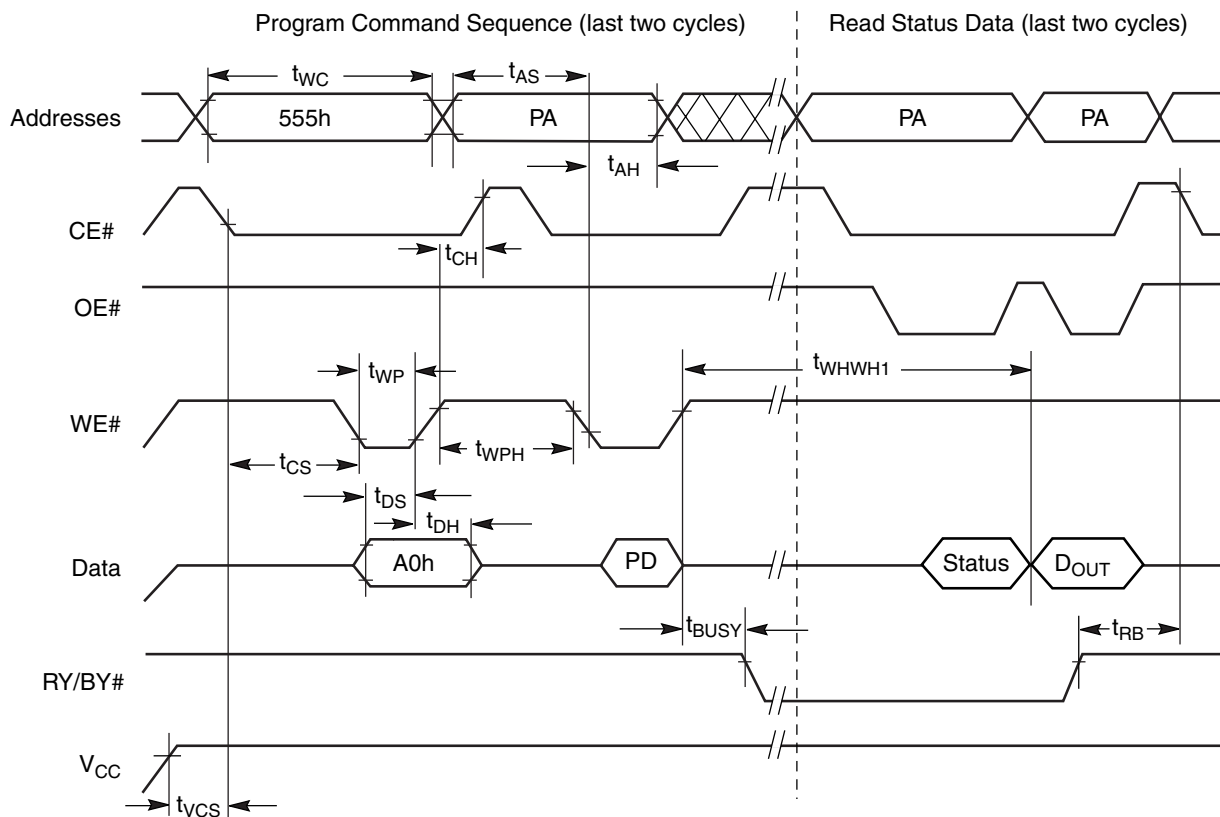
Figure I4.   Program Operation Timings
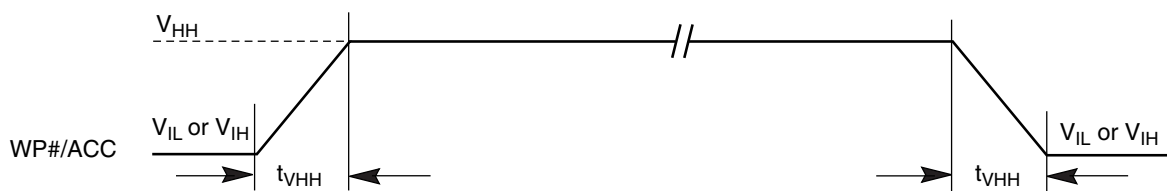
Figure I5.   Accelerated Program Timing Diagram
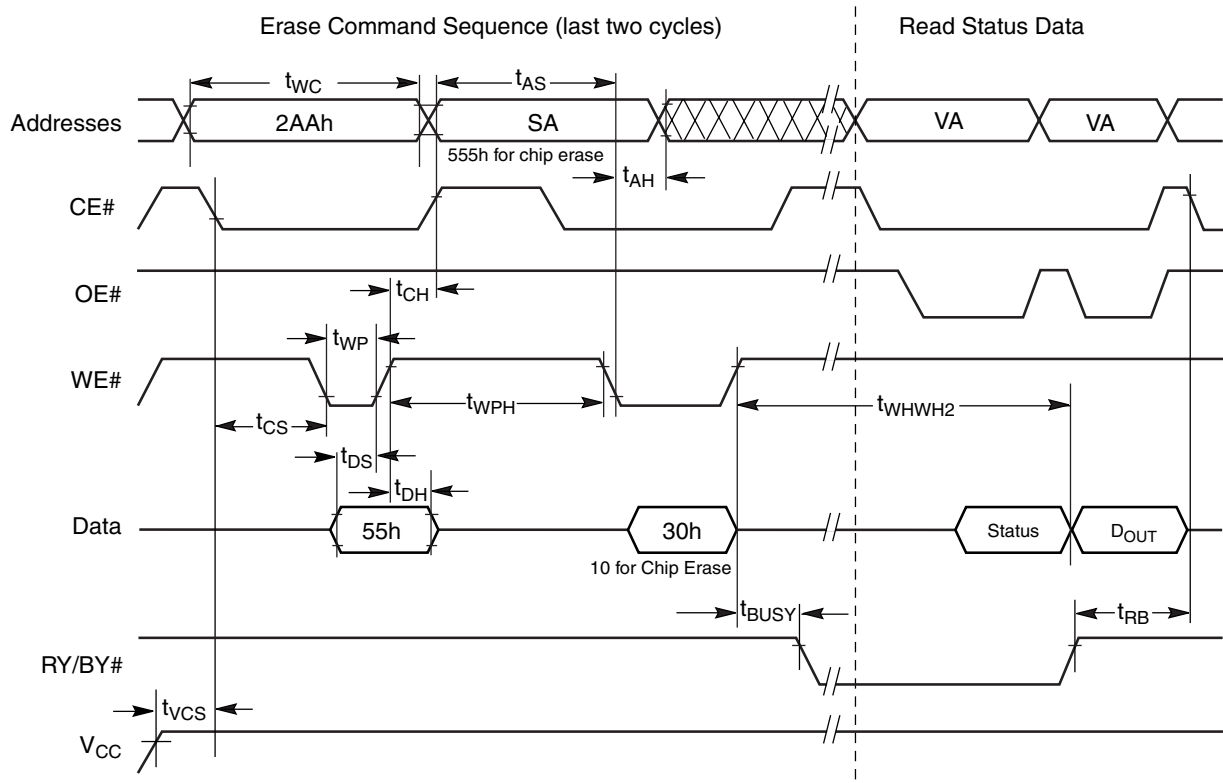
Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see *"Write Operation Status"* on page 56
2. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
3. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#

Figure 16.   Chip/Sector Erase Operation Timings
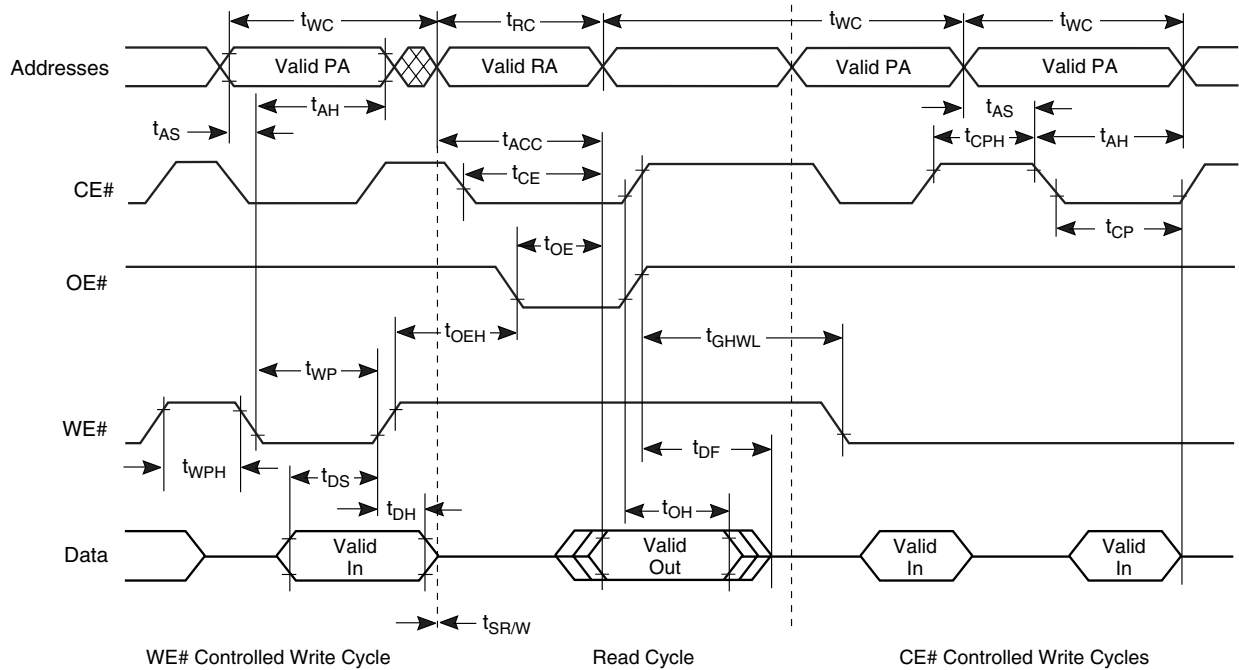
Figure 17.   Back-to-back Read/Write Cycle Timings
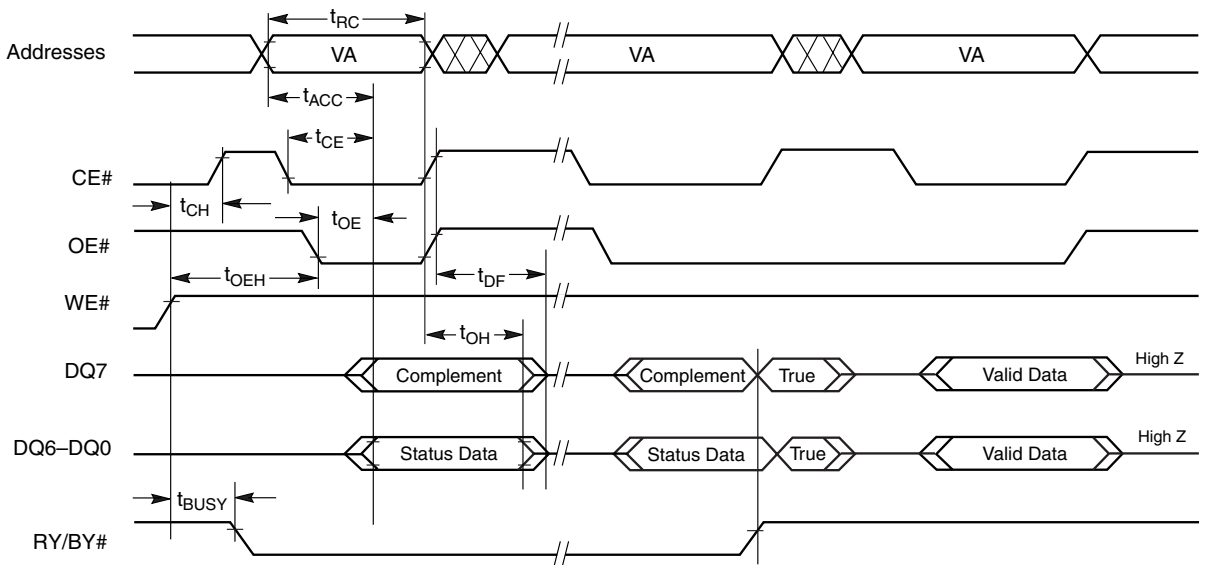
Note: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

Figure 18.   Data# Polling Timings (During Embedded Algorithms)
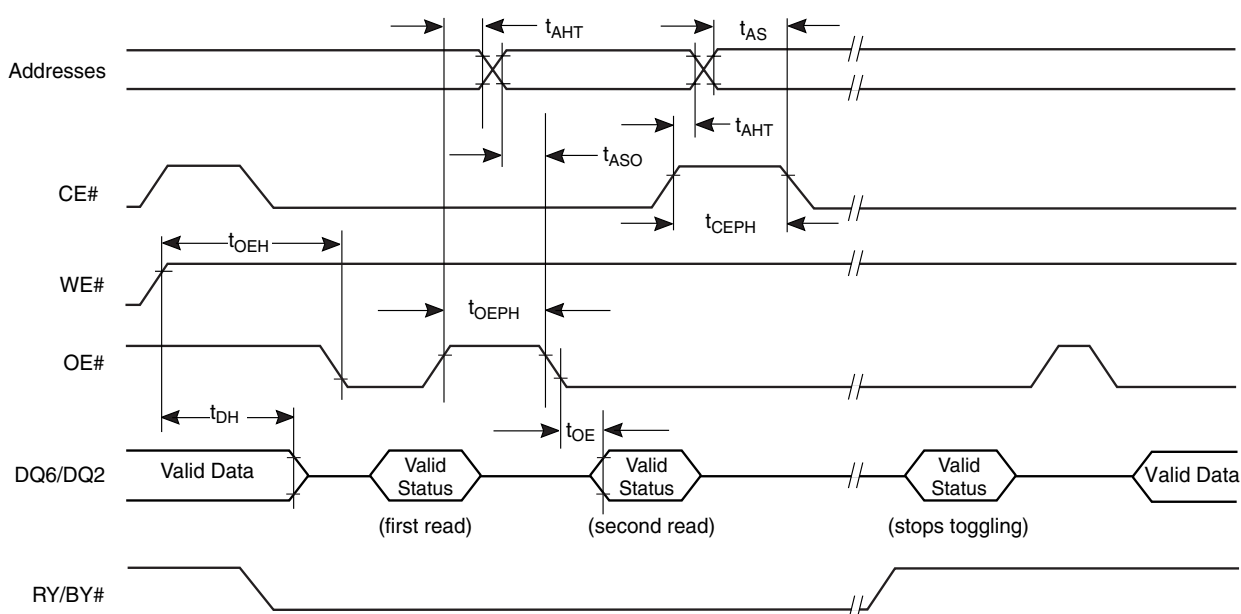
Notes:

1. VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle
2. S29PL129J - During CE1# transitions, CE2# = V$_{IH}$; During CE2# transitions, CE1# = V$_{IH}$
3. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#

Figure 19.   Toggle Bit Timings (During Embedded Algorithms)
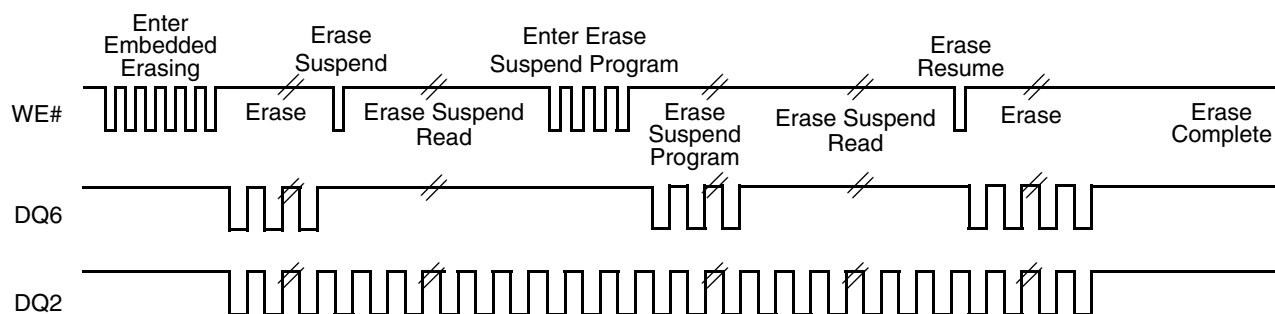
Note: Note: DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

Figure 20.   DQ2 vs. DQ6

Protect/Unprotect

Table 2I.   Temporary Sector Unprotect

Parameter					All Speed Options	Unit
JEDEC	**Std**	**Description**				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min		500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min		250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min		4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min		4	µs

Note: Not 100% tested.
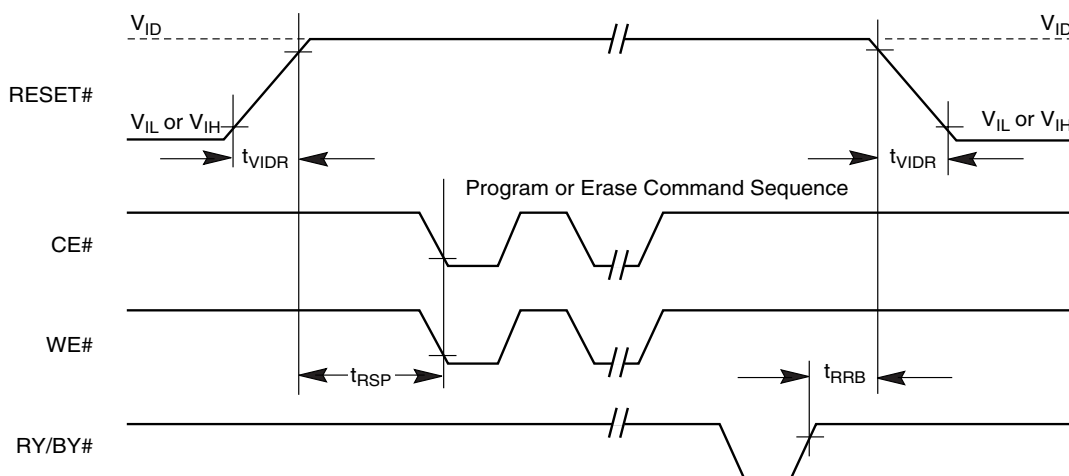
Figure 2I.   Temporary Sector Unprotect Timing Diagram
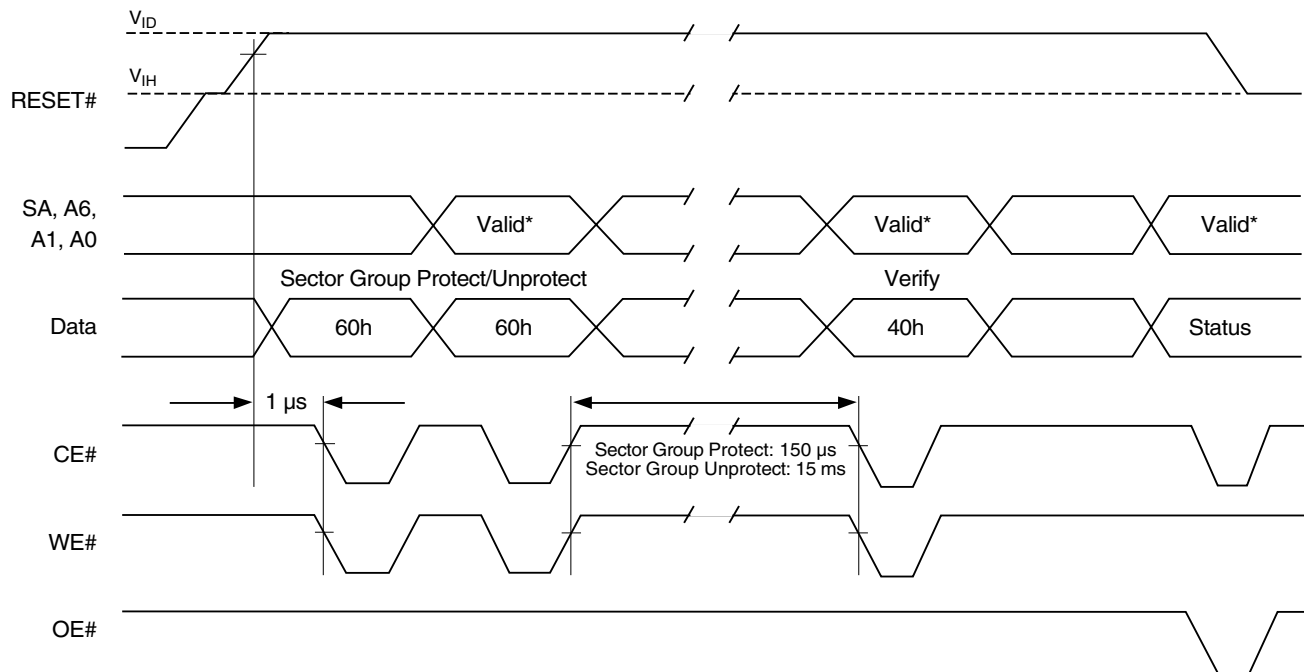
Notes:
1. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.
2. S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}
3. S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#

Figure 22.   Sector/Sector Block Protect and Unprotect Timing Diagram

Controlled Erase Operations

Table 22.   Alternate CE# Controlled Erase and Program Operations

Parameter				Speed Options				
JEDEC	Std	Description		55	60	65	70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	60	65	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	30	35			ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE1# or CE#2 Pulse Width	Min	35	40			ns
t_{EHEL}	t_{CPH}	CE1# or CE#2 Pulse Width High	Min	20	25			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec

Notes:

1. *Not 100% tested.*

2. *See the Table 25, "Erase And Programming Performance," on page 78 for more information.*
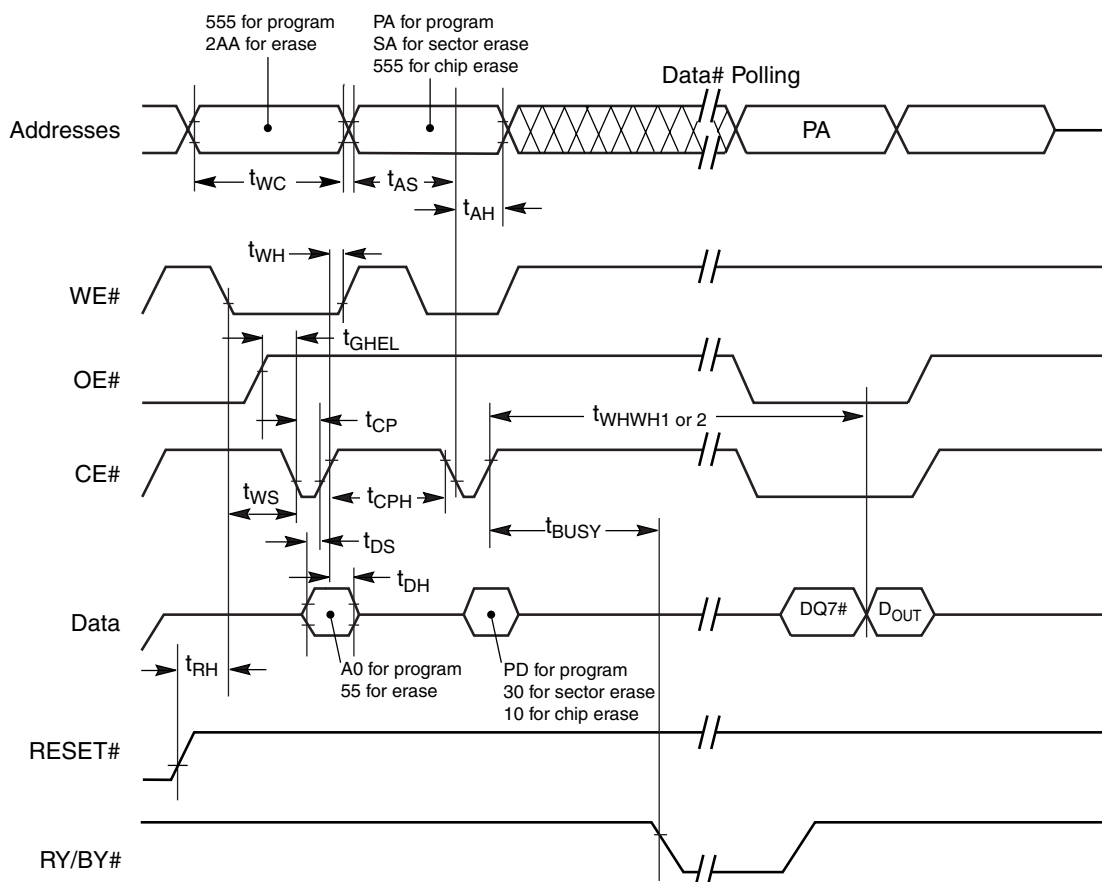
Notes:
1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device*
4. *S29PL129J - During CE1# transitions, CE2# = V_{IH}; During CE2# transitions, CE1# = V_{IH}*
5. *S29PL129J - There are two CE# (CE1#, CE2#). In the above waveform CE# = CE1# or CE2#*

Table 23.   Alternate CE# Controlled Write (Erase/Program) Operation Timings

Table 24.   CEI#/CE2# Timing

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{CCR}	CE1#/CE2# Recover Time	Min	30	ns
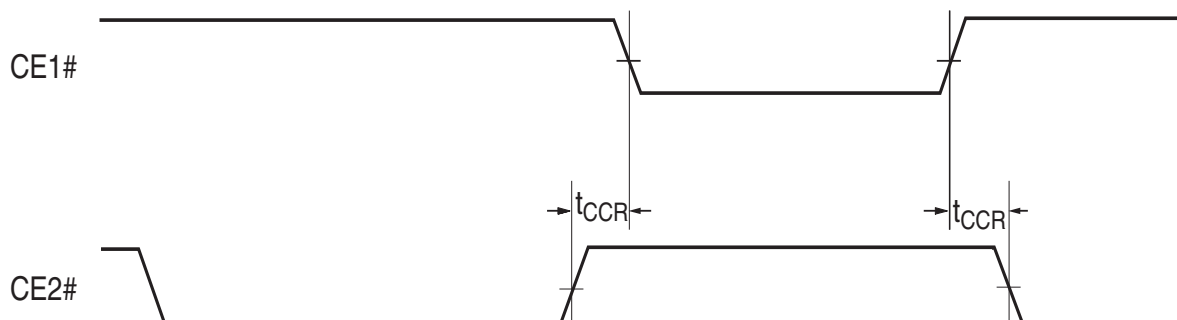
Figure 23.   Timing Diagram for Alternating Between CEI# and CE2# Control

Table 25.   Erase And Programming Performance

Parameter		Typ (Note I)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	2	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	PL129J	135	216	sec	
Word Program Time		6	100	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time		4	60	µs	
Chip Program Time (Note 3)	PL129J	50.4	200	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25° C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern. All values are subject to change.*

2. *Under worst case conditions of 90° C, V_{CC} = 2.7 V, 1,000,000 cycles. All values are subject to change.*

3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*

4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*

5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 12 for further information on command definitions.*

6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

BGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6.3	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	7.0	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	5.5	8	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	11	12	pF

Notes:

1. *Sampled, not 100% tested.*

2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

pSRAM Type 6

2M Word by 16-bit Cmos Pseudo Static RAM (32M Density)
4M Word by 16-bit Cmos Pseudo Static RAM (64M Density)

Features

- Single power supply voltage of 2.6 to 3.3 V
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode:
  — Page read operation by 8 words
- Logic compatible with SRAM R/W pin
- Standby current
  — Standby = 70 μA (32M)
  — Standby = 100 μA (64M)
  — Deep power-down Standby = 5 μA
- Access Times

	32M 64M
Access Time	70 ns
CE1# Access Time	70 ns
OE# Access Time	25 ns
Page Access Time	30 ns

Pin Description

Pin Name	Description
A_0 to A_{21}	Address Inputs
A0 to A2	Page Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
CE1#	Chip Enable Input
CE2	Chip select Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#,UB#	Data Byte Control Inputs
V_{DD}	Power Supply
GND	Ground
NC	Not Connection

SPANSION™

Functional Description

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	Address	I/O$_{1-8}$	I/O$_{9-16}$	Power
Read (Word)	L	H	L	H	L	L	X	D$_{OUT}$	D$_{OUT}$	I$_{DDO}$
Read (Lower Byte)	L	H	L	H	L	H	X	D$_{OUT}$	High-Z	I$_{DDO}$
Read (Upper Byte)	L	H	L	H	H	L	X	High-Z	D$_{OUT}$	I$_{DDO}$
Write (Word)	L	H	X	L	L	L	X	D$_{IN}$	D$_{IN}$	I$_{DDO}$
Write (Lower Byte)	L	H	X	L	L	H	X	D$_{IN}$	Invalid	I$_{DDO}$
Write (Upper Byte)	L	H	X	L	H	L	X	Invalid	D$_{IN}$	I$_{DDO}$
Outputs Disabled	L	H	H	H	X	X	X	High-Z	High-Z	I$_{DDO}$
Standby	H	H	X	X	X	X	X	High-Z	High-Z	I$_{DDO}$
Deep Power-down Standby	H	L	X	X	X	X	X	High-Z	High-Z	I$_{DDSD}$

Legend: L = Low-level Input (V$_{IL}$), H = High-level Input (V$_{IH}$), X = V$_{IL}$ or V$_{IH}$, High-Z = High Impedance.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V$_{DD}$	Power Supply Voltage	-1.0 to 3.6	V
V$_{IN}$	Input Voltage	-1.0 to 3.6	V
V$_{OUT}$	Output Voltage	-1.0 to 3.6	V
T$_{opr}$	Operating Temperature	-40 to 85	°C
T$_{strg}$	Storage Temperature	-55 to 150	°C
P$_{D}$	Power Dissipation	0.6	W
I$_{OUT}$	Short Circuit Output Current	50	mA

Note: ESD Immunity: *Spansion Flash memory Multi-Chip Products (MCPs) may contain component devices that are developed by Spansion and component devices that are developed by a third party (third-party components). Spansion components are tested and guaranteed to the ESD immunity levels listed in the corresponding Spansion Flash memory Qualification Database. Third-party components are neither tested nor guaranteed by Spansion for ESD immunity. However, ESD test results for third-party components may be available from the component manufacturer. Component manufacturer contact information is listed in the Spansion MCP Qualification Report, when available. The Spansion Flash memory Qualification Database and Spansion MCP Qualification Report are available from Spansion sales offices.*

DC Recommended Operating Conditions (Ta = -40°C to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V$_{DD}$	Power Supply Voltage	2.6	2.75	3.3	
V$_{IH}$	Input High Voltage	2.0	—	V$_{DD}$ + 0.3 (Note)	V
V$_{IL}$	Input Low Voltage	-0.3 (Note)	—	0.4	

Note: *V$_{IH}$ (Max) V$_{DD}$ = 1.0 V with 10 ns pulse width. V$_{IL}$ (Min) -1.0 V with 10 ns pulse width.*

DC Characteristics (Ta = -40°C to 85°C, VDD = 2.6 to 3.3 V) (See Note 3 to 4)

Symbol	Parameter	Test Condition		Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		-1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	Output disable, V_{OUT} = 0 V to V_{DD}		-1.0	—	+1.0	µA
V_{OH}	Output High Voltage	I_{OH} = - 0.5 mA		2.0	¾ V	V	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA		—	—	0.4	V
I_{DDO1}	Operating Current	CE1# = V_{IL}, CE2 = V_{IH}, I_{OUT} = 0 mA, t_{RC} = min.	ET5UZ8A-43DS	—	—	40	mA
			ET5VB5A-43DS	—	—	50	
I_{DDO2}	Page Access Operating Current	CE1# = V_{IL}, CE2 = V_{IH}, I_{OUT} = 0 mA Page add. cycling, t_{RC} = min.		—	—	25	mA
I_{DDS}	Standby Current (MOS)	CE1# = V_{DD} - 0.2 V, CE2 = V_{DD} - 0.2 V	ET5UZ8A-43DS	—	—	70	mA
			ET5VB5A-43DS	—	—	100	µA
I_{DDSD}	Deep Power-down Standby Current	CE2 = 0.2 V		—	—	5	µA

Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: *This parameter is sampled periodically and is not 100% tested.*

AC Characteristics and Operating Conditions

(Ta = -40°C to 85°C, VDD = 2.6 to 3.3 V) (See Note 5 to 11)

Symbol	Parameter	Min	Max	Unit
t_{RC}	Read Cycle Time	70	10000	ns
t_{ACC}	Address Access Time	—	70	ns
t_{CO}	Chip Enable (CE1#) Access Time	—	70	ns
t_{OE}	Output Enable Access Time	—	25	ns
t_{BA}	Data Byte Control Access Time	—	25	ns
t_{COE}	Chip Enable Low to Output Active	10	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	Data Byte Control Low to Output Active	0	—	ns
t_{OD}	Chip Enable High to Output High-Z	—	20	ns
t_{ODO}	Output Enable High to Output High-Z	—	20	ns
t_{BD}	Data Byte Control High to Output High-Z	—	20	ns

Symbol	Parameter	Min	Max	Unit
t_{OH}	Output Data Hold Time	10	—	ns
t_{PM}	Page Mode Time	70	10000	ns
t_{PC}	Page Mode Cycle Time	30	—	ns
t_{AA}	Page Mode Address Access Time	—	30	ns
t_{AOH}	Page Mode Output Data Hold Time	10	—	ns
t_{WC}	Write Cycle Time	70	10000	ns
t_{WP}	Write Pulse Width	50	—	ns
t_{CW}	Chip Enable to End of Write	70	—	ns
t_{BW}	Data Byte Control to End of Write	60	—	ns
t_{AW}	Address Valid to End of Write	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{CEH}	Chip Enable High Pulse Width	10	—	ns
t_{WEH}	Write Enable High Pulse Width	6	—	ns
t_{ODW}	WE# Low to Output High-Z	—	20	ns
t_{OEW}	WE# High to Output Active	0		ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{CS}	CE2 Set-up Time	0	—	ns
t_{CH}	CE2 Hold Time	300	—	µs
t_{DPD}	CE2 Pulse Width	10	—	ms
t_{CHC}	CE2 Hold from CE1#	0	—	ns
t_{CHP}	CE2 Hold from Power On	30	—	µs

AC Test Conditions

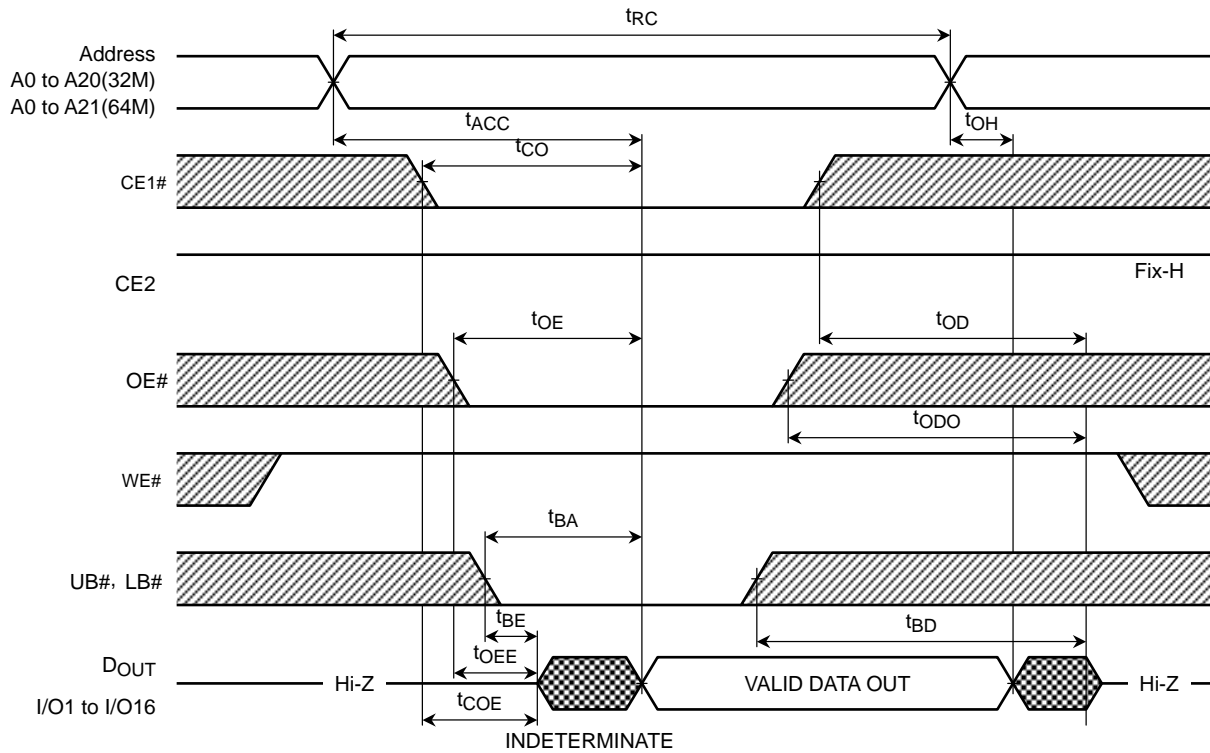| Parameter	Condition
Output load	30 pF + 1 TTL Gate
Input pulse level	V_{DD} - 0.2 V, 0.2 V
Timing measurements	V_{DD} x 0.5
Reference level	V_{DD} x 0.5
t_R, t_F	5 ns

Timing Diagrams

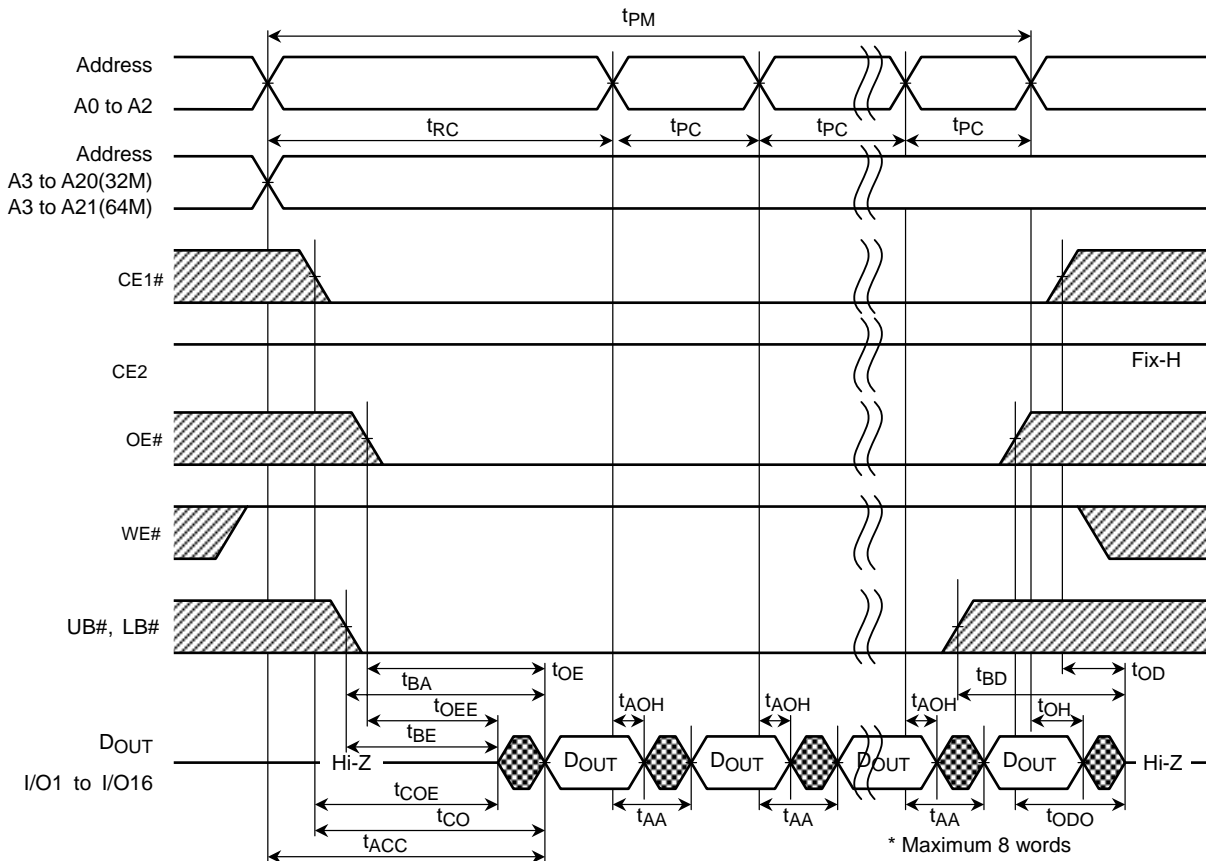## Read Timings

Figure 24.   Read Cycle

Figure 25.   Page Read Cycle (8 Words Access)
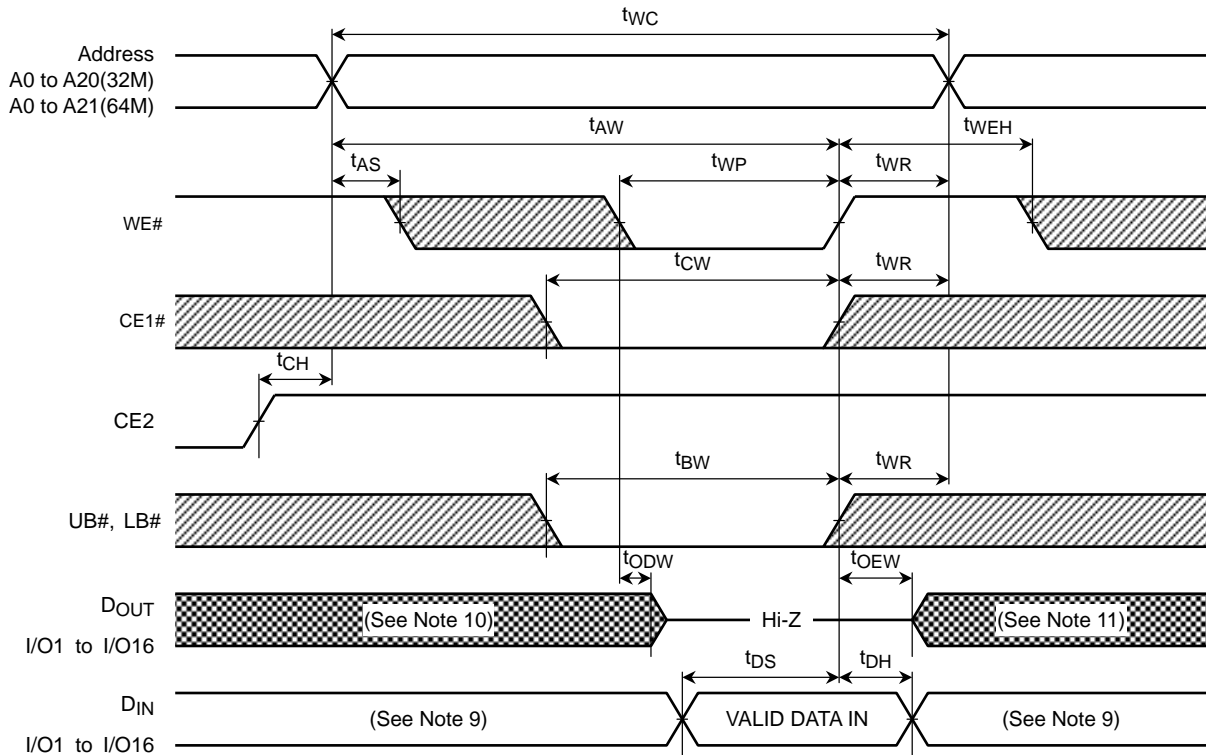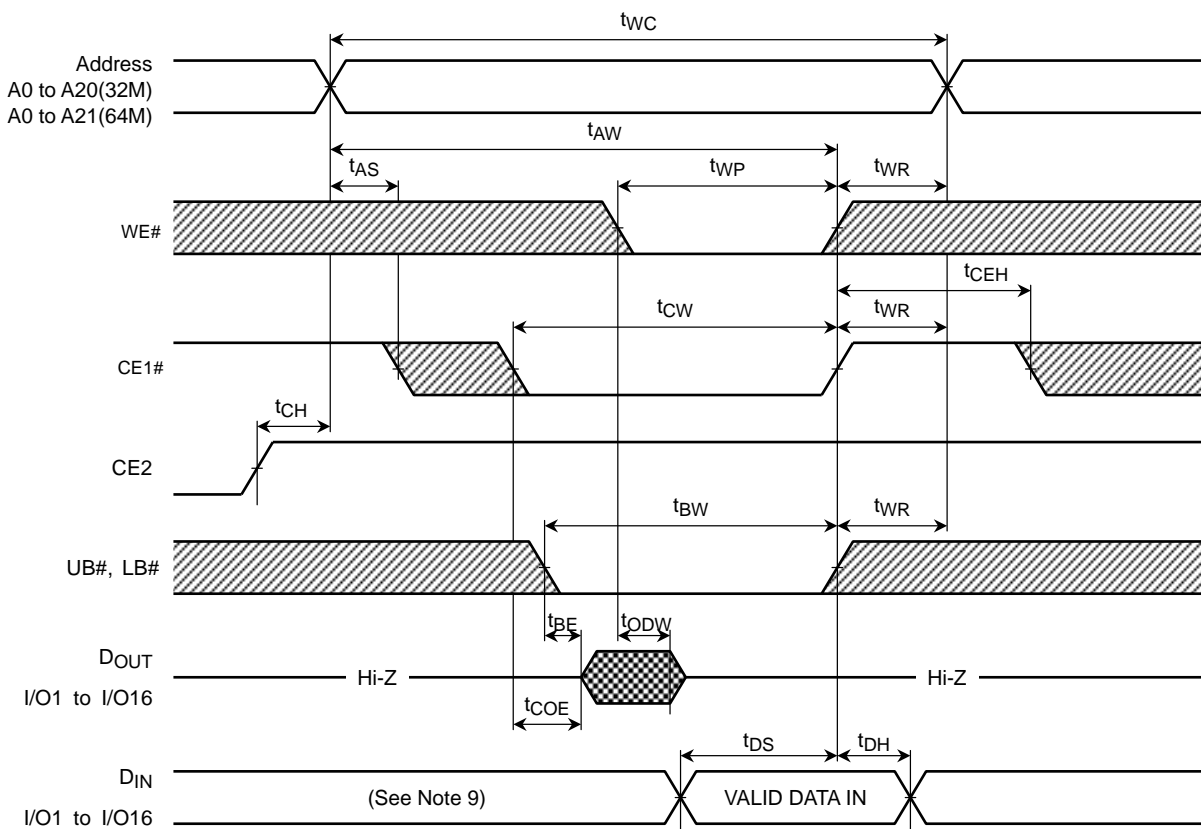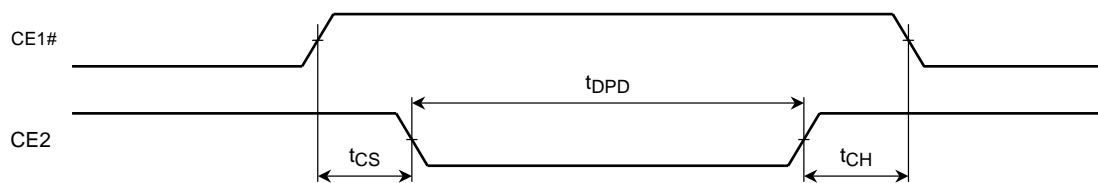
Write Timings

Figure 26.   Write Cycle #l (WE# Controlled) (See Note 8)

Figure 27.   Write Cycle #2 (CE# Controlled) (See Note 8)

Deep Power-down Timing

Figure 28.   Deep Power Down Timing

Power-on Timing
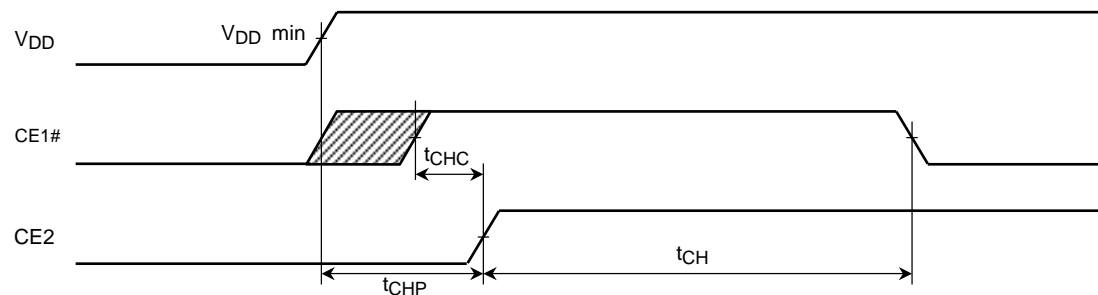
Figure 29.   Power-on Timing

Provisions of Address Skew

Read

In case multiple invalid address cycles shorter than t_{RC} min. sustain over 10 µs in an active status, at least one valid address cycle over t_{RC} min. is required during 10µs.
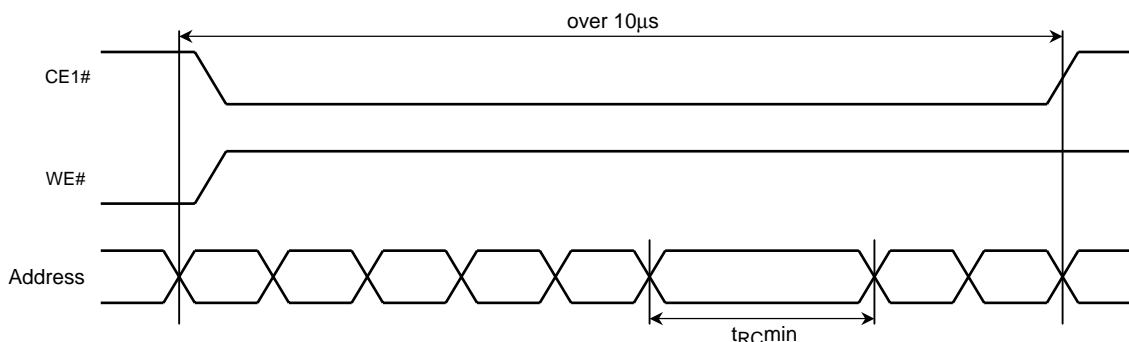
Figure 30.   Read

Write

In case multiple invalid address cycles shorter than t_{WC} min. sustain over 10 µs in an active status, at least one valid address cycle over t_{WC} min. is required during 10 µs.
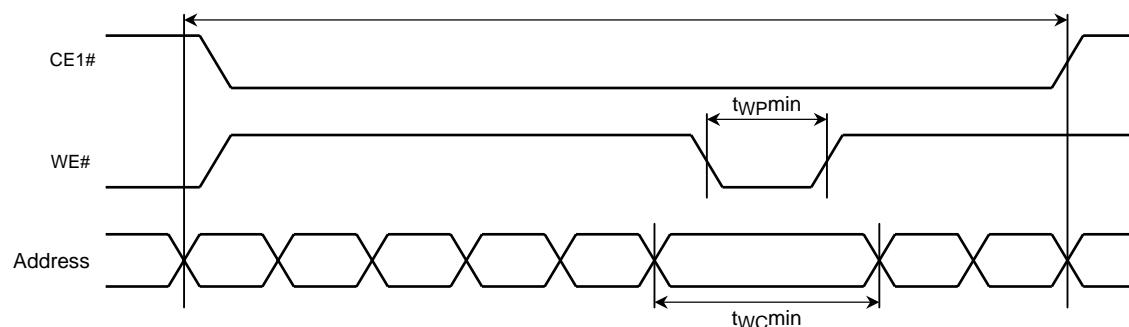
Figure 3I.   Write

Notes:

1. *Stresses greater than listed under "Absolute Maximum Ratings" section may cause permanent damage to the device.*

2. *All voltages are reference to GND.*

3. *I_{DDO} depends on the cycle time.*

4. *I_{DDO} depends on output loading. Specified values are defined with the output open condition.*

5. *AC measurements are assumed t_R, t_F = 5 ns.*

6. *Parameters t_{OD}, t_{ODO}, t_{BD} and $t_{OD}W$ define the time at which the output goes the open condition and are not output voltage reference levels.*

7. *Data cannot be retained at deep power-down stand-by mode.*

8. *If OE# is high during the write cycle, the outputs will remain at high impedance.*

9. *During the output state of I/O signals, input signals of reverse polarity must not be applied.*

10. *If CE1# or LB#/UB# goes LOW coincident with or after WE# goes LOW, the outputs will remain at high impedance.*

11. *If CE1# or LB#/UB# goes HIGH coincident with or before WE# goes HIGH, the outputs will remain at high impedance.*

pSRAM Type I

4Mbit (256K Word x 16-bit)
8Mbit (512K Word x 16-bit)
16Mbit (1M Word x 16-bit)
32Mbit (2M Word x 16-bit)
64Mbit (4M Word x 16-bit)

Functional Description

Mode	CE#	CE2/ZZ#	OE#	WE#	UB#	LB#	Addresses	I/O 1-8	I/O 9-16	Power
Read (word)	L	H	L	H	L	L	X	Dout	Dout	I_{ACTIVE}
Read (lower byte)	L	H	L	H	H	L	X	Dout	High-Z	I_{ACTIVE}
Read (upper byte)	L	H	L	H	L	H	X	High-Z	Dout	I_{ACTIVE}
Write (word)	L	H	X	L	L	L	X	Din	Din	I_{ACTIVE}
Write (lower byte)	L	H	X	L	H	L	X	Din	Invalid	I_{ACTIVE}
Write (upper byte)	L	H	X	L	L	H	X	Invalid	Din	I_{ACTIVE}
Outputs disabled	L	H	H	H	X	X	X	High-Z	High-Z	I_{ACTIVE}
Standby	H	H	X	X	X	X	X	High-Z	High-Z	$I_{STANDBY}$
Deep power down	H	L	X	X	X	X	X	High-Z	High-Z	$I_{DEEP\ SLEEP}$

Absolute Maximum Ratings

Item	Symbol	Ratings	Units
Voltage on any pin relative to V_{SS}	Vin, Vout	-0.2 to V_{CC} +0.3	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-0.2 to 3.6	V
Power dissipation	P_D	1	W
Storage temperature	T_{STG}	-55 to 150	°C
Operating temperature	T_A	-25 to 85	°C

DC Characteristics

(4Mb pSRAM Asynchronous)

			Asynchronous		
Performance Grade			-70		
Density			4Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.3	V
V_{IL}	Input Low Level		-0.3	0.4	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V
		I_{OH} = -0.2 mA	0.8 Vccq		
		I_{OH} = -0.5 mA			
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V
		I_{OL} = 0.2 mA		0.2	
		I_{OL} = 0.5 mA			
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V		70	µA
		V_{CC} = 3.3 V			
$I_{DEEP\ SLEEP}$	Deep Power Down Current			x	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			x	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			x	µA

DC Characteristics

(8Mb pSRAM Asynchronous)

Symbol	Parameter	Conditions	Asynchronous								
			B						**C**		
			-55			-70			-70		
			8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
			Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V	2.7	3.6	V	2.7	3.3	V
V_{IH}	Input High Level		2.2	V_{CC} + 0.3	V	2.2	V_{CC} + 0.3	V	0.8	V_{CC}+0.3	V
V_{IL}	Input Low Level		-0.3	0.6	V	-0.3	0.6	V	-0.3	0.4	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA		0.5	µA		0.5	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA		0.5	µA		0.5	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC}-0.4		V	V_{CC}-0.4		V			V
		I_{OH} = -0.2 mA							0.8 V_{CCQ}		
		I_{OH} = -0.5 mA									
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V		0.4	V			V
		I_{OL} = 0.2 mA								0.2	
		I_{OL} = 0.5 mA									
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		23	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V		60	µA		60	µA		70	µA
		V_{CC} = 3.3 V									
$I_{DEEP SLEEP}$	Deep Power Down Current			x	µA		x	µA		x	µA
$I_{PAR 1/4}$	1/4 Array PAR Current			x	µA		x	µA		x	µA
$I_{PAR 1/2}$	1/2 Array PAR Current			x	µA		x	µA		x	µA

DC Characteristics

(16Mb pSRAM Asynchronous)

			Asynchronous					
		Performance Grade	-55			-70		
		Density	16Mb pSRAM			16Mb pSRAM		
Symbol	Parameter	Conditions	Minimum	Maximum	Units	Minimum	Maximum	Units
V_{CC}	Power Supply		2.7	3.6	V	2.7	3.6	V
V_{IH}	Input High Level		2.2	$V_{CC} + 0.3$	V	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Level		-0.3	0.6	V	-0.3	0.6	V
I_{IL}	Input Leakage Current	$V_{in} = 0$ to V_{CC}		0.5	μA		0.5	μA
I_{LO}	Output Leakage Current	$OE = V_{IH}$ or Chip Disabled		0.5	μA		0.5	μA
V_{OH}	Output High Voltage	$I_{OH} = -1.0$ mA	V_{CC}-0.4		V	V_{CC}-0.4		V
		$I_{OH} = -0.2$ mA						
		$I_{OH} = -0.5$ mA						
V_{OL}	Output Low Voltage	$I_{OL} = 2.0$ mA		0.4	V		0.4	V
		$I_{OL} = 0.2$ mA						
		$I_{OL} = 0.5$ mA						
I_{ACTIVE}	Operating Current	$V_{CC} = 3.3$ V		25	mA		25	mA
$I_{STANDBY}$	Standby Current	$V_{CC} = 3.0$ V		100	μA		100	μA
		$V_{CC} = 3.3$ V						
$I_{DEEP\ SLEEP}$	Deep Power Down Current			x	μA		x	μA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			x	μA		x	μA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			x	μA		x	μA

SPANSION™

DC Characteristics

(16Mb pSRAM Page Mode)

			Page Mode								
Performance Grade			**-60**			**-65**			**-70**		
Density			**16Mb pSRAM**			**16Mb pSRAM**			**16Mb pSRAM**		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Units**	**Min**	**Max**	**Units**	**Min**	**Max**	**Units**
V_{CC}	Power Supply		2.7	3.3	V	2.7	3.3	V	2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		1	µA		1	µA		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		1	µA		1	µA		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V			V			V
		I_{OH} = -0.2 mA									
		I_{OH} = -0.5 mA	0.8 Vccq			0.8 Vccq			0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V			V			V
		I_{OL} = 0.2 mA									
		I_{OL} = 0.5 mA		0.2 Vccq			0.2 Vccq			0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		25	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA			µA			µA
		V_{CC} = 3.3 V		100			100			100	
$I_{DEEP\ SLEEP}$	Deep Power Down Current			10	µA		10	µA		10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA		65	µA		65	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA		80	µA		80	µA

pSRAM Type I pSRAM_Type01_I2_AI_August 30, 2004

DC Characteristics

(32Mb pSRAM Page Mode)

			Page Mode											
Version			C			E								
Performance Grade			-65			-60			-65			-70		
Density			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{CC}	Power Supply		2.7	3.6	V	2.7	3.3	V	2.7	3.3	V	2.7	3.3	V
V_{IH}	Input High Level		1.4	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.4	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA		1	µA		1	µA		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA		1	µA		1	µA		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA												
		I_{OH} = -0.2 mA	0.8 Vccq		V			V			V			V
		I_{OH} = -0.5 mA				0.8 Vccq			0.8 Vccq			0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA												
		I_{OL} = 0.2 mA		0.2	V			V			V			V
		I_{OL} = 0.5 mA					0.2 Vccq			0.2 Vccq			0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		25	mA		25	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA			µA			µA			µA
		V_{CC} = 3.3 V		100			120			120			120	
$I_{DEEP\ SLEEP}$	Deep Power Down Current			10	µA		10	µA		10	µA		10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA		75	µA		75	µA		75	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA		90	µA		90	µA		90	µA

DC Characteristics

(64Mb pSRAM Page Mode)

			Page Mode		
		Performance Grade	-70		
		Density	64Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.2 Vccq	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V
		I_{OH} = -0.2 mA			
		I_{OH} = -0.5 mA	0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V
		I_{OL} = 0.2 mA			
		I_{OL} = 0.5 mA		0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA
		V_{CC} = 3.3 V		120	
$I_{DEEP SLEEP}$	Deep Power Down Current			10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA

Timing Test Conditions

Item	
Input Pulse Level	0.1 V_{CC} to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Operating Temperature	-25°C to +85°C

Output Load Circuit
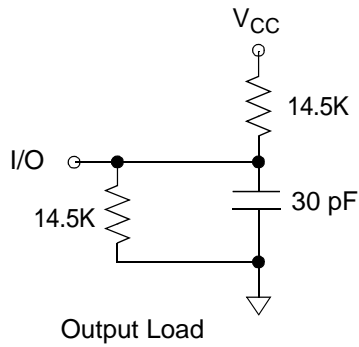
Figure 32.   Output Load Circuit

Power Up Sequence

After applying power, maintain a stable power supply for a minimum of 200 μs after CE# > V_{IH}.

AC Characteristics

(4Mb pSRAM Page Mode)

3 Volt	Symbol	Parameter	Asynchronous		
		Performance Grade	-70		
		Density	4Mb pSRAM		
			Min	Max	Units
Read	trc	Read cycle time	70		ns
	taa	Address Access Time		70	ns
	tco	Chip select to output		70	ns
	toe	Output enable to valid output		20	ns
	tba	UB#, LB# Access time		70	ns
	tlz	Chip select to Low-z output	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns
	tolz	Output enable to Low-Z output	5		ns
	thz	Chip enable to High-Z output	0	20	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns
	tohz	Output disable to High-Z output	0	20	ns
	toh	Output hold from Address Change	10		ns

3 Volt	Symbol	Parameter	Asynchronous		
		Performance Grade	-70		
		Density	4Mb pSRAM		
	Symbol	Parameter	Min	Max	Units
Write	twc	Write cycle time	70		ns
	tcw	Chipselect to end of write	70		ns
	tas	Address set up Time	0		ns
	taw	Address valid to end of write	70		ns
	tbw	UB#, LB# valid to end of write	70		ns
	twp	Write pulse width	55		ns
	twr	Write recovery time	0		ns
	twhz	Write to output High-Z		20	ns
	tdw	Data to write time overlap	25		ns
	tdh	Data hold from write time	0		ns
	tow	End write to output Low-Z	5		
	tow	Write high pulse width	7.5		ns
Other	tpc	Page read cycle	x		
	tpa	Page address access time		x	
	twpc	Page write cycle	x		
	tcp	Chip select high pulse width	x		

AC Characteristics

(8Mb pSRAM Asynchronous)

			Asynchronous								
		Version	B						C		
		Performance Grade	-55			-70			-70		
		Density	8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	55		ns	70		ns	70		ns
	taa	Address Access Time		55	ns		70	ns		70	ns
	tco	Chip select to output		55	ns		70	ns		70	ns
	toe	Output enable to valid output		30	ns		35	ns		20	ns
	tba	UB#, LB# Access time		55	ns		70	ns		70	ns
	tlz	Chip select to Low-z output	5		ns	5		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	5		ns	5		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	tohz	Output disable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	toh	Output hold from Address Change	10		ns	10		ns	10		ns

3 Volt	Symbol	Parameter	Asynchronous								
		Version	B						C		
		Performance Grade	-55			-70			-70		
		Density	8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
			Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	55		ns	70		ns	70		ns
	tcw	Chip select to end of write	45		ns	55		ns	70		ns
	tas	Address set up Time	0		ns	0		ns	0		ns
	taw	Address valid to end of write	45		ns	55		ns	70		ns
	tbw	UB#, LB# valid to end of write	45		ns	55		ns	70		ns
	twp	Write pulse width	45		ns	55		ns	55		ns
	twr	Write recovery time	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		25	ns		25			20	ns
	tdw	Data to write time overlap	40		ns	40		ns	25		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5		
	tow	Write high pulse width	x	x	ns	x	x	ns	x	x	ns
Other	tpc	Page read cycle	x			x			x		
	tpa	Page address access time		x			x			x	
	twpc	Page write cycle	x			x			x		
	tcp	Chip select high pulse width	x			x			x		

SPANSION™

AC Characteristics

(16Mb pSRAM Asynchronous)

3 Volt	Symbol	Parameter	Asynchronous					
		Performance Grade	-55			-70		
		Density	16Mb pSRAM			16Mb pSRAM		
			Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	55		ns	70		ns
	taa	Address Access Time		55	ns		70	ns
	tco	Chip select to output		55	ns		70	ns
	toe	Output enable to valid output		30	ns		35	ns
	tba	UB#, LB# Access time		55	ns		70	ns
	tlz	Chip select to Low-z output	5		ns	5		ns
	tblz	UB#, LB# Enable to Low-Z output	5		ns	5		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns
	thz	Chip enable to High-Z output	0	25	ns	0	25	ns
	tbhz	UB#, LB# disable to High-Z output	0	25	ns	0	25	ns
	tohz	Output disable to High-Z output	0	25	ns	0	25	ns
	toh	Output hold from Address Change	10		ns	10		ns

3 Volt	Symbol	Parameter	Asynchronous					
		Performance Grade	**-55**			**-70**		
		Density	**16Mb pSRAM**			**16Mb pSRAM**		
	Symbol	**Parameter**	**Min**	**Max**	**Units**	**Min**	**Max**	**Units**
Write	twc	Write cycle time	55		ns	70		ns
	tcw	Chipselect to end of write	50		ns	55		ns
	tas	Address set up Time	0		ns	0		ns
	taw	Address valid to end of write	50		ns	55		ns
	tbw	UB#, LB# valid to end of write	50		ns	55		ns
	twp	Write pulse width	50		ns	55		ns
	twr	Write recovery time	0		ns	0		ns
	twhz	Write to output High-Z		25	ns		25	ns
	tdw	Data to write time overlap	25		ns	25		ns
	tdh	Data hold from write time	0		ns	0		ns
	tow	End write to output Low-Z	5			5		
	tow	Write high pulse width	x	x	ns	x	x	ns
Other	tpc	Page read cycle	x			x		
	tpa	Page address access time		x			x	
	twpc	Page write cycle	x			x		
	tcp	Chip select high pulse width	x			x		

AC Characteristics

(16Mb pSRAM Page Mode)

			Page Mode								
	Performance Grade		-60			-65			-70		
	Density		16Mb pSRAM			16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	60	20k	ns	65	20k	ns	70	20k	ns
	taa	Address Access Time		60	ns		65	ns		70	ns
	tco	Chip select to output		60	ns		65	ns		70	ns
	toe	Output enable to valid output		25	ns		25	ns		25	ns
	tba	UB#, LB# Access time		60	ns		65	ns		70	ns
	tlz	Chip select to Low-z output	10		ns	10		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns	10		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	tohz	Output disable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	toh	Output hold from Address Change	5		ns	5		ns	5		ns

			Page Mode								
Performance Grade			-60			-65			-70		
Density			16Mb pSRAM			16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	60	20k	ns	65	20k	ns	70	20k	ns
	tcw	Chipselect to end of write	50		ns	60		ns	60		ns
	tas	Address set up Time	0		ns	0		ns	0		ns
	taw	Address valid to end of write	50		ns	60		ns	60		ns
	tbw	UB#, LB# valid to end of write	50		ns	60		ns	60		ns
	twp	Write pulse width	50		ns	50		ns	50		ns
	twr	Write recovery time	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		5	ns		5	ns		5	ns
	tdw	Data to write time overlap	20		ns	20		ns	20		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5		
	tow	Write high pulse width	7.5		ns	7.5		ns	7.5		ns
Other	tpc	Page read cycle	25	20k	ns	25	20k	ns	25	20k	ns
	tpa	Page address access time		25	ns		25	ns		25	ns
	twpc	Page write cycle	25	20k	ns	25	20k	ns	25	20k	ns
	tcp	Chip select high pulse width	10		ns	10		ns	10		ns

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AC Characteristics

(32Mb pSRAM Page Mode)

			Page Mode									
		Version	C			E						
		Performance Grade	-65			-60			-65			-70
		Density	32Mb pSRAM			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	65	20k	ns	60	20k	ns	65	20k	ns	70	20k	ns
	taa	Address Access Time		65	ns		60	ns		65	ns		70	ns
	tco	Chip select to output		65	ns		60	ns		65	ns		70	ns
	toe	Output enable to valid output		20	ns		25	ns		25	ns		25	ns
	tba	UB#, LB# Access time		65	ns		60	ns		65	ns		70	ns
	tlz	Chip select to Low-z output	10		ns	10		ns	10		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns	10		ns	10		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	tohz	Output disable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	toh	Output hold from Address Change	5		ns	5		ns	5		ns	5		ns

			Page Mode												
Version			**C**			**E**									
Performance Grade			**-65**			**-60**			**-65**			**-70**			
Density			**32Mb pSRAM**			**32Mb pSRAM**			**32Mb pSRAM**			**32Mb pSRAM**			
3 Volt	**Symbol**	**Parameter**	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	65	20k	ns	60	20k	ns	65	20k	ns	70	20k	ns
	tcw	Chipselect to end of write	55		ns	50		ns	60		ns	60		ns
	tas	Address set up Time	0		ns	0		ns	0		ns	0		ns
	taw	Address valid to end of write	55		ns	50		ns	60		ns	60		ns
	tbw	UB#, LB# valid to end of write	55		ns	50		ns	60		ns	60		ns
	twp	Write pulse width	55	20k	ns	50		ns	50		ns	50		ns
	twr	Write recovery time	0		ns	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		5	ns		5	ns		5	ns		5	ns
	tdw	Data to write time overlap	25		ns	20		ns	20		ns	20		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5			5		
	tow	Write high pulse width	7.5		ns	7.5		ns	7.5		ns	7.5		ns
Other	tpc	Page read cycle	25	20k	ns	25	20k	ns	25	20k	ns	25	20k	ns
	tpa	Page address access time		25	ns		25	ns		25	ns		25	ns
	twpc	Page write cycle	25	20k	ns	25	20k	ns	25	20k	ns	25	20k	ns
	tcp	Chip select high pulse width	10		ns	10		ns	10		ns	10		ns

AC Characteristics

(64Mb pSRAM Page Mode)

3 Volt	Symbol	Parameter	Page Mode		
		Performance Grade	-70		
		Density	64Mb pSRAM		
	Symbol	Parameter	Min	Max	Units
Read	trc	Read cycle time	70	20k	ns
	taa	Address Access Time		70	ns
	tco	Chip select to output		70	ns
	toe	Output enable to valid output		25	ns
	tba	UB#, LB# Access time		70	ns
	tlz	Chip select to Low-z output	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns
	tolz	Output enable to Low-Z output	5		ns
	thz	Chip enable to High-Z output	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	5	ns
	tohz	Output disable to High-Z output	0	5	ns
	toh	Output hold from Address Change	5		ns

			Page Mode		
	Performance Grade		-70		
	Density		64Mb pSRAM		
3 Volt	**Symbol**	**Parameter**	**Min**	**Max**	**Units**
	twc	Write cycle time	70	20k	ns
	tcw	Chipselect to end of write	60		ns
	tas	Address set up Time	0		ns
	taw	Address valid to end of write	60		ns
	tbw	UB#, LB# valid to end of write	60		ns
	twp	Write pulse width	50	20k	ns
Write	twr	Write recovery time	0		ns
	twhz	Write to output High-Z		5	ns
	tdw	Data to write time overlap	20		ns
	tdh	Data hold from write time	0		ns
	tow	End write to output Low-Z	5		
	tow	Write high pulse width	7.5		ns
	tpc	Page read cycle	20	20k	ns
Other	tpa	Page address access time		20	ns
	twpc	Page write cycle	20	20k	ns
	tcp	Chip select high pulse width	10		ns

Timing Diagrams

Read Cycle
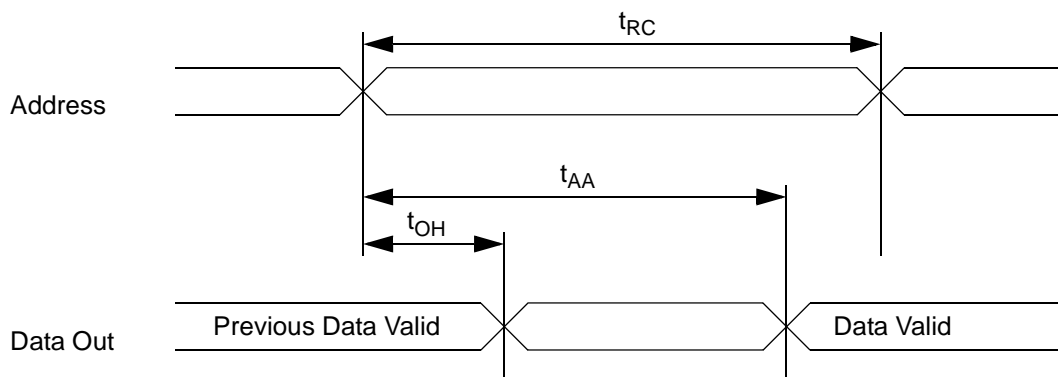
Figure 33.   Timing of Read Cycle (CE# = OE# = V$_{IL}$, WE# = ZZ# = V$_{IH}$)

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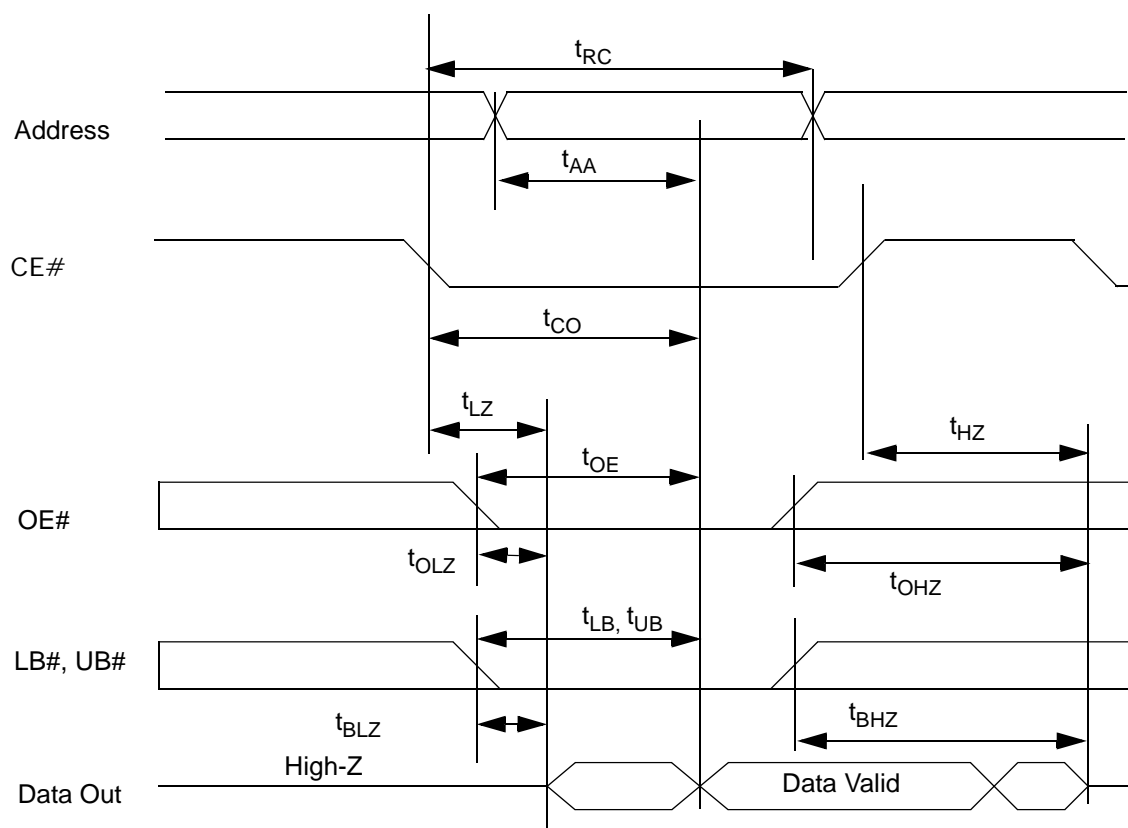
Figure 34.   Timing Waveform of Read Cycle (WE# = ZZ# = V$_{IH}$)
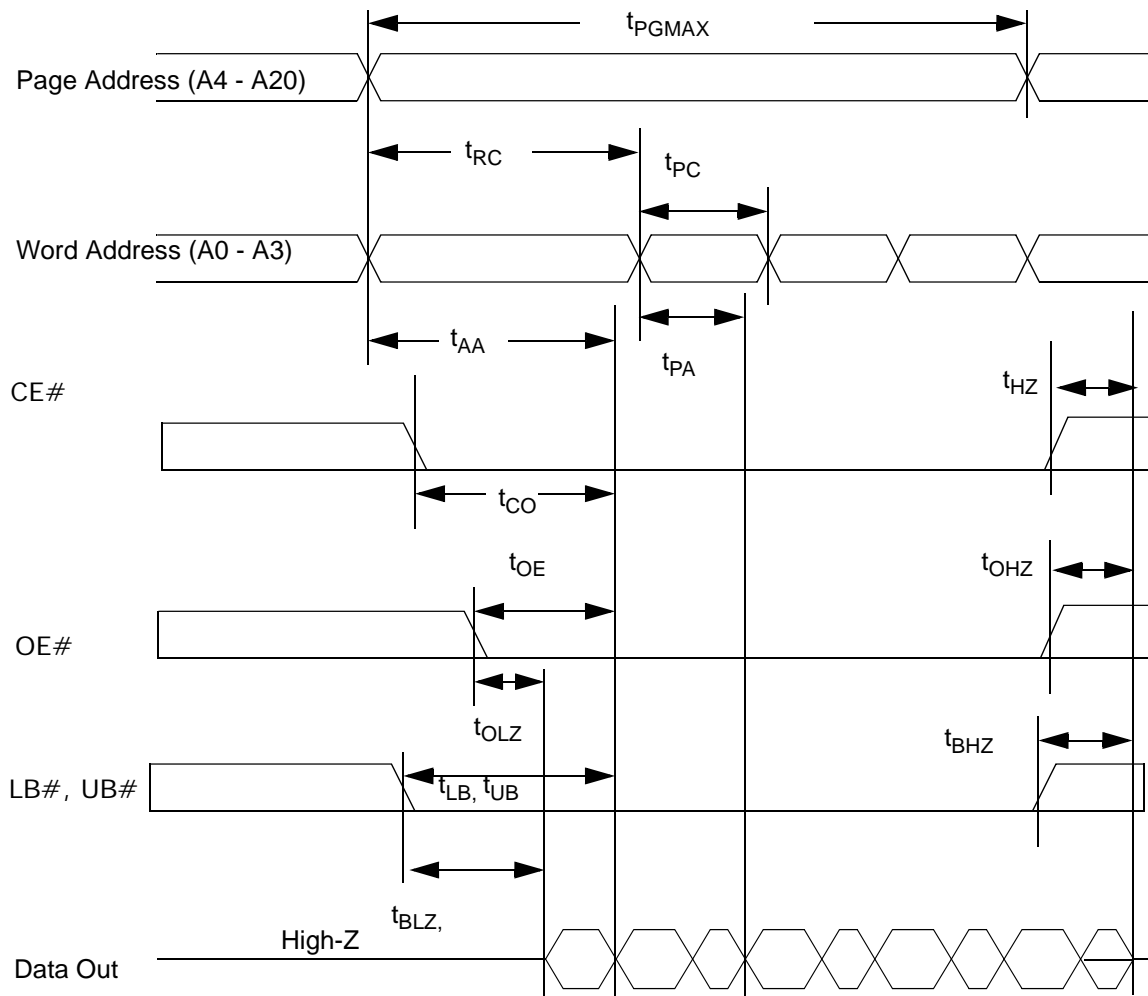
Figure 35.   Timing Waveform of Page Mode Read Cycle (WE# = ZZ# = V$_{IH}$)

Write Cycle
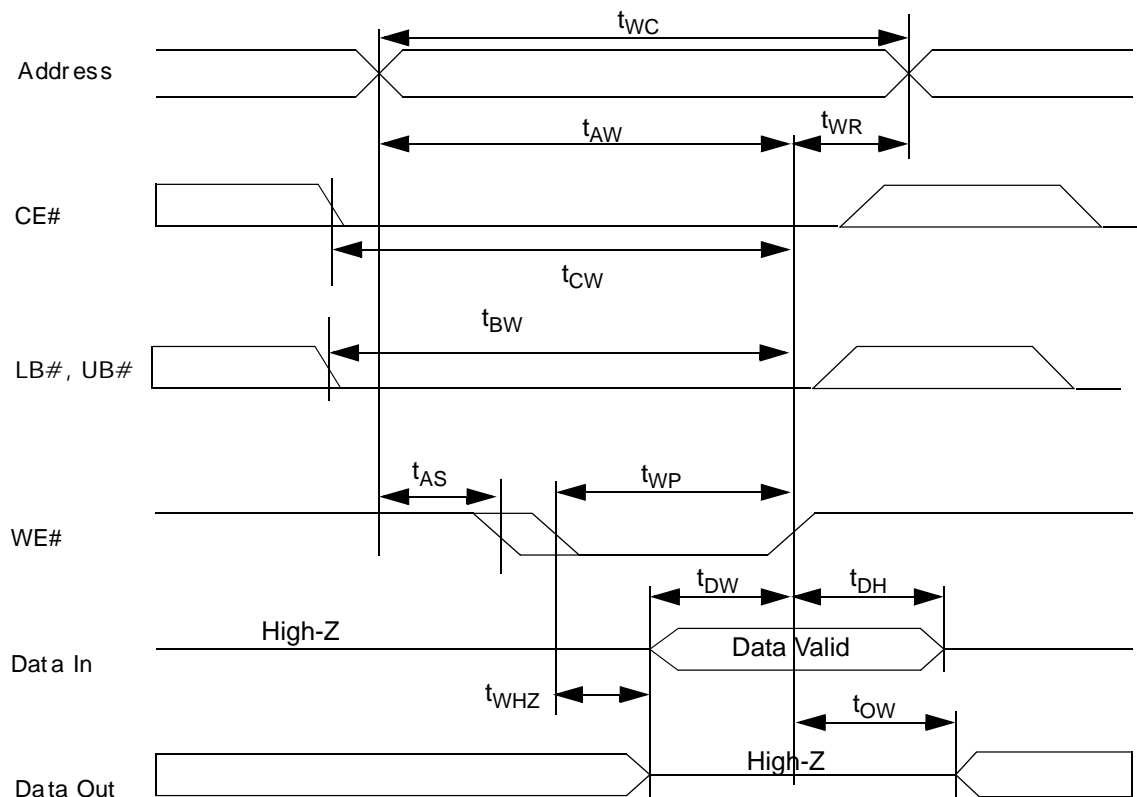
Figure 36.   Timing Waveform of Write Cycle (WE# Control, ZZ# = V$_{IH}$)
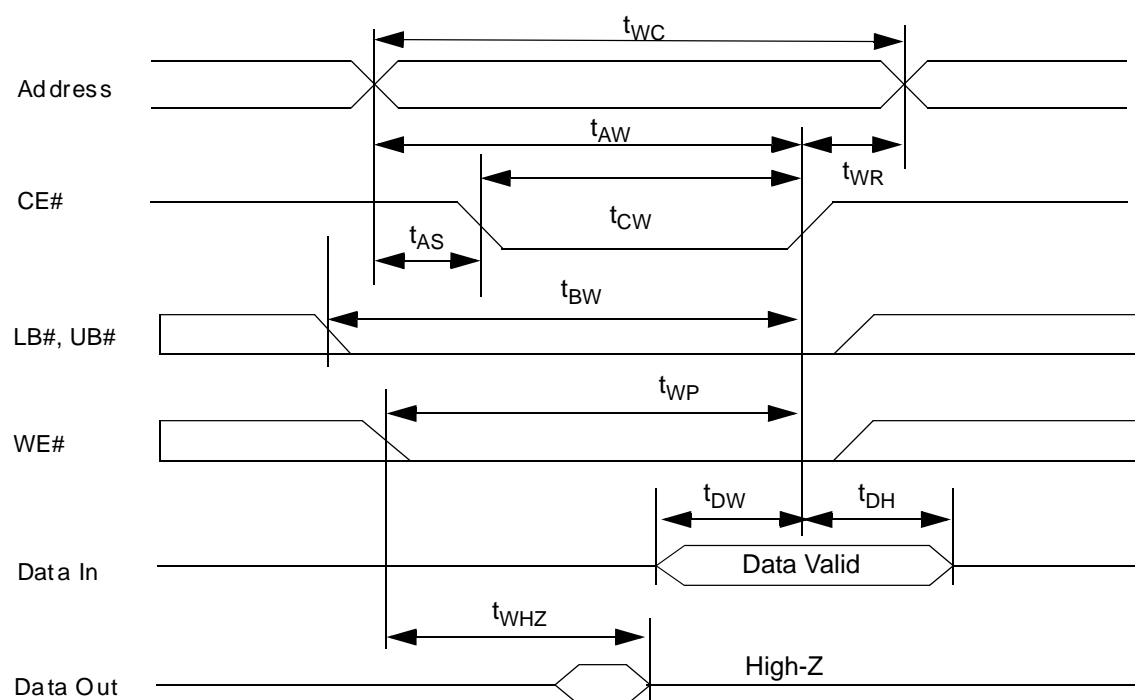
Figure 37.   Timing Waveform of Write Cycle (CE# Control, ZZ# = V$_{IH}$)
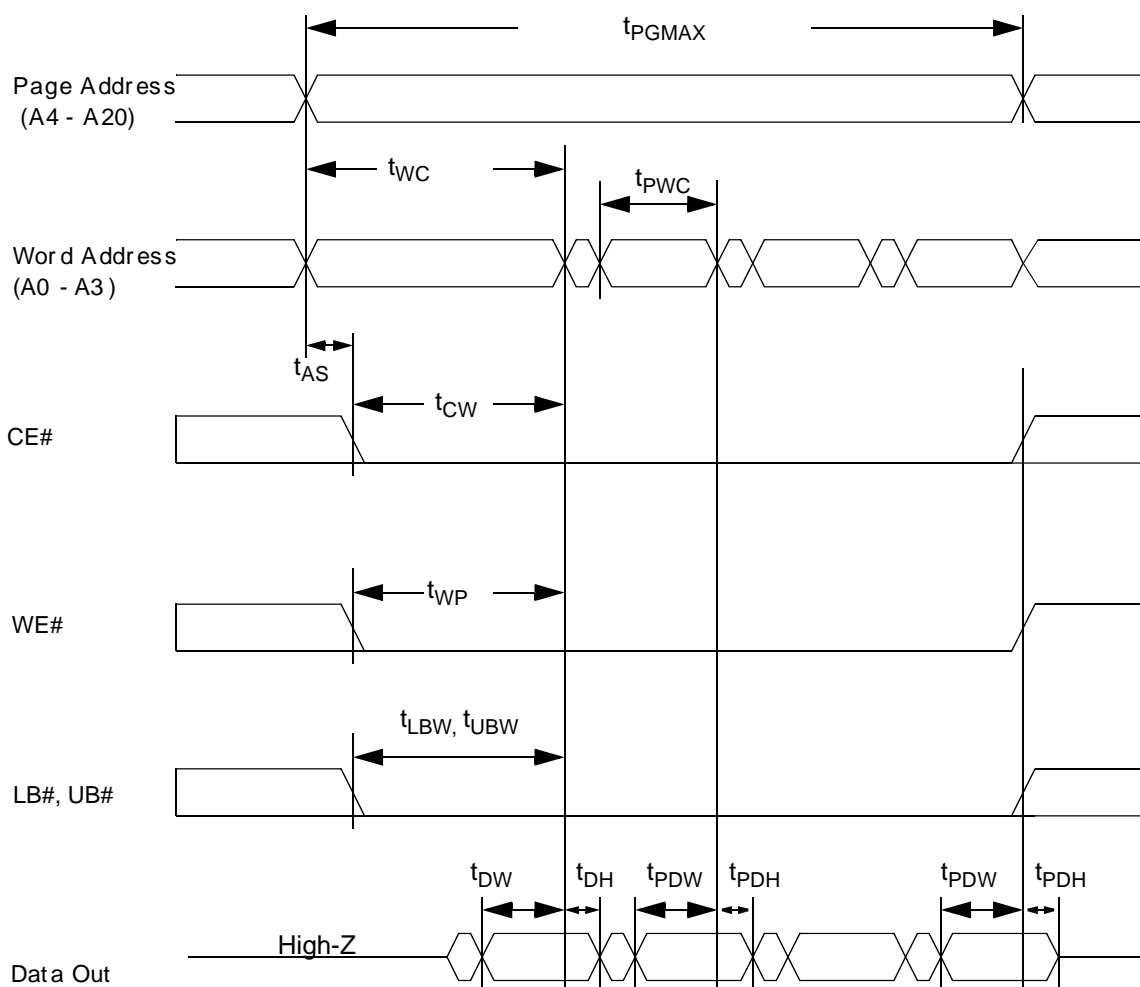
Figure 38.   Timing Waveform of Page Mode Write Cycle (ZZ# = V$_{IH}$)

Power Savings Modes (For l6M Page Mode, 32M and 64M Only)

There are several power savings modes.

- Partial Array Self Refresh
- Temperature Compensated Refresh (64M)
- Deep Sleep Mode
- Reduced Memory Size (32M, 16M)

The operation of the power saving modes ins controlled by the settings of bits contained in the Mode Register. This definition of the Mode Register is shown in Figure 39 and the various bits are used to enable and disable the various low power modes as well as enabling Page Mode operation. The Mode Register is set by using the timings defined in Figure xxx.

Partial Array Self Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 16Mb, 32Mb, or 48Mb portion of the array. The array partition to be refreshed is determined by the respective bit settings in the Mode Register. The register settings for the PASR operation are defined in Table xxx. In this PASR mode, when ZZ# is active low, only the portion of the array that is set in the register is re-

freshed. The data in the remainder of the array will be lost. The PASR operation mode is only available during standby time (ZZ# low) and once ZZ# is returned high, the device resumes full array refresh. All future PASR cycles will use the contents of the Mode Register that has been previously set. To change the address space of the PASR mode, the Mode Register must be reset using the previously defined procedures. For PASR to be activated, the register bit, A4 must be set to a one (1) value, "PASR Enabled". If this is the case, PASR will be activated 10 µs after ZZ# is brought low. If the A4 register bit is set equal to zero (0), PASR will not be activated.

Temperature Compensated Refresh (for 64Mb)

In this mode of operation, the internal refresh rate can be optimized for the operation temperature used and this can then lower standby current. The DRAM array in the PSRAM must be refreshed internally on a regular basis. At higher temperatures, the DRAM cell must be refreshed more often than at lower temperatures. By setting the temperature of operation in the Mode Register, this refresh rate can be optimized to yield the lowest standby current at the given operating temperature. There are four different temperature settings that can be programmed in to the PSRAM. These are defined in Figure 39.

Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing ZZ# low with the A4 register bit set to a zero (0), "Deep Sleep Enabled". If this is the case, Deep Sleep will be entered 10 µs after ZZ# is brought low. The device will remain in this mode as long as ZZ# remains low. If the A4 register bit is set equal to one (1), Deep Sleep will not be activated.

Reduced Memory Size (for 32M and 16M)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb or 16Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the following timings and the bit settings in the table "Address Patterns for RMS". The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures. While operating in the RMS mode, the unselected portion of the array may not be used.

Other Mode Register Settings (for 64M)

The Page Mode operation can also be enabled and disabled using the Mode Register. Register bit A7 controls the operation of Page Mode and setting this bit to a one (1), enables Page Mode. If the register bit A7 is set to a zero (0), Page Mode operation is disabled.
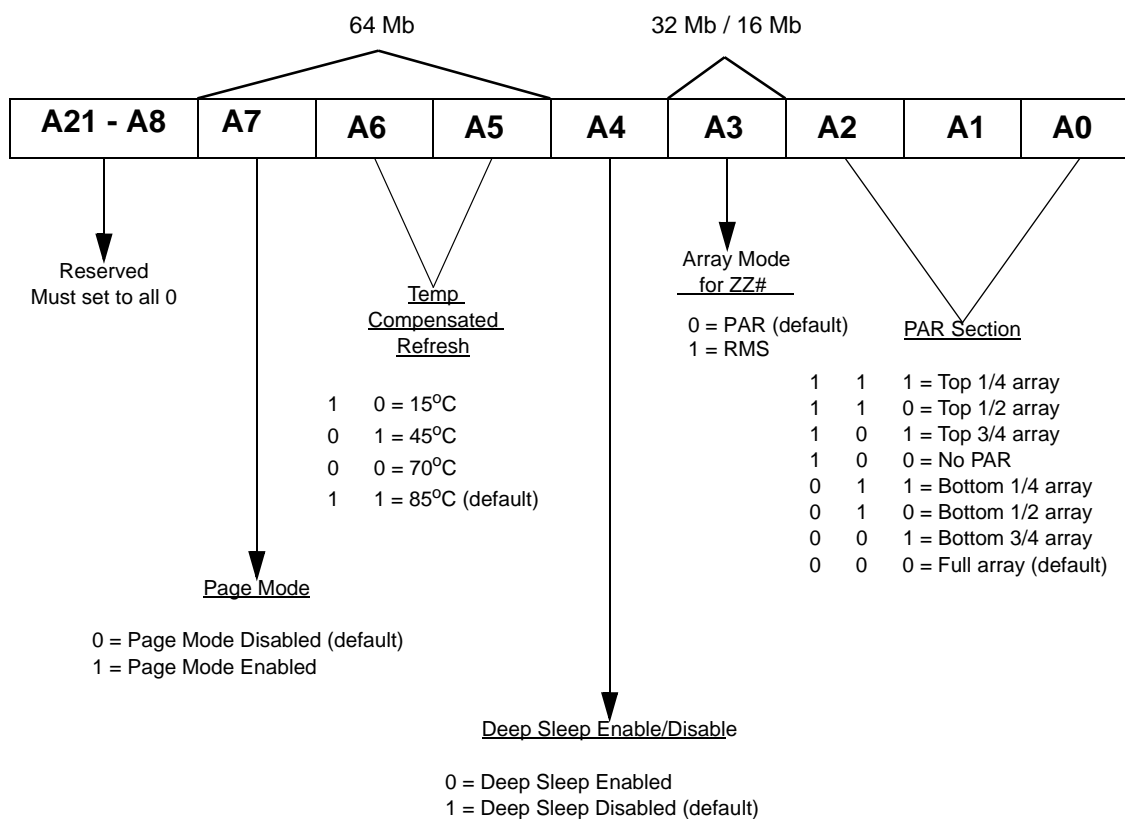
Figure 39.   Mode Register
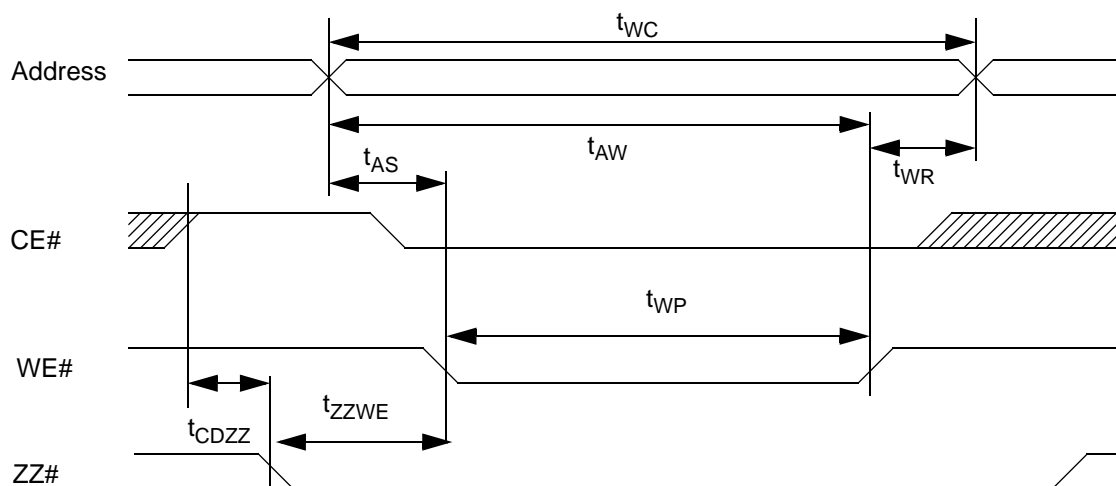
Figure 40.   Mode Register Update Timings (UB#, LB#, OE# are Don't Care)

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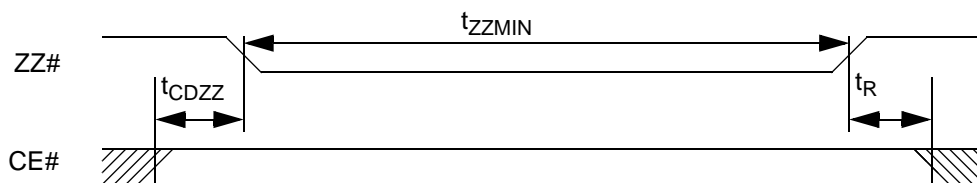
Figure 41.   Deep Sleep Mode - Entry/Exit Timings (for 64M)
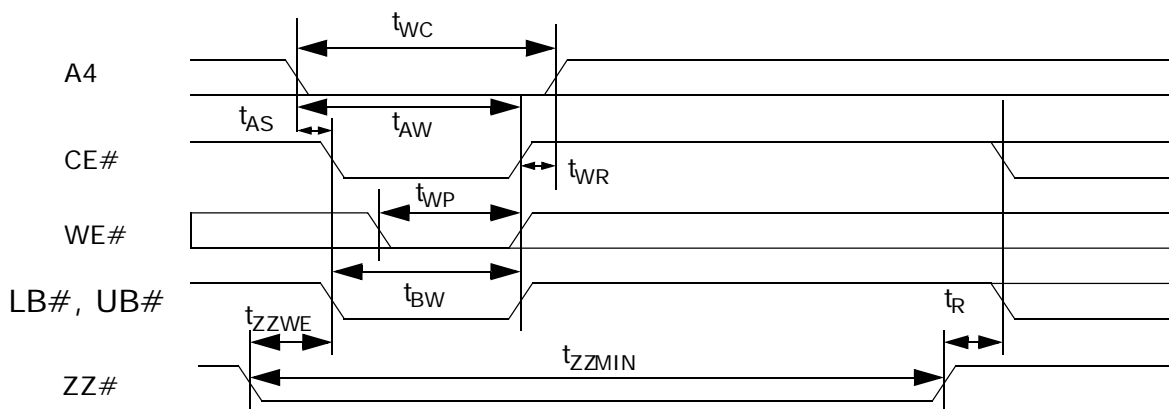
Figure 42.   Deep Sleep Mode - Entry/Exit Timings (for 32M and 16M)

Mode Register Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit	Note
Chip deselect to ZZ# low	t_{CDZZ}	5		ns	
ZZ# low to WE# low	t_{ZZWE}	10	500	ns	
Write register cycle time	t_{WC}	70/85		ns	1
Chip enable to end of write	t_{CW}	70/85		ns	1
Address valid to end of write	t_{AW}	70/85		ns	1
Write recovery time	t_{WR}	0		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WR}	40		ns	
Deep Sleep Pulse Width	t_{ZZMIN}	10		µs	
Deep Sleep Recovery	t_R	200		µs	

Notes:
1. Minimum cycle time for writing register is equal to speed grade of product.

Address Patterns for PASR (A4=1) (64M)

A2	A1	A0	Active Section	Address Space	Size	Density
1	1	1	Top quarter of die	300000h-3FFFFFh	1Mb x 16	16Mb
1	1	0	Top half of die	200000h-3FFFFFh	2Mb x 16	32Mb
1	0	1	Reserved			
1	0	0	No PASR	None	0	0
0	1	1	Bottom quarter of die	000000h-0FFFFFh	1Mb x 16	16Mb
0	1	0	Bottom half of die	000000h-1FFFFFh	2Mb x 16	32Mb
0	0	1	Reserved			
0	0	0	Full array	000000h-3FFFFFh	4Mb x 16	64Mb

Deep ICC Characteristics (for 64Mb)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PASR Mode Standby Current	I_{PASR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85°C$	None		10	µA
			1/4 Array		60	
			1/2 Array		80	
			Full Array		120	

Item	Symbol	Max Temperature	Typ	Max	Unit
Temperature Compensated Refresh Current	I_{TCR}	15°C		50	µA
		45°C		60	
		70°C		80	
		85°C		120	

Item	Symbol	Test	Typ	Max	Unit
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in ZZ# mode, $t_A = 25°C$		10	µA

Address Patterns for PAR (A3= 0, A4=1) (32M)

A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
x	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

Address Patterns for RMS (A3 = 1, A4 = 1) (32M)

A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

Low Power ICC Characteristics (32M)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85°C$	1/4 Array		75	µA
			1/2 Array		90	µA
RMS Mode Standby Current	I_{RMSSB}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85°C$	8Mb Device		75	µA
			16Mb Device		90	µA
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in $\overline{ZZ}$ mode, $t_A = 85°C$			10	µA

Address Patterns for PAR (A3= 0, A4=1) (16M)

A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	00000h - 0FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
x	0	0	Full die	00000h - FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	C0000h - FFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - 1FFFFFh	512Kb x 16	8Mb

Address Patterns for RMS (A3 = 1, A4 = 1) (16M)

A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	00000h - 0FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
1	1	1	One-quarter of die	C0000h - FFFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - FFFFFh	512Kb x 16	8Mb

Low Power ICC Characteristics (16M)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85°C$	1/4 Array		65	µA
			1/2 Array		80	
RMS Mode Standby Current	I_{RMSSB}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85°C$	4Mb Device		65	µA
			8Mb Device		80	
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in ZZ# mode, $t_A = 85°C$			10	µA

Type 2 pSRAM
16Mbit (1M Word x 16-bit)
32Mbit (2M Word x 16-bit)
64Mbit (4M Word x 16-bit)
128Mbit (8M Word x 16-bit)

Features

- Process Technology: CMOS
- Organization: x16 bit
- Power Supply Voltage: 2.7~3.1V
- Three State Outputs
- Compatible with Low Power SRAM

Product Information

Density	V_{CC} Range	Standby (ISBI, Max.)	Operating (ICC2, Max.)	Mode
16Mb	2.7-3.1V	80 µA	30 mA	Dual CS
16Mb	2.7-3.1V	80 µA	35 mA	Dual CS and Page Mode
32Mb	2.7-3.1V	100 µA	35 mA	Dual CS
32Mb	2.7-3.1V	100 µA	40 mA	Dual CS and Page Mode
64Mb	2.7-3.1V	TBD	TBD	Dual CS
64Mb	2.7-3.1V	TBD	TBD	Dual CS and Page Mode
128Mb	2.7-3.1V	TBD	TBD	Dual CS and Page Mode

Pin Description

Pin Name	Description	I/O
CS1#, CS2	Chip Select	I
OE#	Output Enable	I
WE#	Write Enable	I
LB#, UB#	Lower/Upper Byte Enable	I
A0-A19 (16M) A0-A20 (32M) A0-A21 (64M) A0-A22 (128M)	Address Inputs	I
I/O0-I/O15	Data Inputs/Outputs	I/O
V_{CC}/V_{CCQ}	Power Supply	—
V_{SS}/V_{SSQ}	Ground	—
NC	Not Connection	—
DNU	Do Not Use	—

Power Up Sequence

1. Apply power.
2. Maintain stable power (V_{CC} min.=2.7V) for a minimum 200 µs with CS1#=high or CS2=low.

Timing Diagrams

Power Up
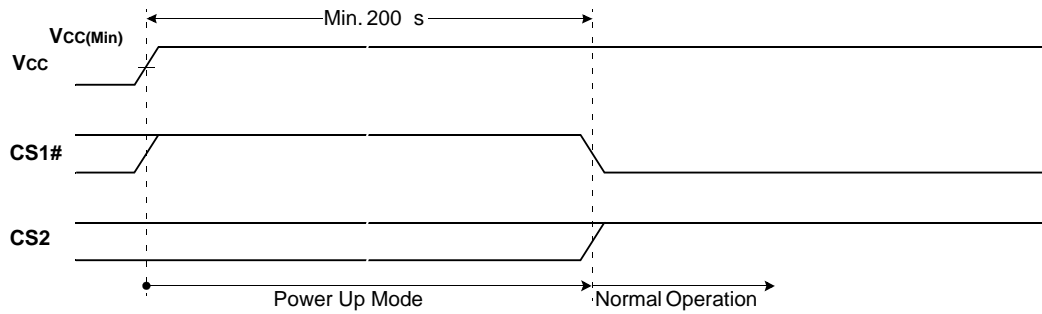
Figure 43.   Power Up 1 (CSI# Controlled)

Notes:
1. After V_{CC} reaches V_{CC}(Min.), wait 200 µs with CS1# high. Then the device gets into the normal operation.
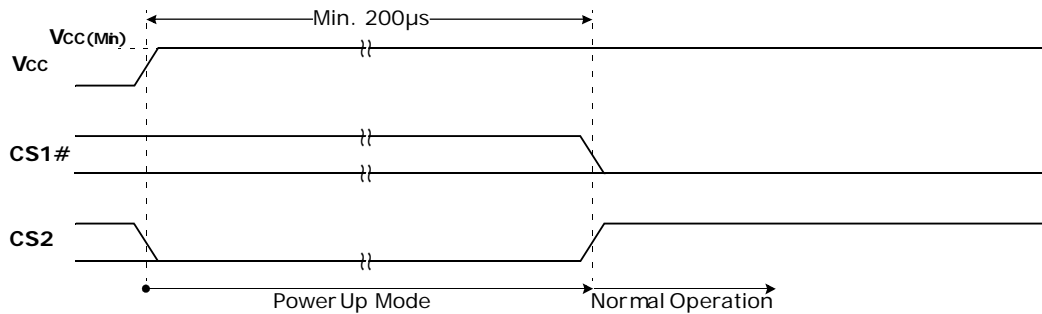
Figure 44.   Power Up 2 (CS2 Controlled)

Notes:
1. After V_{CC} reaches V_{CC}(Min.), wait 200 µs with CS2 low. Then the device gets into the normal operation.

Functional Description

Mode	CS1#	CS2	OE#	WE#	LB#	UB#	I/O$_{1-8}$	I/O$_{9-16}$	Power
Deselected	H	X	X	X	X	X	High-Z	High-Z	Standby
Deselected	X	L	X	X	X	X	High-Z	High-Z	Standby
Deselected	X	X	X	X	H	H	High-Z	High-Z	Standby
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	Active
Outputs Disabled	L	H	H	H	X	L	High-Z	High-Z	Active
Lower Byte Read	L	H	L	H	L	H	D$_{OUT}$	High-Z	Active
Upper Byte Read	L	H	L	H	H	L	High-Z	D$_{OUT}$	Active
Word Read	L	H	L	H	L	L	D$_{OUT}$	D$_{OUT}$	Active
Lower Byte Write	L	H	X	L	L	H	D$_{IN}$	High-Z	Active
Upper Byte Write	L	H	X	L	H	L	High-Z	D$_{IN}$	Active
Word Write	L	H	X	L	L	L	D$_{IN}$	D$_{IN}$	Active

Legend: X = Don't care (must be low or high state).

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V$_{SS}$	V$_{IN}$, V$_{OUT}$	-0.2 to V$_{CC}$+0.3V	V
Voltage on V$_{CC}$ supply relative to V$_{SS}$	V$_{CC}$	-0.2 to 3.6V	V
Power Dissipation	P$_D$	1.0	W
Operating Temperature	T$_A$	-40 to 85	°C

Notes:

1. *Stresses greater than those listed under "Absolute Maximum Ratings" section may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than one second may affect reliability.*

DC Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V$_{CC}$	Power Supply Voltage	2.7	2.9	3.1	V
V$_{SS}$	Ground	0	0	0	
V$_{IH}$	Input High Voltage	2.2	—	V$_{CC}$ + 0.3 (Note 2)	
V$_{IL}$	Input Low Voltage	-0.2 (Note 3)	—	0.6	

Notes:

1. *TA=-40 to 85°C, unless otherwise specified.*

2. *Overshoot: V$_{CC}$+1.0V in case of pulse width ≤ 20ns.*

3. *Undershoot: -1.0V in case of pulse width ≤ 20ns.*

4. *Overshoot and undershoot are sampled, not 100% tested.*

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Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	8	pF
C_{IO}	Input/Output Capacitance	V_{OUT} = 0V	—	10	pF

Note: This parameter is sampled periodically and is not 100% tested.

DC and Operating Characteristics

Common

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	—	1	μA
Output Leakage Current	I_{LO}	CS1#=V_{IH} or CS2=V_{IL} or OE#=V_{IH} or WE#=V_{IL} or LB#=UB#=V_{IH}, V_{IO}=V_{SS} to V_{CC}	-1	—	1	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA	2.4	—	—	V

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16M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	7	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	30	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			35	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	80	mA

Notes:
1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

32M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	7	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	35	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			40	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	100	mA

Notes:
1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

64M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1μs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	TBD	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	TBD	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			TBD	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	TBD	mA

Notes:
1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

128M pSRAM

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	TBD	mA
	I_{CC2}	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}	—	—	TBD	mA
Standby Current (CMOS)	I_{SB1} (Note 1)	Other inputs=0-V_{CC} 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	TBD	mA

Notes:
1. *Standby mode is supposed to be set up after at least one active operation after power up. I_{SB1} is measured after 60ms from the time when standby mode is set up.*

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AC Operating Conditions

Test Conditions (Test Load and Test Input/Output Reference)

- Input pulse level: 0.4 to 2.2V
- Input rising and falling time: 5ns
- Input and output reference voltage: 1.5V
- Output load (See Figure 45): CL=50pF
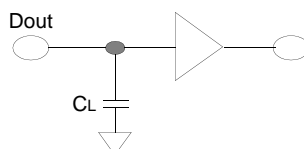
Figure 45.   Output Load

Note: *Including scope and jig capacitance.*

AC Characteristics (Ta = -40°C to 85°C, V_{CC} = 2.7 to 3.1 V)

	Symbol	Parameter	70ns Min	70ns Max	Unit
Read	t_{RC}	Read Cycle Time	70	—	ns
Read	t_{AA}	Address Access Time	—	70	ns
Read	t_{CO}	Chip Select to Output	—	70	ns
Read	t_{OE}	Output Enable to Valid Output	—	35	ns
Read	t_{BA}	UB#, LB# Access Time	—	70	ns
Read	t_{LZ}	Chip Select to Low-Z Output	10	—	ns
Read	t_{BLZ}	UB#, LB# Enable to Low-Z Output	10	—	ns
Read	t_{OLZ}	Output Enable to Low-Z Output	5	—	ns
Read	t_{HZ}	Chip Disable to High-Z Output	0	25	ns
Read	t_{BHZ}	UB#, LB# Disable to High-Z Output	0	25	ns
Read	t_{OHZ}	Output Disable to High-Z Output	0	25	ns
Read	t_{OH}	Output Hold from Address Change	5	—	ns
Read	t_{PC}	Page Cycle Time	25	—	ns
Read	t_{PA}	Page Access Time	—	20	ns
Write	t_{WC}	Write Cycle Time	70	—	ns
Write	t_{CW}	Chip Select to End of Write	60	—	ns
Write	t_{AS}	Address Set-up Time	0	—	ns
Write	t_{AW}	Address Valid to End of Write	60	—	ns
Write	t_{BW}	UB#, LB# Valid to End of Write	60	—	ns
Write	t_{WP}	Write Pulse Width	55 (Note 1)	—	ns
Write	t_{WR}	Write Recovery Time	0	—	ns
Write	t_{WHZ}	Write to Output High-Z	0	25	ns
Write	t_{DW}	Data to Write Time Overlap	30	—	ns
Write	t_{DH}	Data Hold from Write Time	0	—	ns
Write	t_{OW}	End Write to Output Low-Z	5	—	ns

Notes:
1. t_{WP} *(min)=70ns for continuous write operation over 50 times.*

Timing Diagrams

Read Timings
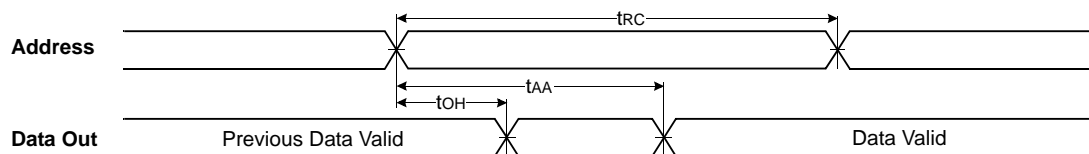
Figure 46.   Timing Waveform of Read Cycle(1)

Notes:
1. Address Controlled, CS1#=OE#=V_{IL}, CS2=WE#=V_{IH}, UB# and/or LB#=V_{IL}.
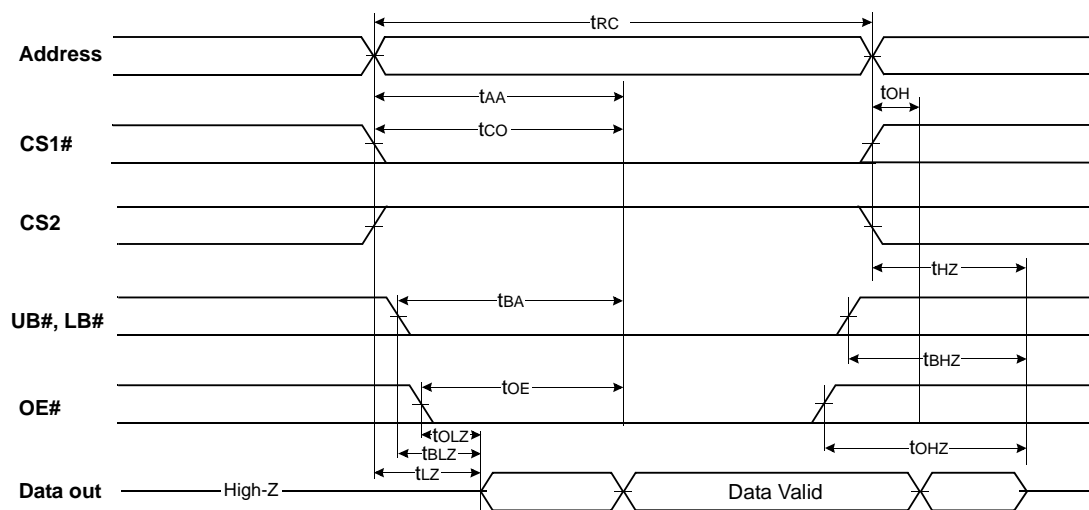
Figure 47.   Timing Waveform of Read Cycle(2)

Notes:
1.   WE#=V_{IH}.
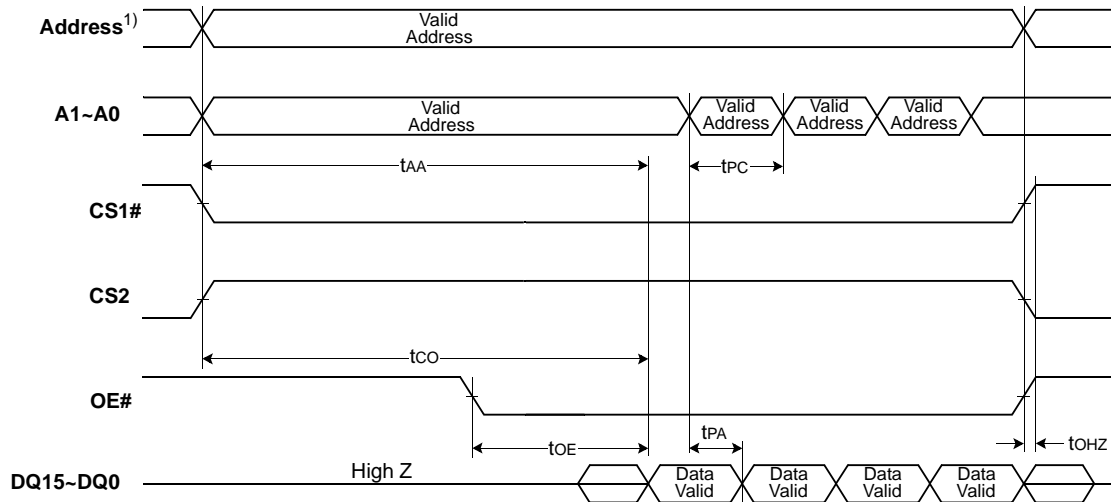
Figure 48.   Timing Waveform of Page Cycle (Page Mode Only)

Notes:

1. 16Mb: A2 ~ A19, 32Mb: A2 ~ A20, 64Mb: A2 ~ A21, 128Mb: A2 ~ A22.

    t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

    At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

    t_{OE}(max) is met only when OE# becomes enabled after t_{AA}(max).

    If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4µs, the device needs a normal read timing (t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4µs.

Write Timings
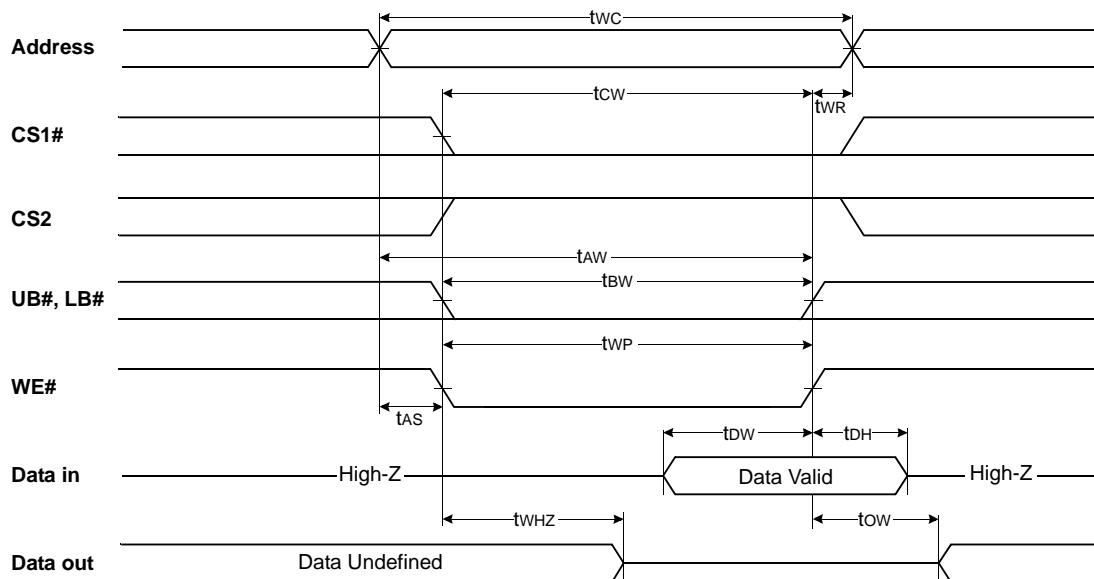
Figure 49.   Write Cycle #I (WE# Controlled)
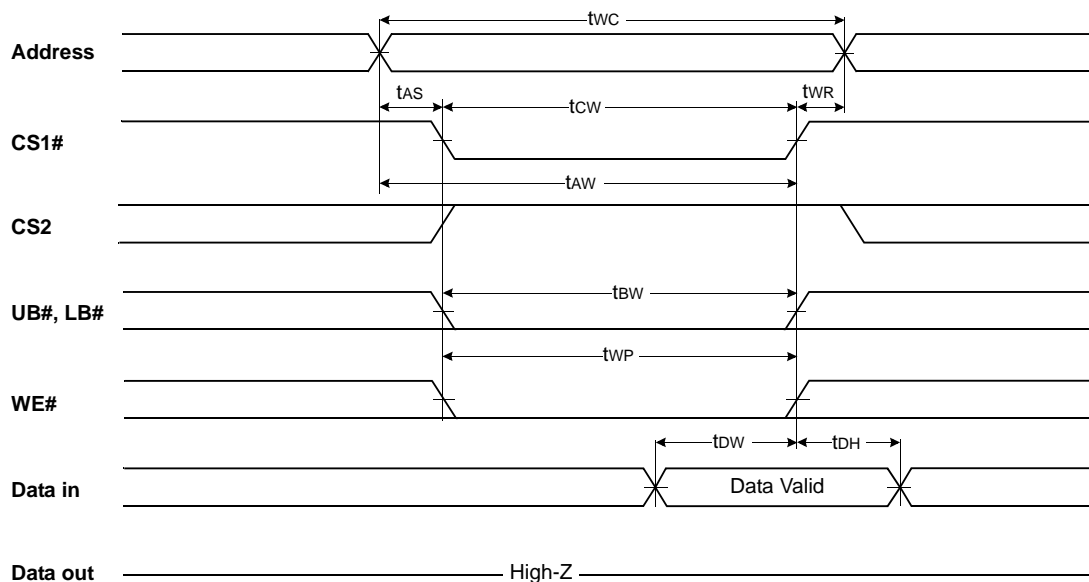
Figure 50.   Write Cycle #2 (CSI# Controlled)
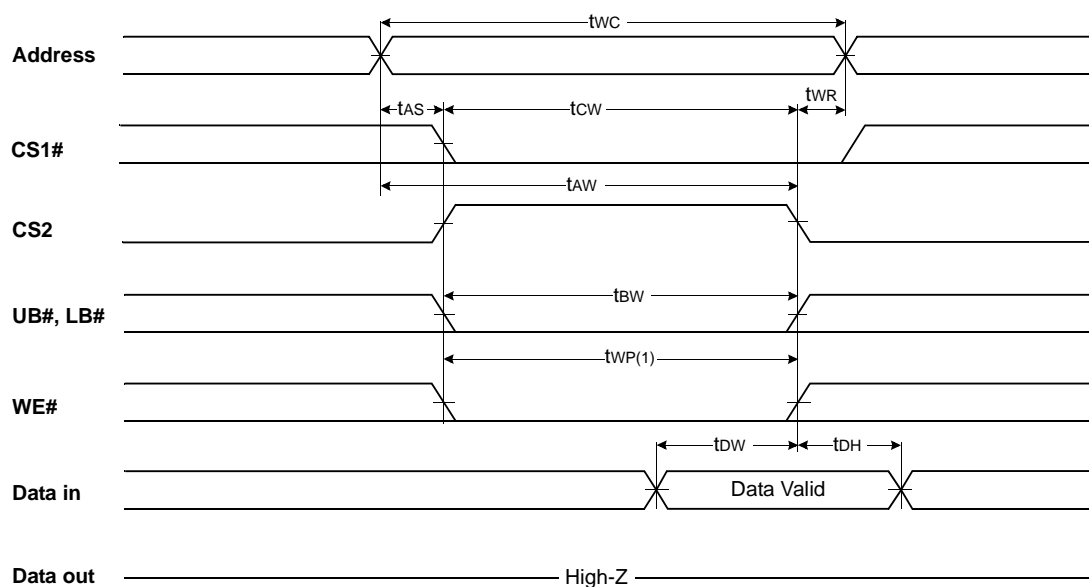
Figure 5I.   Timing Waveform of Write Cycle(3) (CS2 Controlled)
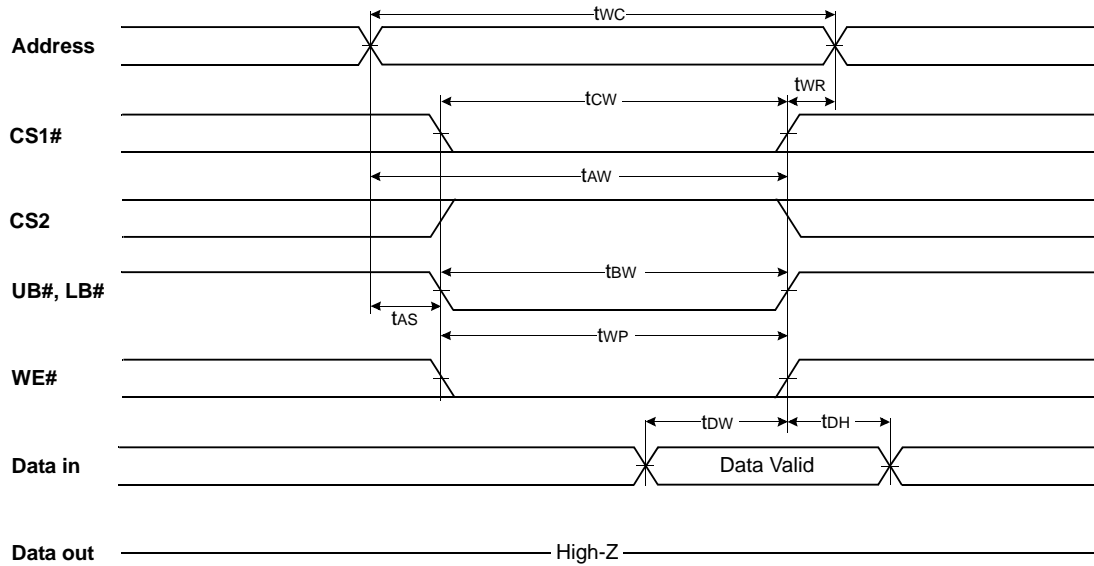
Figure 52.   Timing Waveform of Write Cycle(4) (UB#, LB# Controlled)

Notes:
1. *A write occurs during the overlap (t_{WP}) of low CS1# and low WE#. A write begins when CS1# goes low and WE# goes low with asserting UB# or LB# for single byte operation or simultaneously asserting UB# and LB# for double byte operation. A write ends at the earliest transition when CS1# goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

2. *t_{CW} is measured from the CS1# going low to the end of write.*

3. *t_{AS} is measured from the address valid to the beginning of write.*

4. *t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with CS1# or WE# going high.*

SPANSION™

pSRAM Type 7

16Mb (1M word x 16-bit)
32Mb (2M word x 16-bit)
64Mb (4M word x 16-bit)
CMOS 1M/2M/4M-Word x 16-bit Fast Cycle Random Access Memory with Low Power SRAM Interface

Features

- Asynchronous SRAM Interface
- Fast Access Time
  - tCE = tAA = 60ns max (16M)
  - tCE = tAA = 65ns max (32M/64M)
- 8 words Page Access Capability
  - tPAA = 20ns max (32M/64M)
- Low Voltage Operating Condition
  - VDD = +2.7V to +3.1V
- Wide Operating Temperature
  - TA = -30°C to +85°C
- Byte Control by LB and UB
- Various Power Down modes
  - Sleep (16M)
  - Sleep, 4M-bit Partial, or 8M-bit Partial (32M)
  - Sleep, 8M-bit Partial, or 16M-bit Partial (64M)

Pin Description

Pin Name	Description
A_{21} to A_0	Address Input: A_{19} to A_0 for 16M, A_{20} to A_0 for 32M, A_{21} to A_0 for 64M
CE1#	Chip Enable (Low Active)
CE2#	Chip Enable (High Active)
WE#	Write Enable (Low Active)
OE#	Output Enable (Low Active)
UB#	Upper Byte Control (Low Active)
LB#	Lower Byte Control (Low Active)
DQ_{16}-9	Upper Byte Data Input/Output
DQ_8-1	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

Functional Description

Mode	CE2#	CE1#	WE#	OE#	LB#	UB#	A_{21-0}	DQ_{8-1}	DQ_{16-9}
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable (Note 1)	H	L	H	H	X	X	Note 3	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)			H	L	H	L	Valid	High-Z	Output Valid
Read (Lower Byte)			H	L	L	H	Valid	Output Valid	High-Z
Read (Word)			H	L	L	L	Valid	Output Valid	Output Valid
No Write			L	H	H	H	Valid	Invalid	Invalid
Write (Upper Byte)			L	H	H	L	Valid	Invalid	Input Valid
Write (Lower Byte)			L	H	L	H	Valid	Input Valid	Invalid
Write (Word)			L	H	L	L	Valid	Input Valid	Input Valid
Power Down	L	X	X	X	X	X	X	High-Z	High-Z

Legend: $L = V_{IL}$, $H = V_{IH}$, X can be either V_{IL} or V_{IH}, High-Z = High Impedance.

Notes:

1. Should not be kept this logic condition longer than 1 ms. Please contact local Spansion representative for the relaxation of 1ms limitation.

2. Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of the Power-Down Program, 16M has data retention in all modes except Power Down. Refer to Power Down for details.

3. Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

Power Down (for 32M, 64M Only)

Power Down

The Power Down is a low-power idle state controlled by CE2. CE2 Low drives the device in power-down mode and maintains the low-power idle state as long as CE2 is kept Low. CE2 High resumes the device from power-down mode. These devices have three power-down modes. These can be programmed by series of read/write operation. Each mode has following features.

32M			64M		
Mode	Retention Data	Retention Address	Mode	Retention Data	Retention Address
Sleep (default)	No	N/A	Sleep (default)	No	N/A
4M Partial	4M bit	00000h to 3FFFFh	8M Partial	8M bit	00000h to 7FFFFh
8M Partial	8M bit	00000h to 7FFFFh	16M Partial	16M bit	00000h to FFFFFh

The default state is Sleep and it is the lowest power consumption but all data is lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

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Power Down Program Sequence

The program requires 6 read/write operations with a unique address. Between each read/write operation requires that device be in standby mode. The following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	3FFFFFh (MSB)	Read Data (RDa)
2nd	Write	3FFFFFh	RDa
3rd	Write	3FFFFFh	RDa
4th	Write	3FFFFFh	Don't Care (X)
5th	Write	3FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle reads from the most significant address (MSB).

The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled, and the data written by the second or third cycle is valid as a normal write operation.

The fourth and fifth cycles write to MSB. The data from the fourth and fifth cycles is "don't care." If the fourth or fifth cycles are written into different address, the program is also cancelled but write data might not be written as normal write operation.

The last cycle is to read from specific address key for mode selection.

Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in memory cell array can be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

Address Key

The address key has following format.

Mode		Address				
32M	**64M**	**A2I**	**A20**	**AI9**	**AI8 - A0**	**Binary**
Sleep (default)	Sleep (default)	1	1	1	1	3FFFFFh
4M Partial	N/A	1	1	0	1	37FFFFh
8M Partial	8M Partial	1	0	1	1	2FFFFFh
N/A	16M Partial	1	0	0	1	27FFFFh

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions (See Warning Below)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.7	3.1	V
	V_{SS}	0	0	V
High Level Input Voltage (Note 1)	V_{IH}	V_{DD} 0.8	V_{DD}+0.2	V
High Level Input Voltage (Note 1)	V_{IL}	-0.3	V_{DD} 0.2	V
Ambient Temperature	T_A	-30	85	°C

Notes:

1. Maximum DC voltage on input and I/O pins is $V_{DD}+0.2V$. During voltage transitions, inputs can positive overshoot to $V_{DD}+1.0V$ for periods of up to 5 ns.

2. Minimum DC voltage on input or I/O pins is -0.3V. During voltage transitions, inputs can negative overshoot V_{SS} to -1.0V for periods of up to 5ns.

WARNING: *Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.*

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges can adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Package Capacitance

Test conditions: T_A = 25°C, f = 1.0 MHz

Symbol	Description	Test Setup	Typ	Max	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IN2}	Control Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V	—	8	pF

DC Characteristics

(Under Recommended Conditions Unless Otherwise Noted)

Parameter	Symbol	Test Conditions		16M Min.	16M Max.	32M Min.	32M Max.	64M Min.	64M Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}		-1.0	+1.0	-1.0	+1.0	-1.0	+1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DD}, Output Disable		-1.0	+1.0	-1.0	+1.0	-1.0	+1.0	μA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}(min)$, $I_{OH} = -0.5mA$		2.2	—	2.4	—	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 1mA$		—	0.4	—	0.4	—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, $CE2 \leq 0.2$ V	SLEEP		10	—	10	—	10	μA
	I_{DDP4}		4M Partial	N/A	N/A	—	40	N/A	N/A	μA
	I_{DDP8}		8M Partial	N/A	N/A	—	50	—	80	μA
	I_{DDP16}		16M Partial	N/A	N/A	N/A	N/A	—	100	μA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL} $CE1 = CE2 = V_{IH}$		—	1	—	1.5	—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ max., $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{DD} - 0.2V$, $\overline{CE1} = CE2 \geq V_{DD} - 0.2V$	TA< +85°C	—	100	—	80	—	170	μA
			TA< +40°C						90	μA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, $CE1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0mA$	t_{RC} / t_{WC} = min.	—	20	—	30	—	40	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1μs	—	3	—	3	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, $CE1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0mA$, t_{PRC} = min.		N/A	N/A	—	10	—	10	mA

Notes:

1. All voltages are referenced to V_{SS}.

2. DC Characteristics are measured after following POWER-UP timing.

3. I_{OUT} depends on the output load conditions.

AC Characteristics

(Under Recommended Operating Conditions Unless Otherwise Noted)

Read Operation

Parameter	Symbol	16M		32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	70	1000	65	1000	65	1000	ns	1, 2
CE1# Access Time	t_{CE}	—	60	—	65	—	65	ns	3
OE# Access Time	t_{OE}	—	40	—	40	—	40	ns	3
Address Access Time	t_{AA}	—	60	—	65	—	65	ns	3, 5
LB# / UB# Access Time	t_{BA}	—	30	—	30	—	30	ns	3
Page Address Access Time	t_{PAA}	N/A		—	20	—	20	ns	3,6
Page Read Cycle Time	t_{PRC}	N/A		20	1000	20	1000	ns	1, 6, 7
Output Data Hold Time	t_{OH}	5	—	5	—	5	—	ns	3
CE1# Low to Output Low-Z	t_{CLZ}	5	—	5	—	5	—	ns	4
OE# Low to Output Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	4
LB# / UB# Low to Output Low-Z	t_{BLZ}	0	—	0	—	0	—	ns	4
CE1# High to Output High-Z	t_{CHZ}	—	20	—	20	—	20	ns	3
OE# High to Output High-Z	t_{OHZ}	—	20	—	14	—	14	ns	3
LB# / UB# High to Output High-Z	t_{BHZ}	—	20	—	20	—	20	ns	3
Address Setup Time to CE1# Low	t_{ASC}	–6	—	–6	—	–6	—	ns	
Address Setup Time to OE# Low	t_{ASO}	10	—	10	—	10	—	ns	
Address Invalid Time	t_{AX}	—	10	—	10	—	10	ns	5, 8
Address Hold Time from CE1# High	t_{CHAH}	-6	—	–6	—	–6	—	ns	9
Address Hold Time from OE# High	t_{OHAH}	-6	—	–6	—	–6	—	ns	
WE# High to OE# Low Time for Read	t_{WHOL}	10	1000	12	—	25	—	ns	10
CE1# High Pulse Width	t_{CP}	10	—	12	—	12	—	ns	

Notes:

1. *Maximum value is applicable if CE#1 is kept at Low without change of address input of A3 to A21. If needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Address should not be changed within minimum t_{RC}.*
3. *The output load 50 pF with 50 ohm termination to V_{DD} x 0.5 (16M), The output load 50 pF (32M and 64M).*
4. *The output load 5pF.*
5. *Applicable to A3 to A21 (32M and 64M) when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 (32M and 64M) when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.*
8. *Applicable when at least two of address inputs among applicable are switched from previous state.*
9. *t_{RC}(min) and t_{PRC}(min) must be satisfied.*
10. *If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read can become longer by the amount of subtracting the actual value from the specified minimum value.*

AC Characteristics

Write Operation

Parameter	Symbol	16M		32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	70	1000	65	1000	65	1000	ns	1,2
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	3
CE1# Write Pulse Width	t_{CW}	45	—	40	—	40	—	ns	3
WE# Write Pulse Width	t_{WP}	45	—	40	—	40	—	ns	3
LB#/UB# Write Pulse Width	t_{BW}	45	—	40	—	40	—	ns	3
LB#/UB# Byte Mask Setup Time	t_{BS}	-5	—	–5	—	–5	—	ns	4
LB#/UB# Byte Mask Hold Time	t_{BH}	-5	—	–5	—	–5	—	ns	5
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	6
CE1# High Pulse Width	t_{CP}	10	—	12	—	12	—	ns	
WE# High Pulse Width	t_{WHP}	7.5	1000	7.5	1000	7.5	1000	ns	7
LB#/UB# High Pulse Width	t_{BHP}	10	1000	12	1000	12	1000	ns	
Data Setup Time	t_{DS}	15	—	12	—	12	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
OE# High to CE1# Low Setup Time for Write	t_{OHCL}	-5	—	–5	—	–5	—	ns	8
OE# High to Address Setup Time for Write	t_{OES}	0	—	0	—	0	—	ns	9
LB# and UB# Write Pulse Overlap	t_{BWO}	30	—	30	—	30	—	ns	

Notes:
1. *Maximum value is applicable if CE1# is kept at Low without any address change. If the relaxation is needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB#/UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB#/UB#, whichever occurs first.*
7. *t_{WPH} minimum is absolute minimum value for device to detect High level. And it is defined at minimum V_{IH} level.*
8. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other words, OE# must be brought to High within 5ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.*
9. *If OE# is Low after new address input, read cycle is initiated. In other word, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z.*

AC Characteristics

Power Down Parameters

Parameter	Symbol	16M		32M		64M		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	10	—	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	80	—	65	—	65	—	ns	
CE1# High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	300	—	300	—	µs	1
CE1# High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	N/A		1	—	1	—	µs	2
CE1# High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	0	—	0	—	ns	1

Notes:

1. Applicable also to power-up.

2. Applicable when 4Mb and 8Mb Partial modes are programmed.

Other Timing Parameters

Parameter	Symbol	16M		32M		64M		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CE1# High to OE# Invalid Time for Standby Entry	t_{CHOX}	10	—	10	—	10	—	ns	
CE1# High to WE# Invalid Time for Standby Entry	t_{CHWX}	10	—	10	—	10	—	ns	1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	50	—	50	—	µs	
CE1# High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	300	—	300	—	µs	
Input Transition Time	t_T	1	25	1	25	1	25	ns	2

Notes:

1. Some data might be written into any address location if t_{CHWX}(min) is not satisfied.

2. The Input Transition Time (t_T) at AC testing is 5ns as shown in below. If actual tT is longer than 5ns, it can violate the AC specification of some of the timing parameters.

AC Characteristics

AC Test Conditions

Symbol	Description	Test Setup	Value	Unit	Note
V_{IH}	Input High Level		$V_{DD} * 0.8$	V	
V_{IL}	Input Low Level		$V_{DD} * 0.2$	V	
V_{REF}	Input Timing Measurement Level		$V_{DD} * 0.5$	V	
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns	

AC Measurement Output Load Circuits
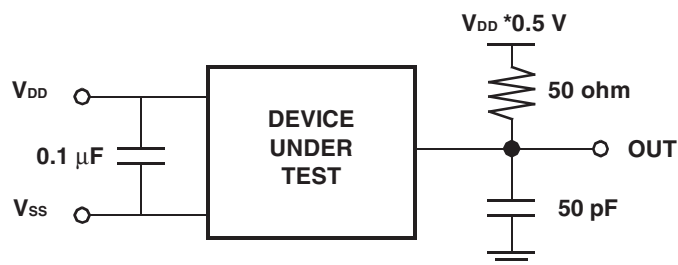
Figure 53. AC Output Load Circuit – 16 Mb
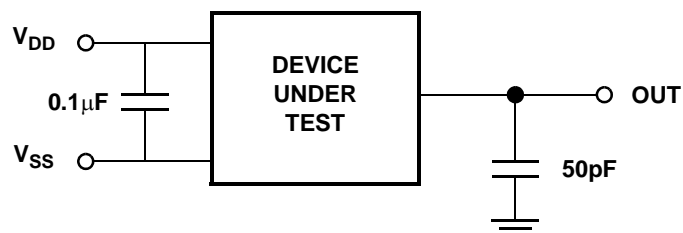
Figure 54. AC Output Load Circuit – 32 Mb and 64 Mb

Timing Diagrams

Read Timings
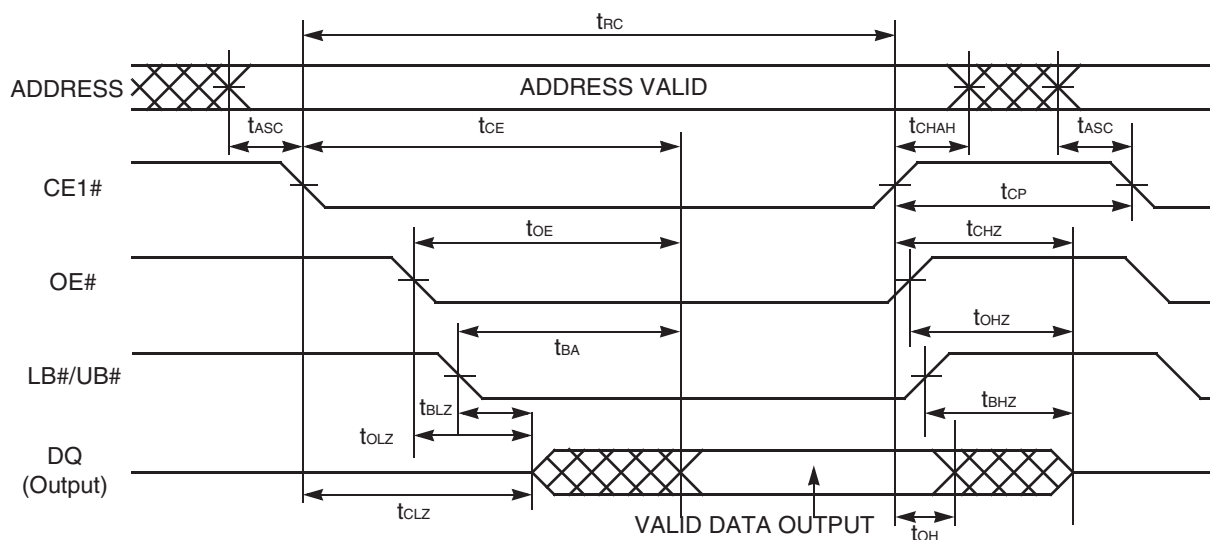
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 55.   Read Timing #I (Basic Timing)
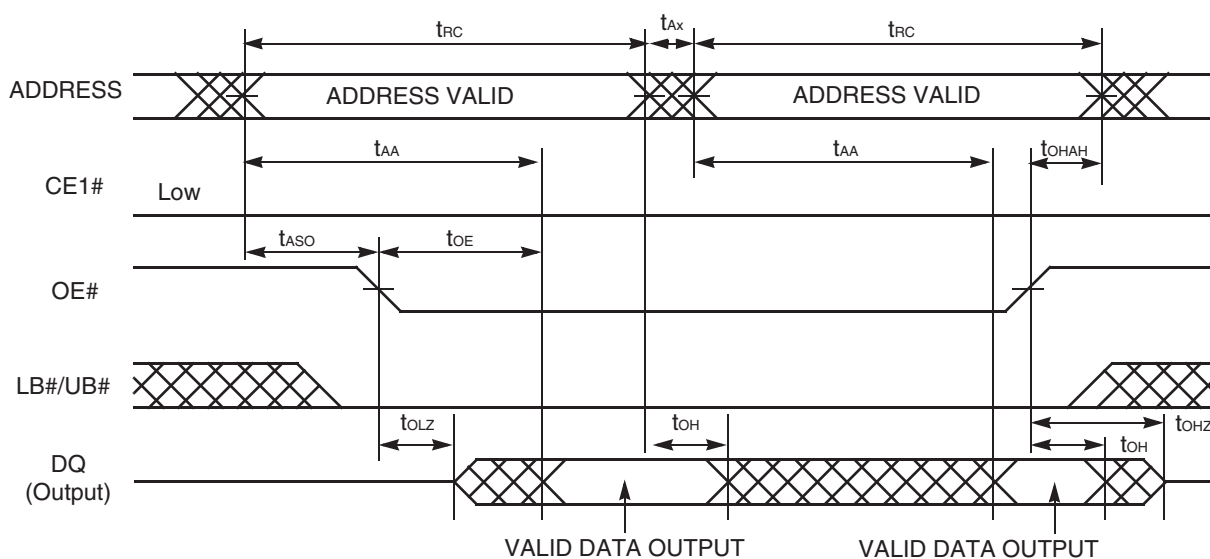
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 56.   Read Timing #2 (OE# Address Access
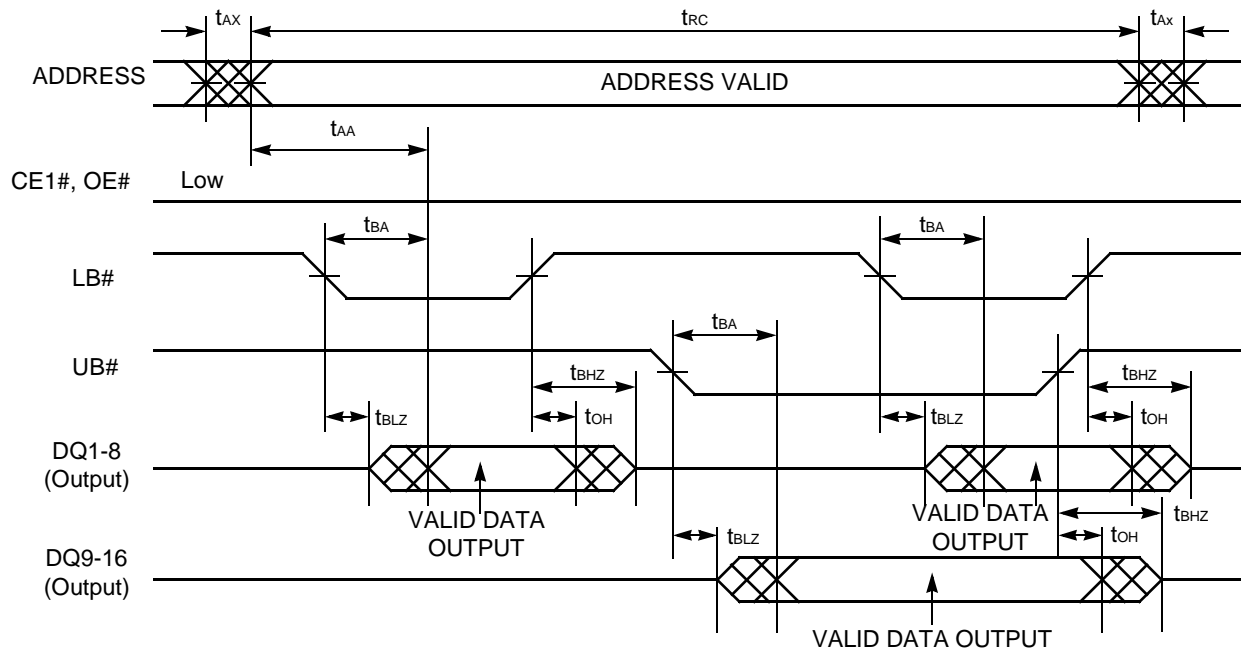
Note: This timing diagram assumes CE2=H and WE#=H.

Figure 57.   Read Timing #3 (LB#/UB# Byte Access)
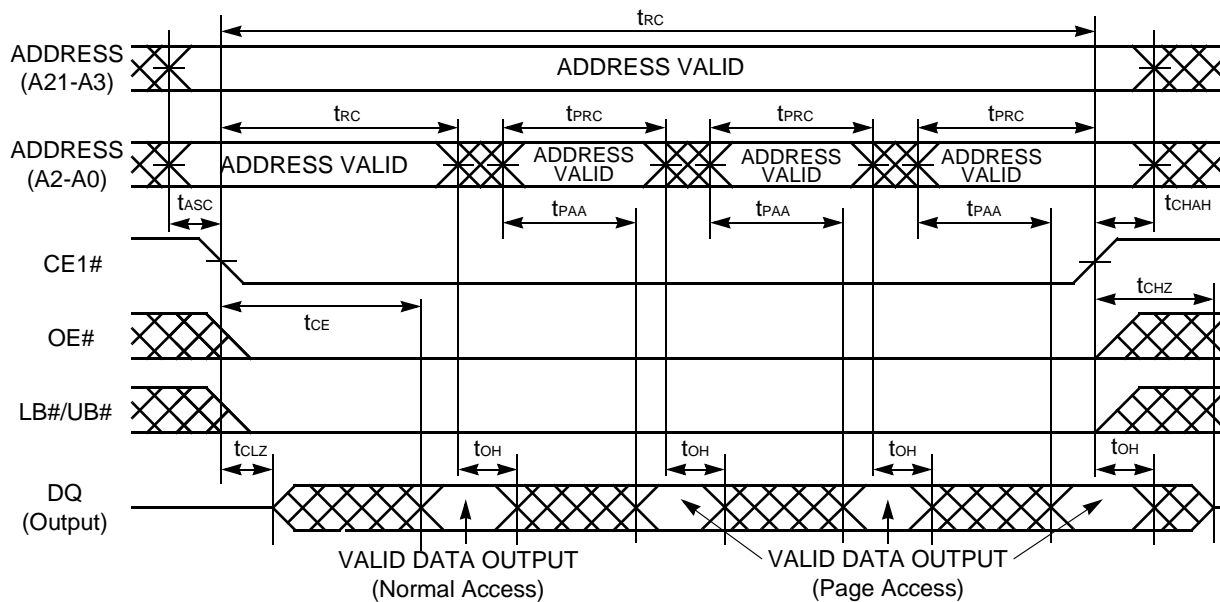
Note: This timing diagram assumes CE2=H and WE#=H.

Figure 58.   Read Timing #4 (Page Address Access after CEI# Control Access for 32M and 64M Only)
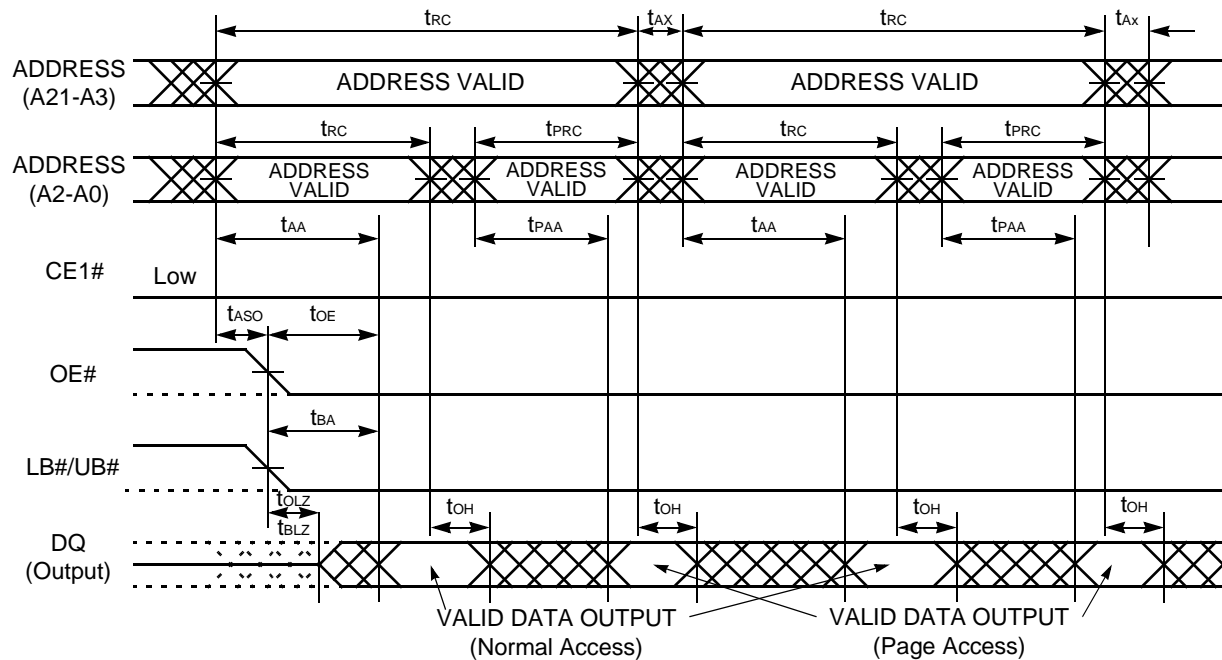
Notes:

1. This timing diagram assumes CE2=H and WE#=H.
2. Either or both LB# and UB# must be Low when both CE1# and OE# are Low.

Figure 59.   Read Timing #5 (Random and Page Address Access for 32M and 64M Only)

Write Timings
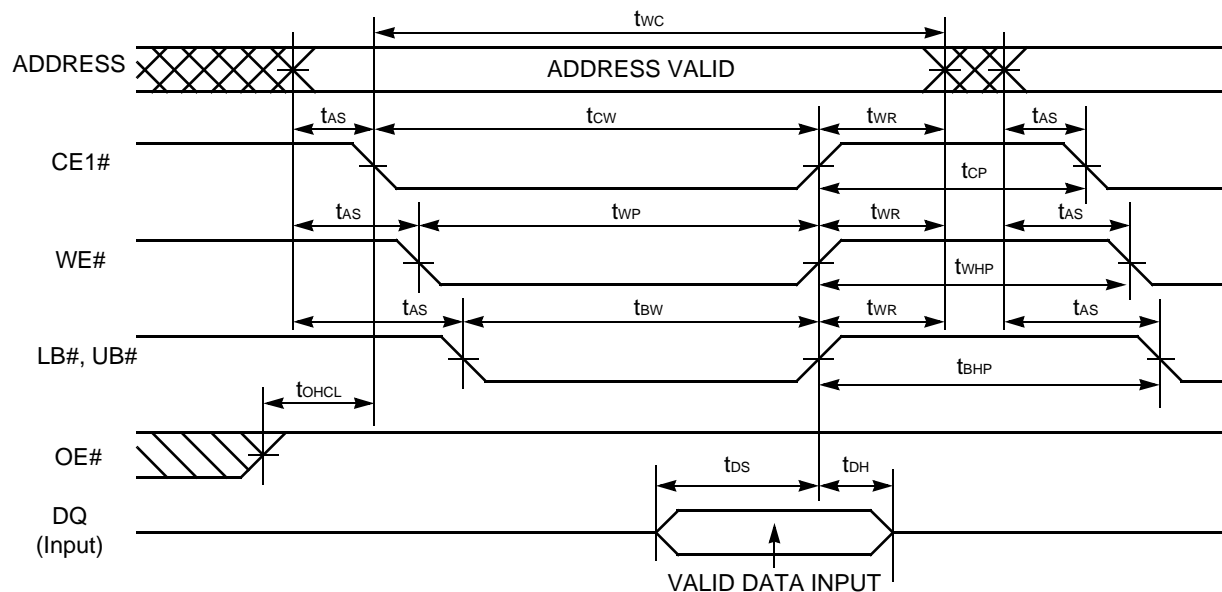
Note: This timing diagram assumes CE2=H.

Figure 60.   Write Timing #I (Basic Timing)
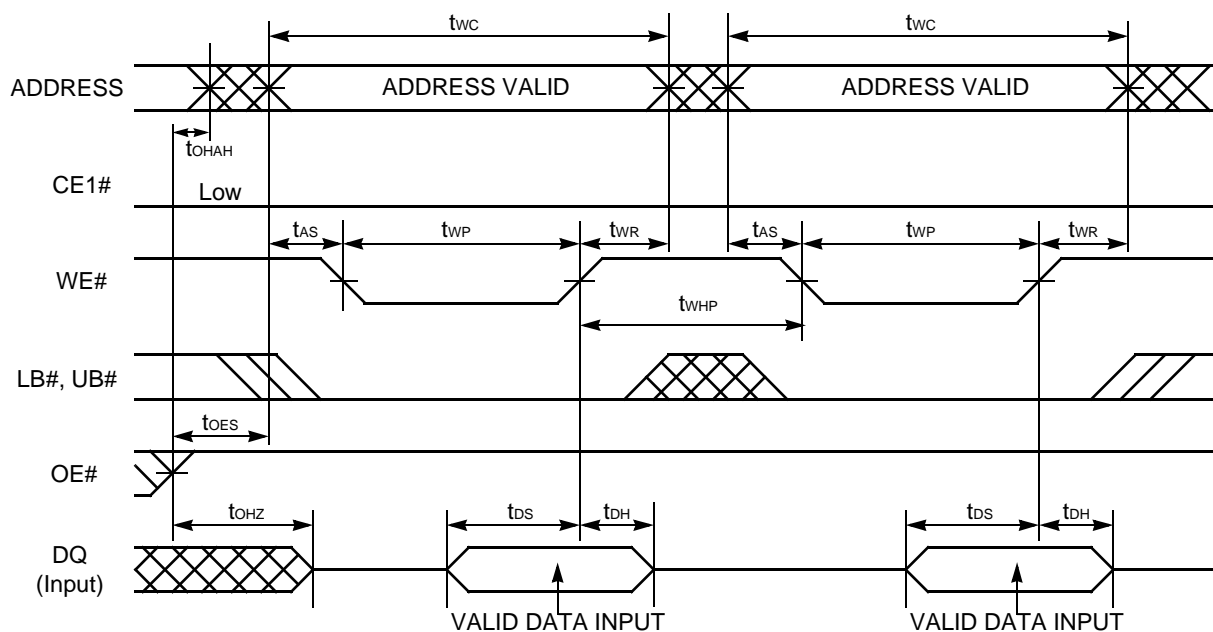
Note: *This timing diagram assumes CE2=H.*

Figure 6I.   Write Timing #2 (WE# Control)
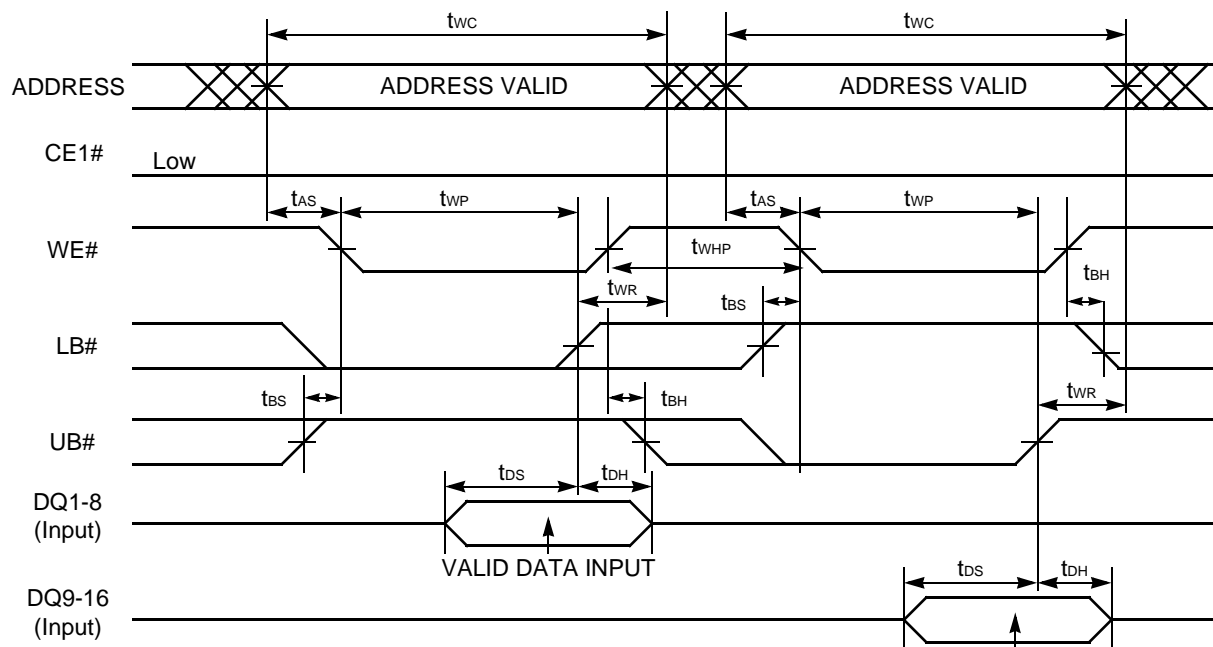
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 62.   Write Timing #3-I (WE#/LB#/UB# Byte Write Control)
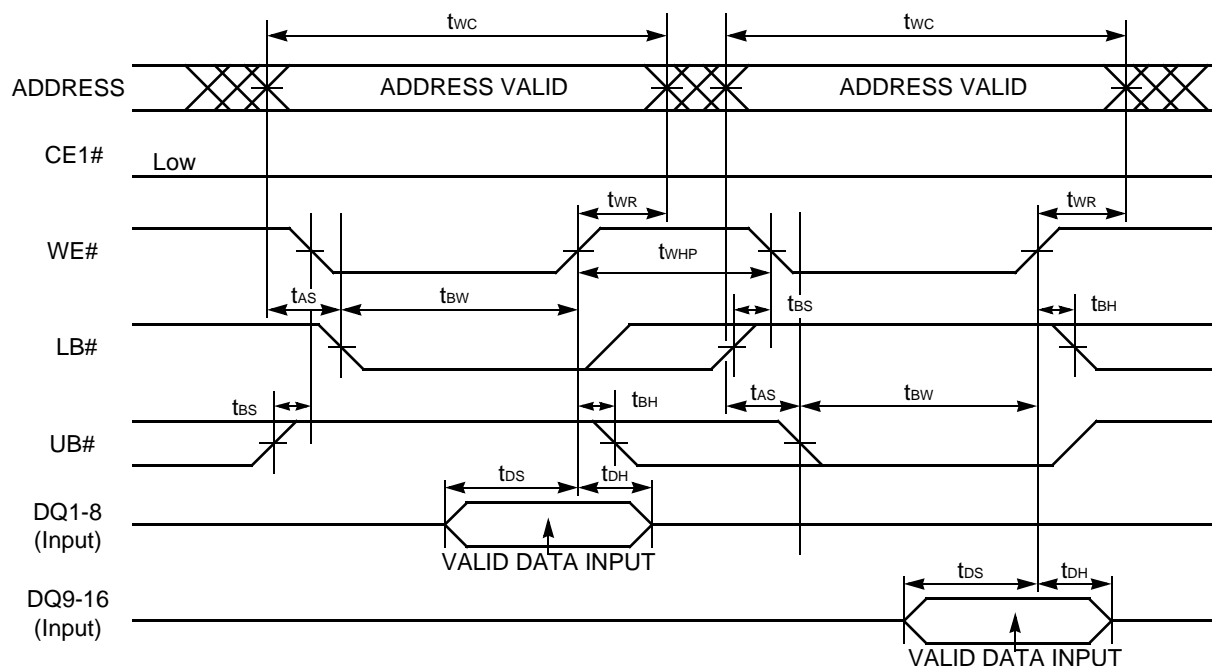
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 63.   Write Timing #3-3 (WE#/LB#/UB# Byte Write Control)
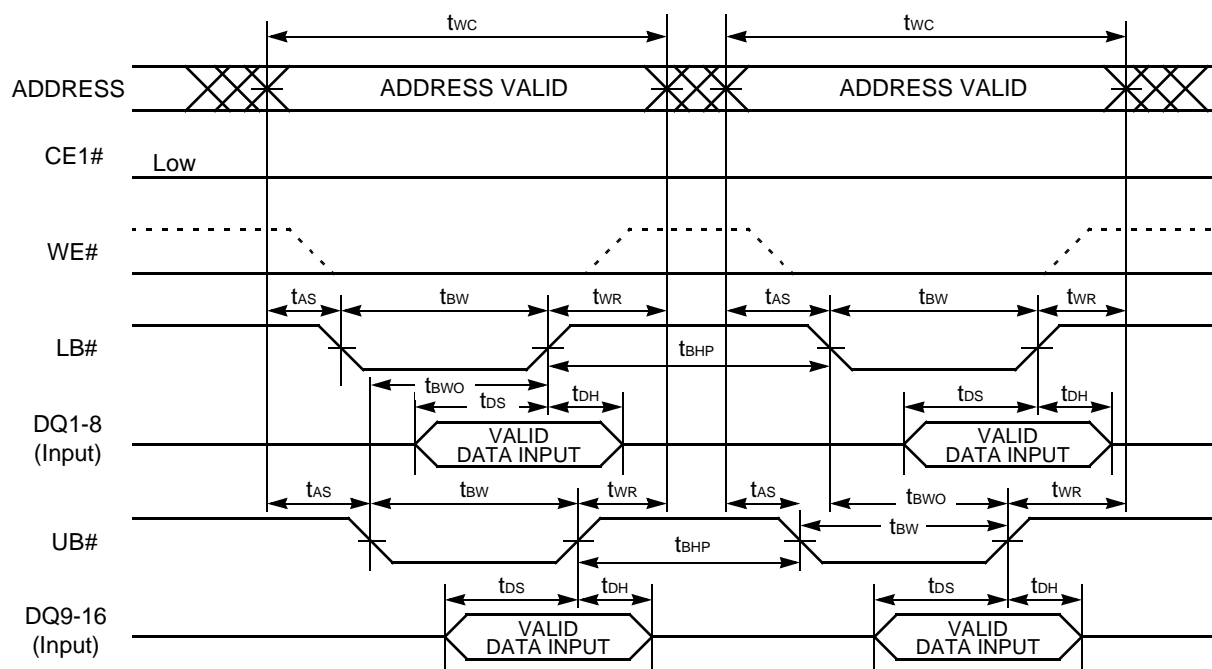
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 64.   Write Timing #3-4 (WE#/LB#/UB# Byte Write Control)

Read/Write Timings
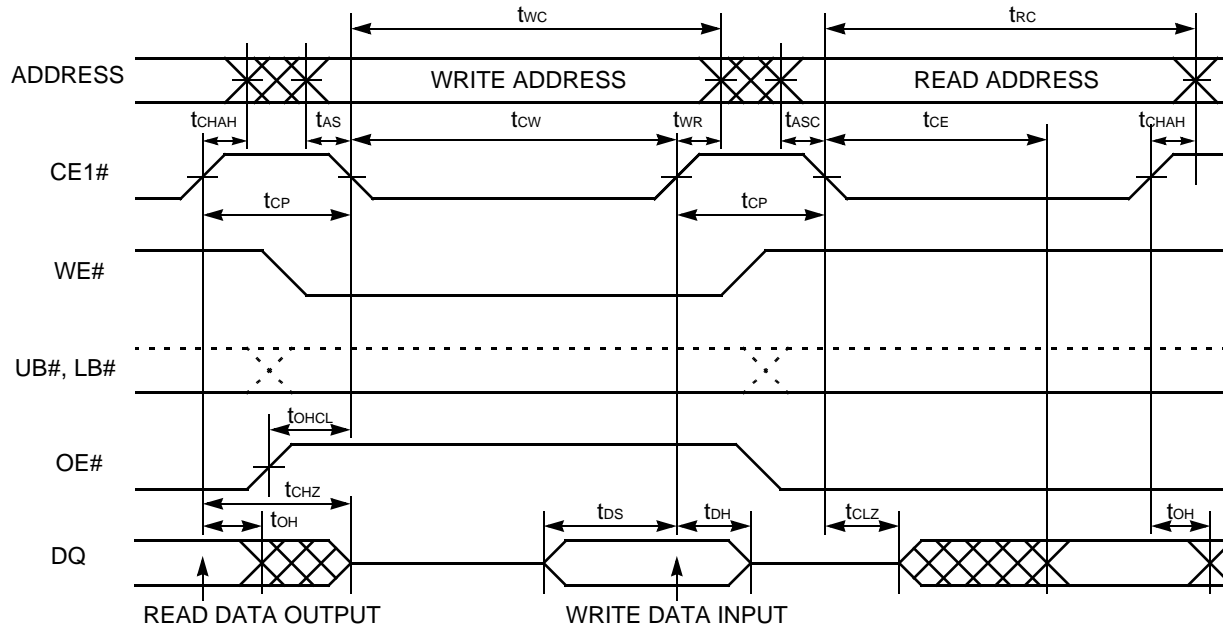
Notes:
1. This timing diagram assumes CE2=H.
2. Write address is valid from either CE1# or WE# of last falling edge.

Figure 65.   Read/Write Timing #1-1 (CEI# Control)
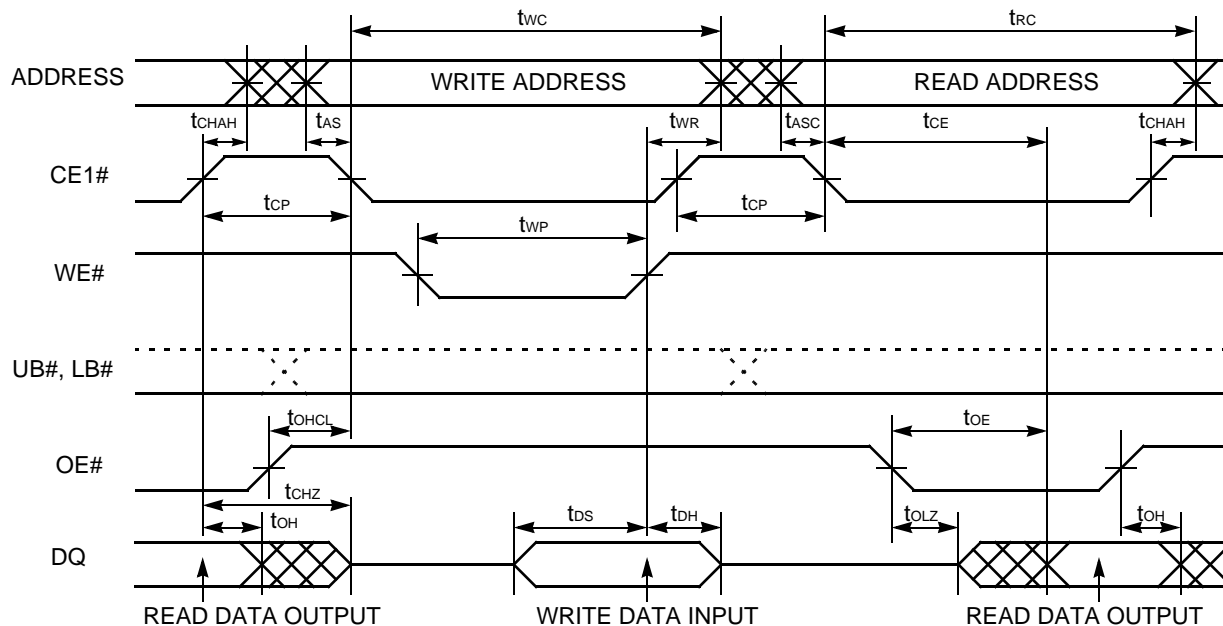
Notes:
1. This timing diagram assumes CE2=H.
2. OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read sequence.

Figure 66.   Read / Write Timing #1-2 (CEI#/WE#/OE# Control)
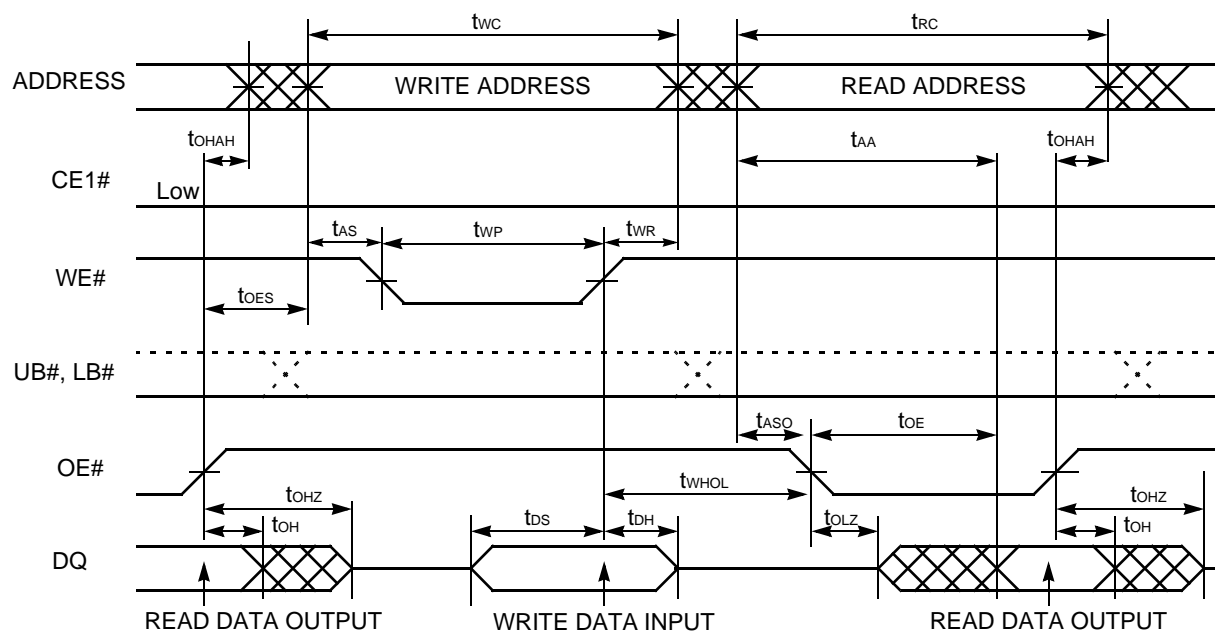
Notes:
1. This timing diagram assumes CE2=H.
2. CE1# can be tied to Low for WE# and OE# controlled operation.

Figure 67.   Read / Write Timing #2 (OE#, WE# Control)
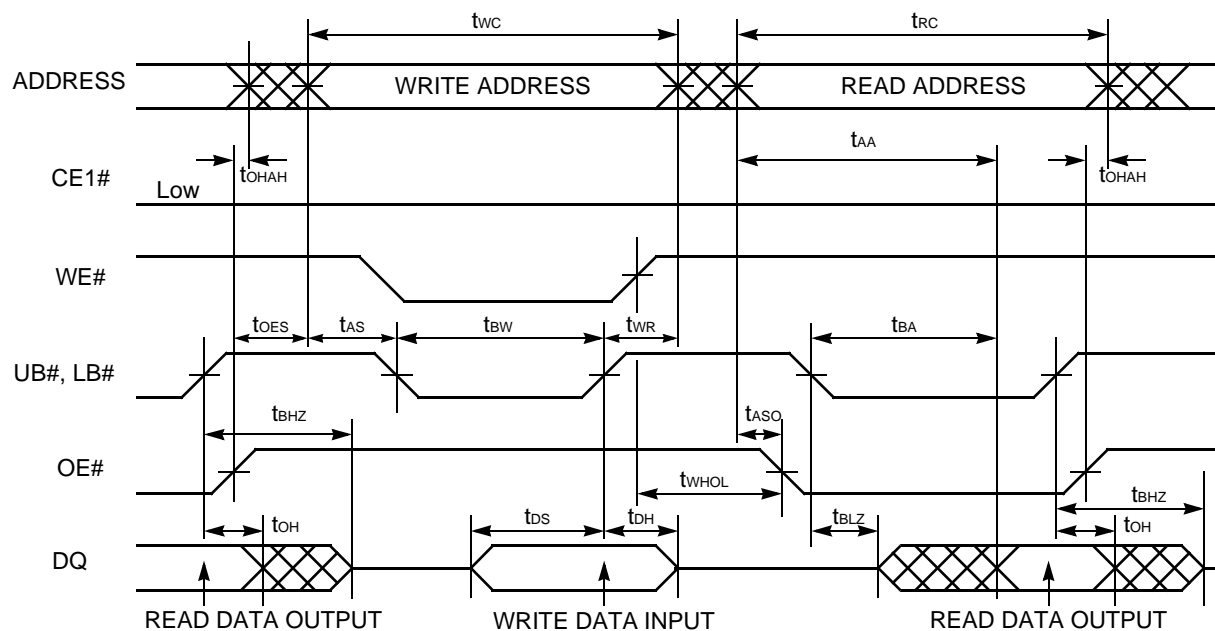
Notes:
1. This timing diagram assumes CE2=H.
2. CE1# can be tied to Low for WE# and OE# controlled operation.

Figure 68.   Read / Write Timing #3 (OE#, WE#, LB#, UB# Control)
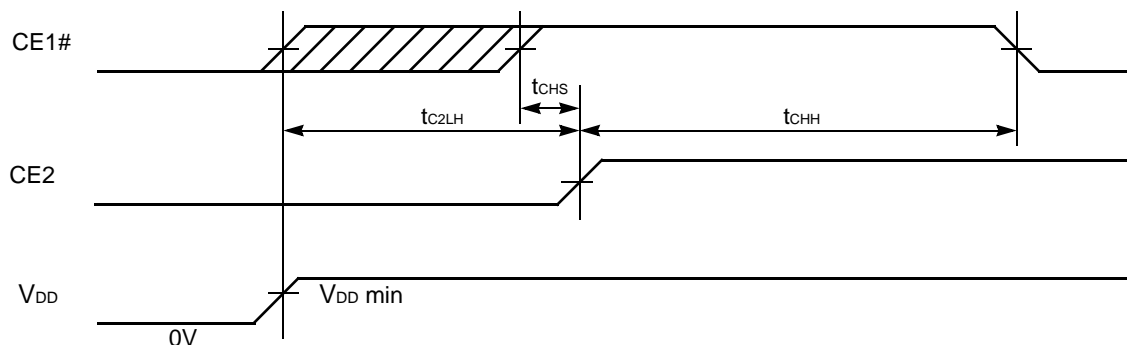
Note: The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

Figure 69.   Power-up Timing #1
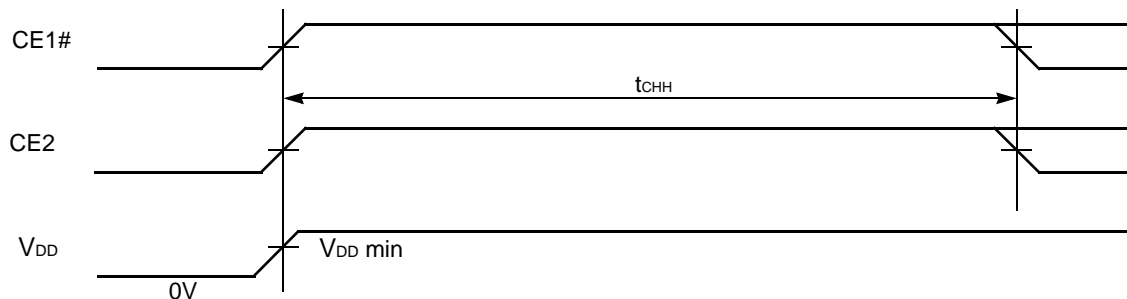
Note: The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both CE1# and CE2.

Figure 70.   Power-up Timing #2
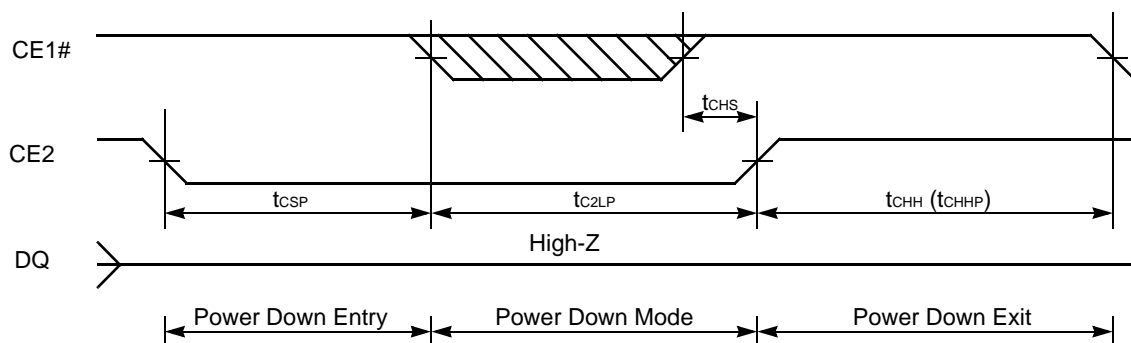
Note: This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.

Figure 71.   Power Down Entry and Exit Timing
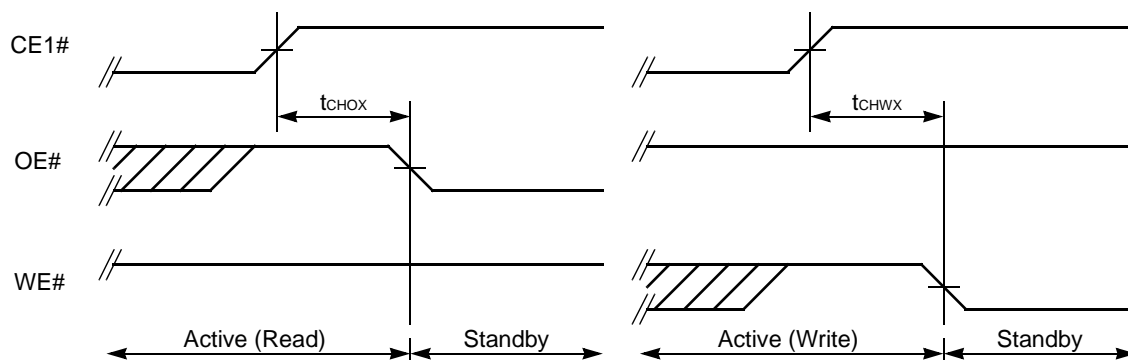
Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from CE1# Low to High transition.

Figure 72.   Standby Entry Timing after Read or Write
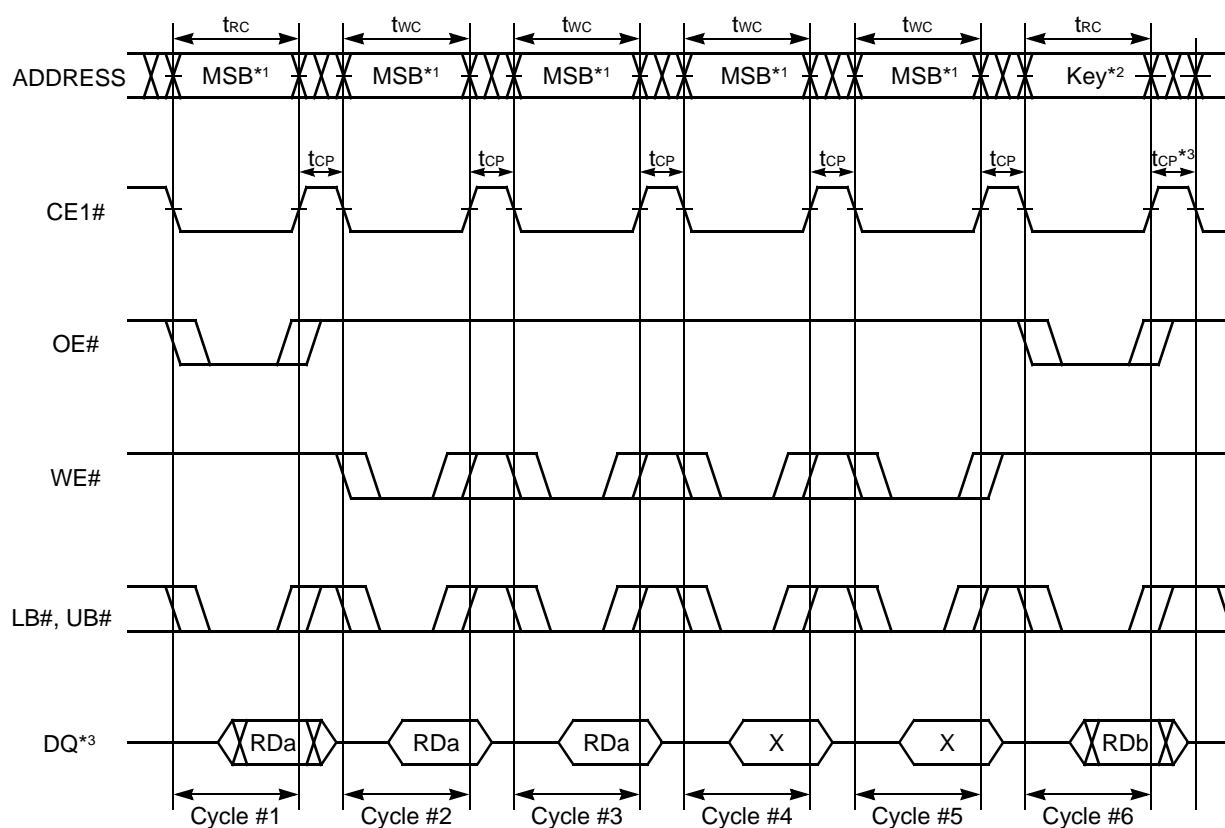
Notes:

1. The all address inputs must be High from Cycle #1 to #5.

2. The address key must confirm the format specified in page 132. If not, the operation and data are not guaranteed.

3. After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.

Figure 73.   Power Down Program Timing (for 32M/64M Only)

Revision Summary

Revision A0 (June 9, 2004)

Initial release.

Revision A1 (July 19, 2004)

Global Change

Change all instances of FASL to Spansion

Added Colophon text.

"Product Selector Guide" on page 2

Replaced "S71PL129JA0-9Z" with "S71PL129JA0-9P".

"Ordering Information" on page 9

In Model Number section replaced pSRAM part number with "See valid combinations table".

Revision A2 (July 21, 2004)

"Connection Diagram" on page 7

Changed Row D of pinout for accuracy.

Added the following note: "May be shared depending on density: A21 is shared for the 64M pSRAM configuration; A20 is shred for the 32M pSRAM configuration; A19 is shared for the 16M pSRAM configuration.

Revision A3 (October 18, 2004)

Core Flash Module

Replaced core flash module from S29PL127J_064J_032J_MCP_00_A1_E to S29PL129J_MCP_00_A0

Revision A4 (November 30, 2004)

Product Selector Guide

Added a new model number.

Valid Combinations Table

Whole table updated with new OPNs.

Revision A5 (December 23, 2004)

Connection Diagram

Updated pin L5.

Valid Combinations Table

Added a note to the bottom of the table.