



MOS INTEGRATED CIRCUIT

**μPD4416008**

**16M-BIT CMOS FAST SRAM  
2M-WORD BY 8-BIT**

**Description**

The μPD4416008 is a high speed, low power, 16,777,216 bits (2,097,152 words by 8 bits) CMOS static RAM.

Operating supply voltage is 3.3 V ± 0.3 V.

The μPD4416008 is packaged in a 54-PIN PLASTIC TSOP (II) (10.16 mm (400))

**Features**

- 2,097,152 words by 8 bits
- Fast access time : 15, 17 ns (MAX.)
- Output Enable input for easy application

**Ordering Information**

	Part number	Package	Supply voltage V	Access time ns (MAX.)	Supply current mA (MAX.)	
					At operating	At standby
★	μPD4416008G5-A15-9JF	54-PIN PLASTIC TSOP (II) (10.16 mm (400))	3.3 ± 0.3	15	230	10
★	μPD4416008G5-A17-9JF			17	220	

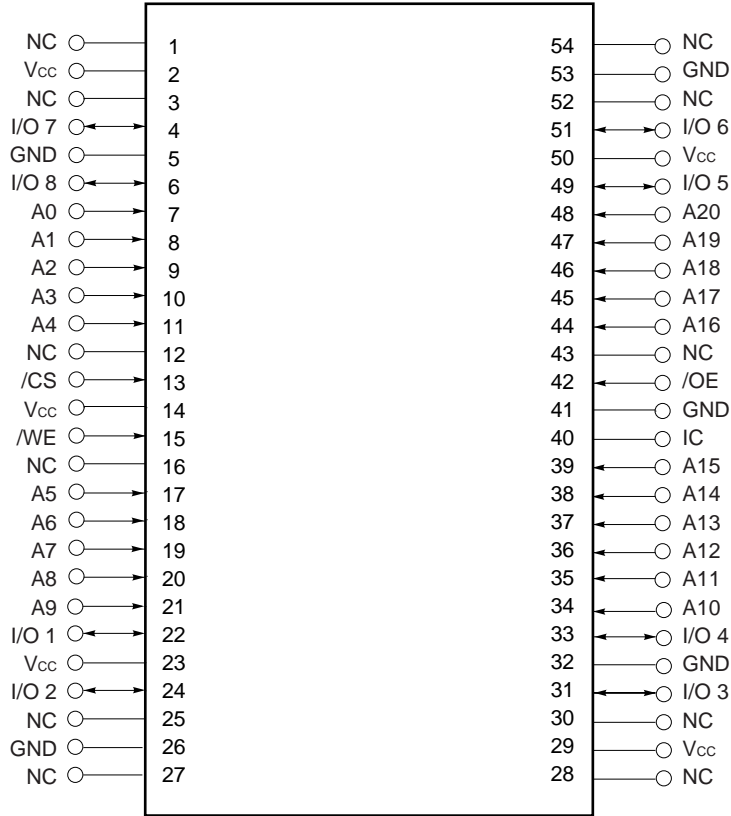
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**Pin Configuration (Marking Side)**

/xxx indicates active low signal.

**54-PIN PLASTIC TSOP (II) (10.16 mm (400))**

**[μPD4416008G5-xxx-9JF]**

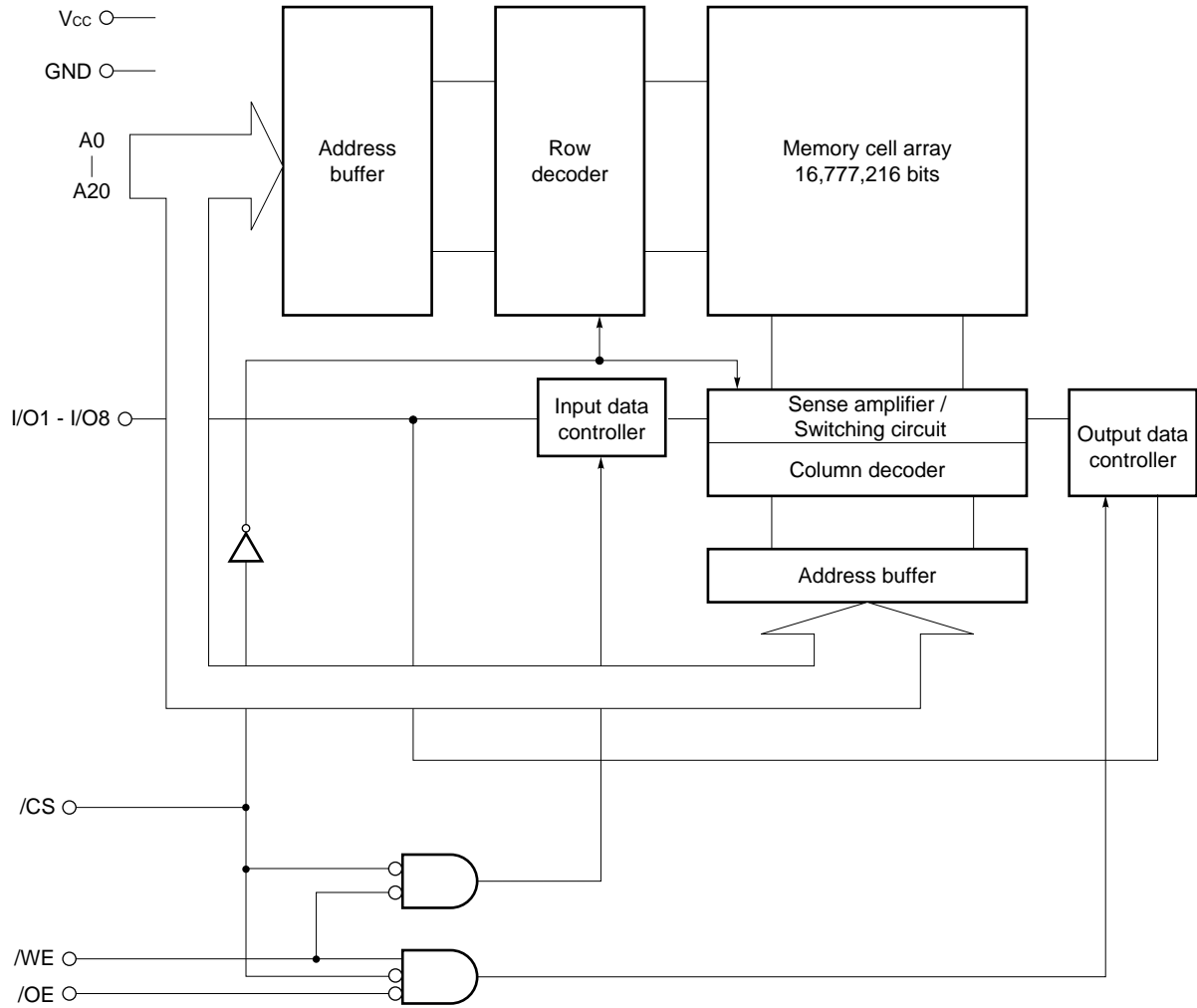


- A0 - A20 : Address Inputs
- I/O1 - I/O8 : Data Inputs / Outputs
- /CS : Chip Select
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection
- IC : Internal connection <sup>Note</sup>

**Note** Leave this pin connect to GND.

**Remark** Refer to **Package Drawing** for 1-pin index mark.

**Block Diagram**



**Truth Table**

/CS	/OE	/WE	Mode	I/O	Supply current
H	x	x	Not selected	High impedance	I <sub>SB</sub>
L	L	H	Read	D <sub>OUT</sub>	I <sub>CC</sub>
L	x	L	Write	D <sub>IN</sub>	
L	H	H	Output disable	High impedance	

**Remark** x : Don't care

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
★ Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +4.0	V
★ Input / Output voltage	V <sub>T</sub>		-0.5 <sup>Note</sup> to +4.0	V
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Note** -2.0 V (MIN.) (pulse width : 2 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Note** -2.0 V (MIN.) (pulse width : 2 ns)

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-2		+2	μA
Output leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-2		+2	μA
★ Operating supply current	I <sub>CC</sub>	/CS = V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA, Minimum cycle time				
		Cycle time : 15 ns			230	mA
		Cycle time : 17 ns			220	
★ Standby supply current	I <sub>SB</sub>	/CS = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Minimum cycle time			80	mA
	I <sub>SB1</sub>	/CS ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			10	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	2.4			V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +8.0 mA			0.4	V

**Remark** V<sub>IN</sub> : Input voltage, V<sub>I/O</sub> : Input / Output voltage

**Capacitance (TA = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			6	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			8	pF

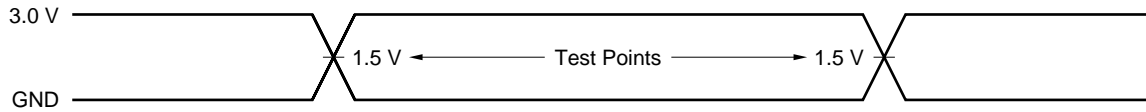
**Remarks** 1. V<sub>IN</sub> : Input voltage, V<sub>I/O</sub> : Input / Output voltage  
 2. These parameters are periodically sampled and not 100% tested.

**AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

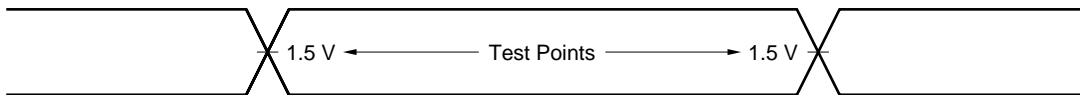
**AC Test Conditions**

**LVTTTL Interface**

**Input Waveform (Rise and Fall Time ≤ 3 ns)**

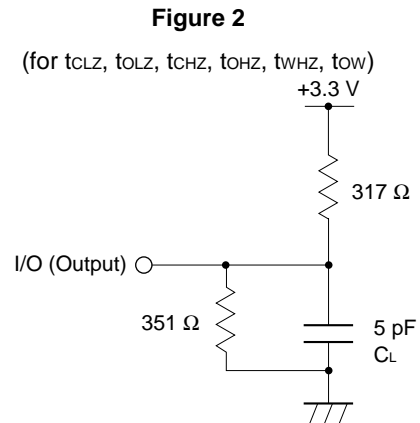
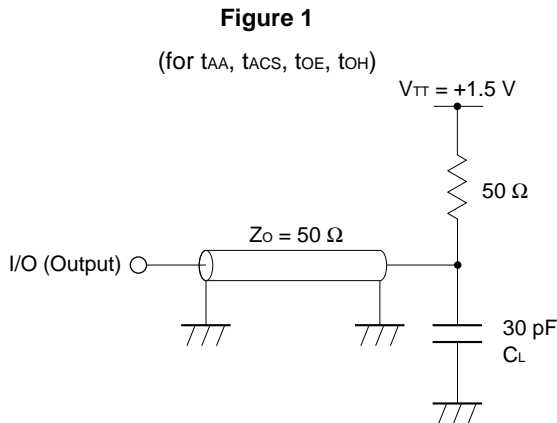


**Output Waveform**



**Output Load**

AC characteristics directed with the note should be measured with the output load shown in Figure 1 or Figure 2.



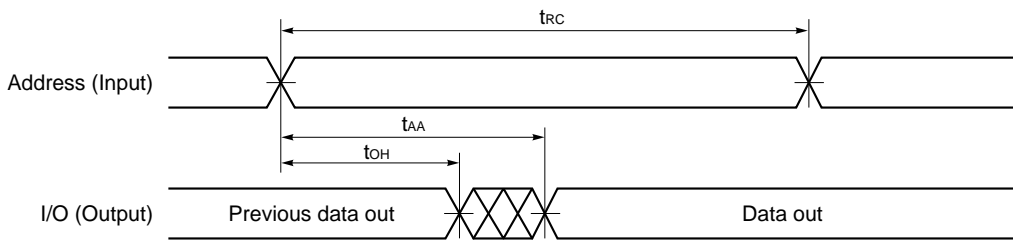
**Remark**  $C_L$  includes capacitances of the probe and jig, and stray capacitances.

**Read Cycle**

Parameter	Symbol	-A15		-A17		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	$t_{RC}$	15		17		ns	
Address access time	$t_{AA}$		15		17	ns	1
/CS access time	$t_{ACS}$		15		17	ns	
/OE access time	$t_{OE}$		7		8	ns	
Output hold from address change	$t_{OH}$	3		3		ns	
/CS to output in low impedance	$t_{CLZ}$	3		3		ns	2, 3
/OE to output in low impedance	$t_{OLZ}$	0		0		ns	
/CS to output in high impedance	$t_{CHZ}$		7		8	ns	
/OE to output hold in high impedance	$t_{OHZ}$		7		8	ns	

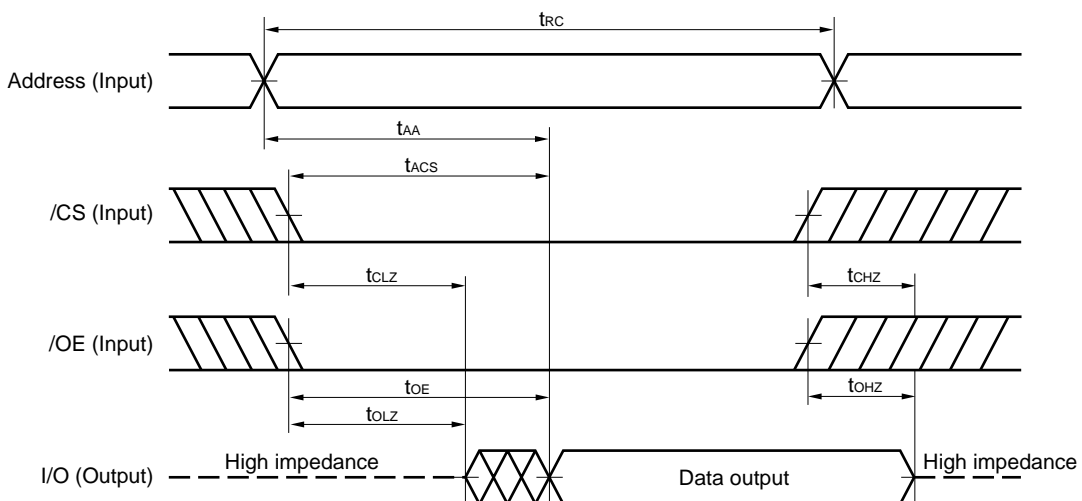
- Notes**
1. See the output load shown in **Figure 1**.
  2. Transition is measured at  $\pm 200$  mV from steady-state voltage with the output load shown in **Figure 2**.
  3. These parameters are periodically sampled and not 100% tested.

**Read Cycle Timing Chart 1 (Address Access)**



- Remarks**
1. In read cycle, /WE should be fixed to high level.
  2. /CS = /OE =  $V_{IL}$

**Read Cycle Timing Chart 2 (/CS Access)**



**Caution** Address valid prior to or coincident with /CS low level input.

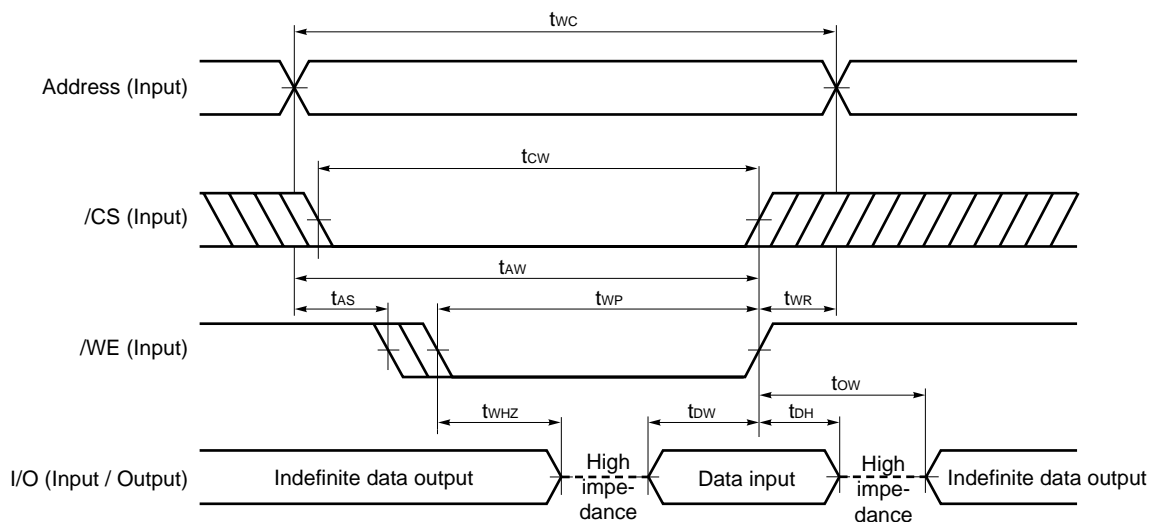
**Remark** In read cycle, /WE should be fixed to high level.

**Write Cycle**

Parameter	Symbol	-A15		-A17		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{wc}$	15		17		ns	
/CS to end of write	$t_{cw}$	10		11		ns	
Address valid to end of write	$t_{aw}$	10		11		ns	
Write pulse width	$t_{wp}$	10		11		ns	
Data valid to end of write	$t_{dw}$	7		8		ns	
Data hold time	$t_{dh}$	0		0		ns	
Address setup time	$t_{as}$	0		0		ns	
Write recovery time	$t_{wr}$	1		1		ns	
/WE to output in high impedance	$t_{whz}$		7		8	ns	1, 2
Output active from end of write	$t_{ow}$	3		3		ns	

- Notes**
1. Transition is measured at  $\pm 200$  mV from steady-state voltage with the output load shown in **Figure 2**.
  2. These parameters are periodically sampled and not 100% tested.

**Write Cycle Timing Chart 1 (/WE Controlled)**



**Cautions** 1. /CS or /WE should be fixed to high level during address transition.

★

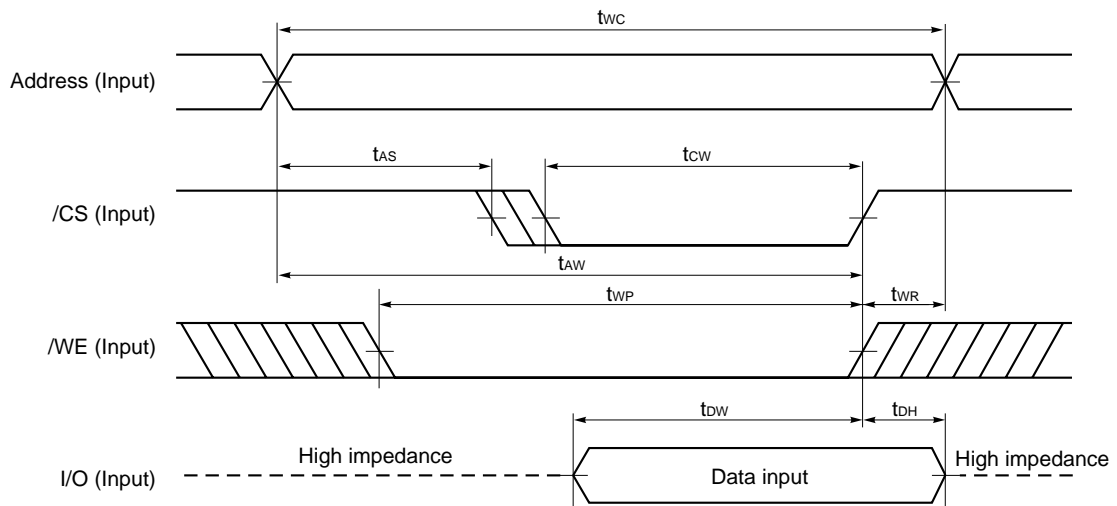
2. Do not input data to the I/O pins while they are in the output state.

**Remarks** 1. Write operation is done during the overlap time of a low level /CS, a low level /WE.

2. During  $t_{whz}$ , I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

**Write Cycle Timing Chart 2 (/CS Controlled)**



**Cautions 1. /CS or /WE should be fixed to high level during address transition.**

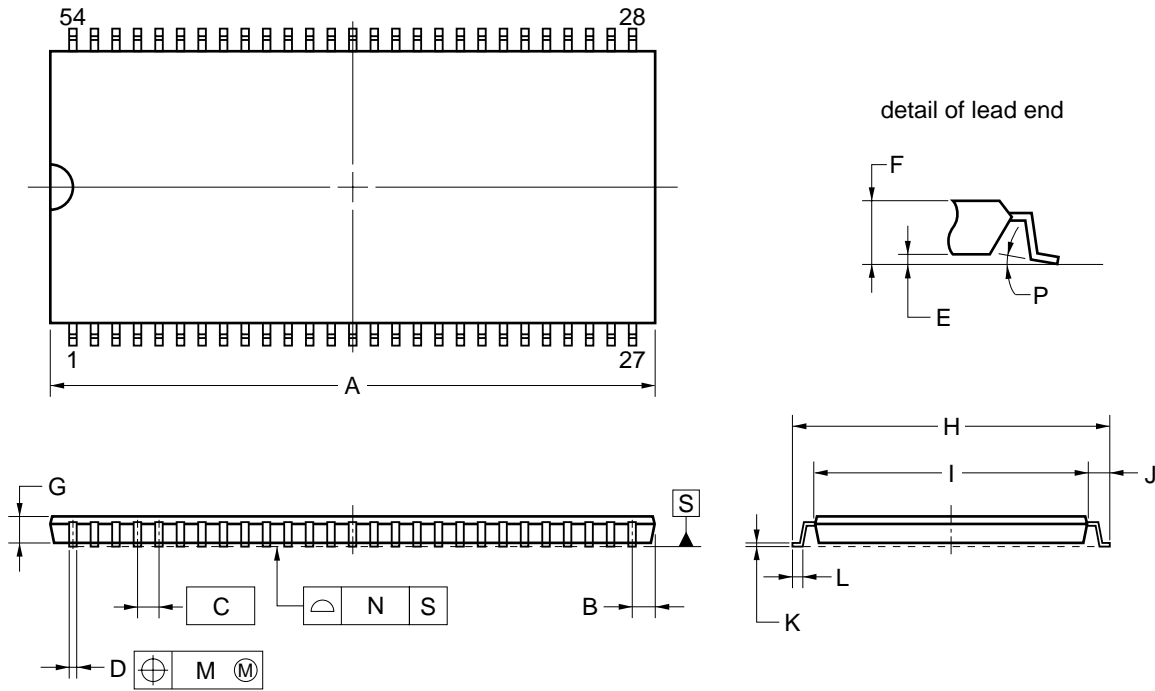
★ **2. Do not input data to the I/O pins while they are in the output state.**

**Remark** Write operation is done during the overlap time of a low level /CS and a low level /WE.



Package Drawing

54-PIN PLASTIC TSOP (II) (10.16 mm (400))



NOTES

1. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.
2. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

ITEM	MILLIMETERS
A	22.22±0.05
B	0.91 MAX.
C	0.80 (T.P.)
D	0.32 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.10±0.05
F	1.1±0.1
G	1.00
H	11.76±0.20
I	10.16±0.10
J	0.80±0.20
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>
L	0.50±0.10
M	0.13
N	0.10
P	3 <sup>+7</sup> <sub>-3</sub> °

S54G5-80-9JF-2

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4416008.

**Type of Surface Mount Device**

$\mu$ PD4416008 : 54-PIN PLASTIC TSOP (II) (10.16 mm (400))

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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