NEC

MOS INTEGRATED CIRCUIT

μPD168001

MONOLITHIC 4-CHANNEL H BRIDGE + LOW-SIDE SWITCH

DESCRIPTION

The μPD168001 is a monolithic 4-channel H bridge driver and low-side switch IC that uses a power MOSFET at the output stage. Because of the MOSFET at the output stage, both the inputs and outputs are interfaced by PWM digital signals, and the power consumption can therefore be lowered. A 30-pin thin shrink SOP is employed as the package to help to create a small and thin set.

FEATURES

O Four H bridge circuits using power MOSFET and low-side switch

O Low on-resistance

4-ch H bridge: 2 Ω MAX. (sum of upper and lower stages)

Low-side switch: 2 Ω MAX.

O High-speed PWM drive: Operating frequency up to 120 kHz

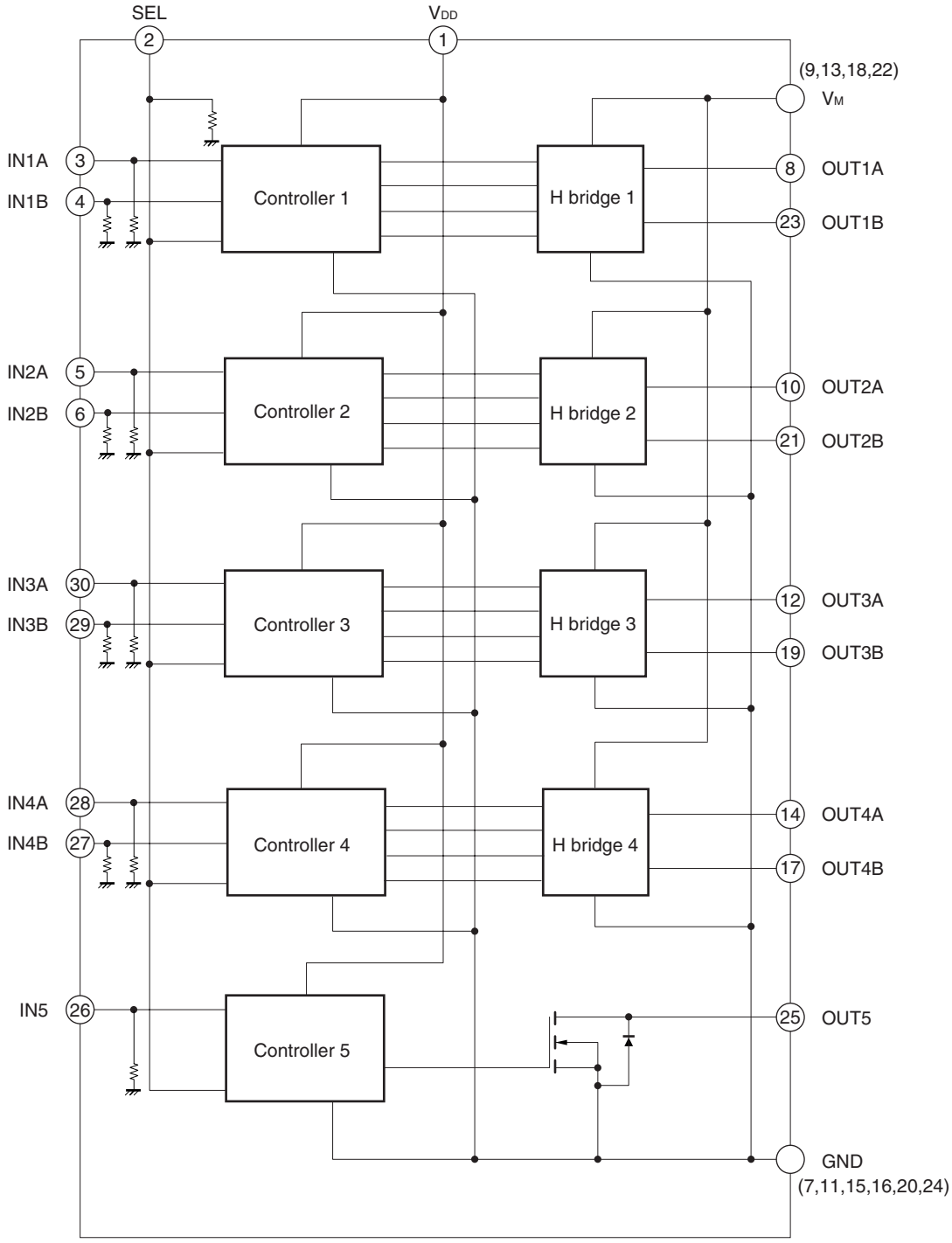
O Thin 30-pin shrink SOP (7.62 mm (300) with 0.65 mm pitch)

ORDERING INFORMATION

Part Number	Package
μPD168001MC-6A4-A	30-pin plastic TSSOP (7.62 mm (300))

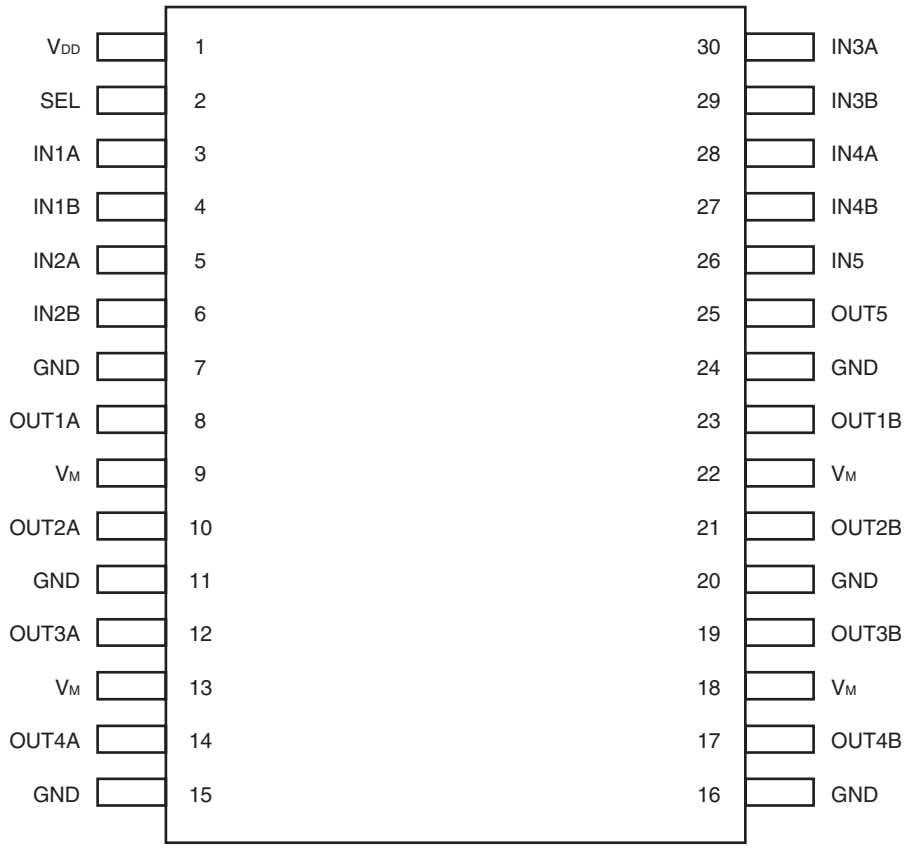
Document No. S15728EJ1V0DS00 (1st edition)
Date Published March 2003 N CP(K)
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION

Package: 30-pin TSSOP (7.62 mm with 0.65 mm pitch)



PIN FUNCTION

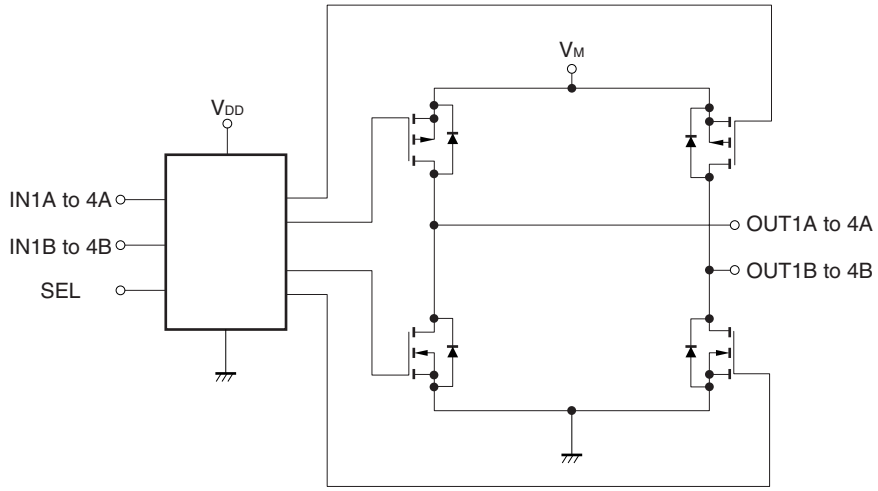
Pin No.	Pin Name	Pin Function
1	V_{DD}	Logic power supply
2	SEL	Control pin
3	IN1A	Channel 1 input pin A
4	IN1B	Channel 1 input pin B
5	IN2A	Channel 2 input pin A
6	IN2B	Channel 2 input pin B
7	GND	GND pin
8	OUT1A	Channel 1 output pin A
9	V_M	Motor power supply pin
10	OUT2A	Channel 2 output pin A
11	GND	GND pin
12	OUT3A	Channel 3 output pin A
13	V_M	Motor power supply pin
14	OUT4A	Channel 4 output pin A
15	GND	GND pin
16	GND	GND pin
17	OUT4B	Channel 4 output pin B
18	V_M	Motor power supply pin
19	OUT3B	Channel 3 output pin B
20	GND	GND pin
21	OUT2B	Channel 2 output pin B
22	V_M	Motor power supply pin
23	OUT1B	Channel 1 output pin B
24	GND	GND pin
25	OUT5	Channel 5 output pin
26	IN5	Channel 5 input pin
27	IN4B	Channel 4 input pin B
28	IN4A	Channel 4 input pin A
29	IN3B	Channel 3 input pin B
30	IN3A	Channel 3 input pin A

FUNCTION SPECIFICATIONS

(1) Revolution control

A high-level/low-level binary signal is input to the H bridge driver block incorporating 4 outputs.

The truth table of the input logic is shown below.

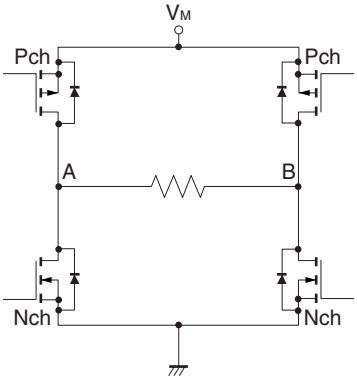


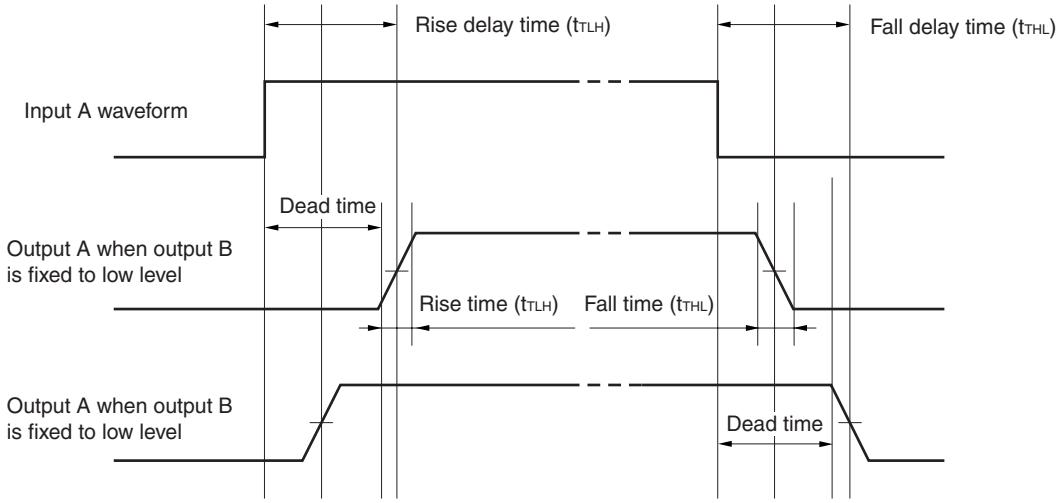
Function Table (Common to All Channels)				
Input			Output	
IN1A to IN4A	IN1B to IN4B	SEL	1A to 4A	1B to 4B
L	L	H	L	L
H	L	H	H	L
L	H	H	L	H
H	H	H	H	H
–	–	L	Hi-Z	Hi-Z

(2) Switching of H bridges

When output A is switched in the figure shown on the right, a dead time (time for which both Pch and Nch are OFF) elapses to prevent through current. Consequently, the waveform of output A (rise time, fall time, and delay time) changes depending on whether output B is fixed to the high or low level.

The figure below shows the voltage waveform of output B in response to an input waveform when output B is fixed to the low level and the high level.





- When output B is fixed to low level

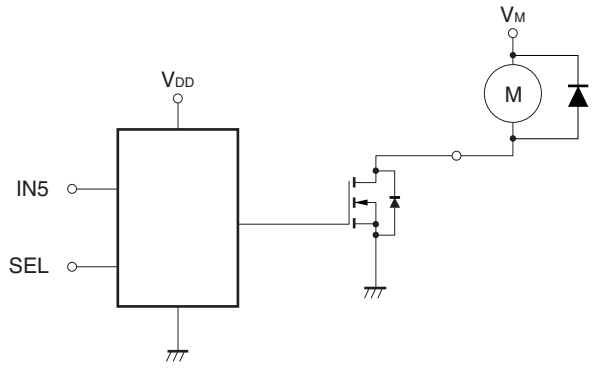
  Output A goes into a high-impedance state and is undefined during the dead time period, but a low level is output to output A because output B is pulled down by the load

- When output B is fixed to high level

  Output A goes into a high-impedance state and is undefined during the dead time period, but a high level is output to output A because output B is pulled up by the load.

(3) Low-side switch

The low-side switch of ch 5 has an output stage configured of an N-ch MOSFET. Its input is a high-level/low-level binary signal. The truth table of the input logic is shown below.



Function Table (Channel 5)		
Input		Output
IN5	SEL	OUT5
L	H	Hi-Z (output off)
H	H	L (ouput on)
–	L	Hi-Z (output off)

(4) Power sequence

This IC has logic power supply (V_{DD}) and output power supply (V_M) pins. The power sequence of these pins must be as follows.

Turn on V_M with V_{DD} turned on to turn on power.

To turn off power, turn off V_M with V_{DD} turned on, and then turn off V_{DD}.

(However, V_{DD} and V_M can be turned off at the same time.)

Cautions 1. Because this IC switches a high current at high speeds, surge may be generated by V_M, GND wiring, and inductance, degrading the IC.

On the PWB, widen and shorten the pattern width of the GND lines as much as possible, and locate bypass capacitors between V_M and GND as close to the IC as possible. Connect two capacitors in parallel: a magnetic capacitor with a low inductance (4700 pF or more) and an electrolytic capacitor of 10 μF or more, depending on the load current.

2. When a load such as a DC motor is connected to ch 5 and the switch is turned OFF, a counter electromotive force is generated. If the absolute maximum rating of the output pin voltage may be exceeded by the voltage applied to the load, be sure to connect a Schottky barrier diode to both the ends of the load to prevent the rating of the output pin voltage from being exceeded.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Control block	−0.5 to +6.0	V
	V_M	Motor block	−0.5 to +6.0	V
Input voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Output pin voltage	V_{OUT}		6.0	V
DC output current	I_{DD}	DC	±0.3	A/ch
Instantaneous output current[Note 1]	I_{DP}	When two or more channels are turned ON at the same time PW ≤ 50 ms, Duty ≤ 5%	±1.0	A/ch
Power consumption[Note 2]	P_T		1.0	W
Peak junction temperature	$T_{CH(MAX)}$		150	°C
Storage temperature	T_{stg}		−55 to 150	°C

Notes 1. DUTY indicates the period during which a current flows, exceeding I_{DD} for the entire sequence

2. When mounted on a glass epoxy board (100 mm × 100 mm × 1 mm, with a copper foil area of 15%)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	Control block	3.0	3.3	3.6	V
	V_{MACT}	Motor block	4.5	5.0	5.5	V
Input voltage	V_{IN}		0		V_{DD}	V
DC output current	I_{DD}	DC			±0.2	A/ch
Instantaneous output current	I_{DP}	When two or more channels are turned ON at the same time PW ≤ 50 ms, Duty ≤ 5%			±0.85	A/ch
Operating frequency	f_{IN}				120	kHz
Operating temperature range	T_A		0		75	°C

ELECTRICAL CHARACTERISTICS

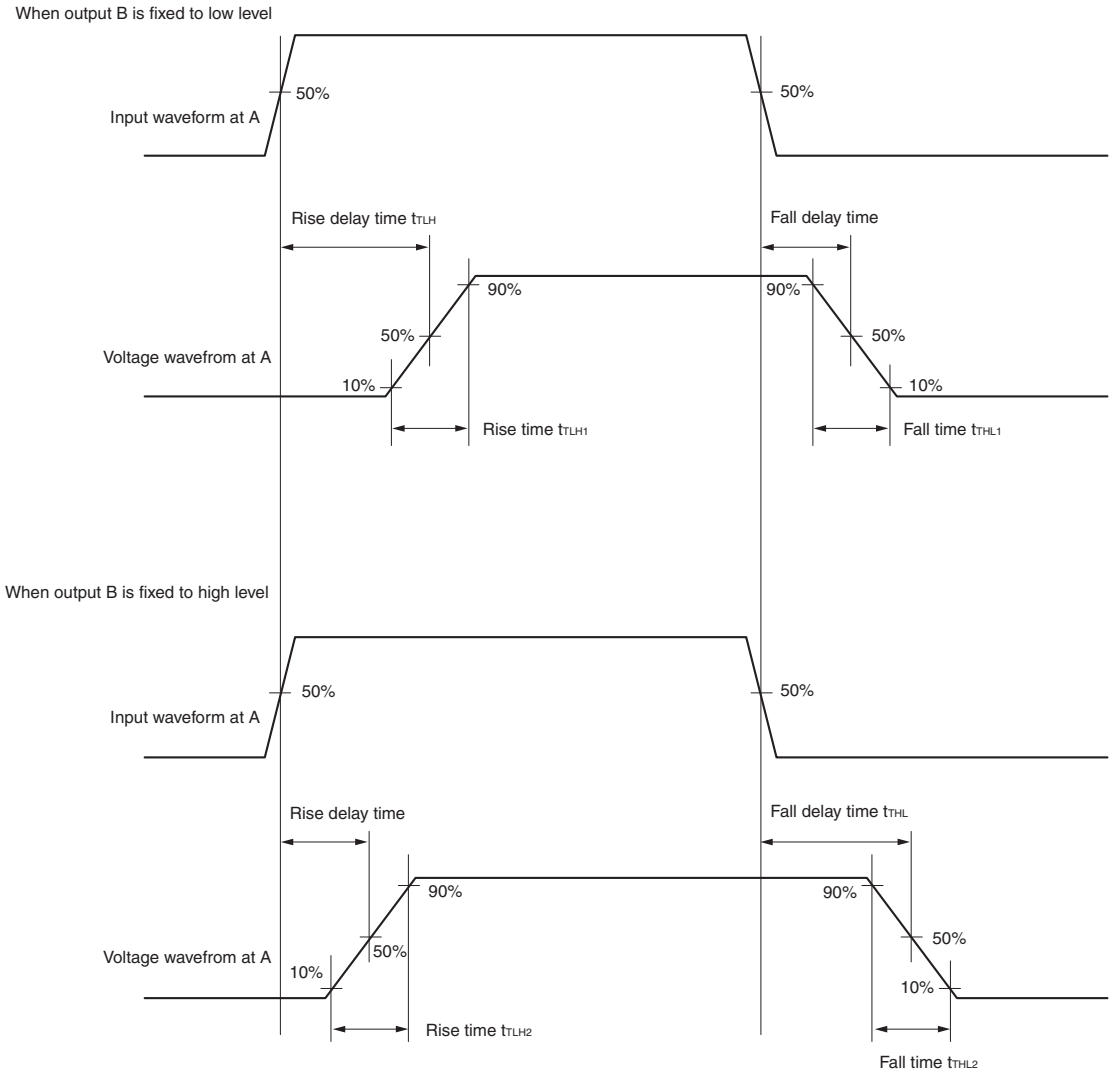
(UNLESS OTHERWISE SPECIFIED, V_{DD} = 3.3 V, V_M = 5 V, T_A = 25°C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
1. DC characteristics								
V_M pin current			I_M	SEL = L			10	μA
V_{DD} pin current			$I_{DZ(OFF)}$	SEL = L			10	μA
Input pull-down resistance			R_{IN}	IN and SEL pins	50		200	kΩ
High-level input voltage			V_{IH}	IN and SEL pins	0.7 × V_{DD}		V_{DD}	V
Low-level input voltage			V_{IL}	IN and SEL pins	–0.3		0.3 × V_{DD}	V
High-level input current			I_{IH}	V_{IN} = V_{DD}			80	μA
Low-level input current			I_{IL}	V_{IN} = 0 V	–2.0			μA
On-resistance (ch1 to 4, sum of upper and lower stages)			R_{ON}	I_D = 0.2 A			2.0	Ω
On-resistance (ch 5)			R_{ON}	I_D = 0.2 A			2.0	Ω
Switching current with no load on H bridge[Note]			$I_{S(AVE)}$	Input frequency: 100 kHz			4.5	mA
2. AC characteristics								
1 to 4ch	With output of one side fixed to low	Rise delay time	t_{TLH}	Load: 20 Ω Input frequency: 1 kHz	150	400	800	ns
		Rise time	t_{TLH1}		35	250	500	
		Fall time	t_{THL1}		35	75	150	
	With output of one side fixed to high	Fall delay time	t_{THL}		150	500	800	
		Rise time	t_{THL2}		35	75	150	
		Fall time	t_{THL2}		35	300	600	
5ch	Rise time		t_{TLH3}			100	200	
	Fall time		t_{THL3}			50	100	

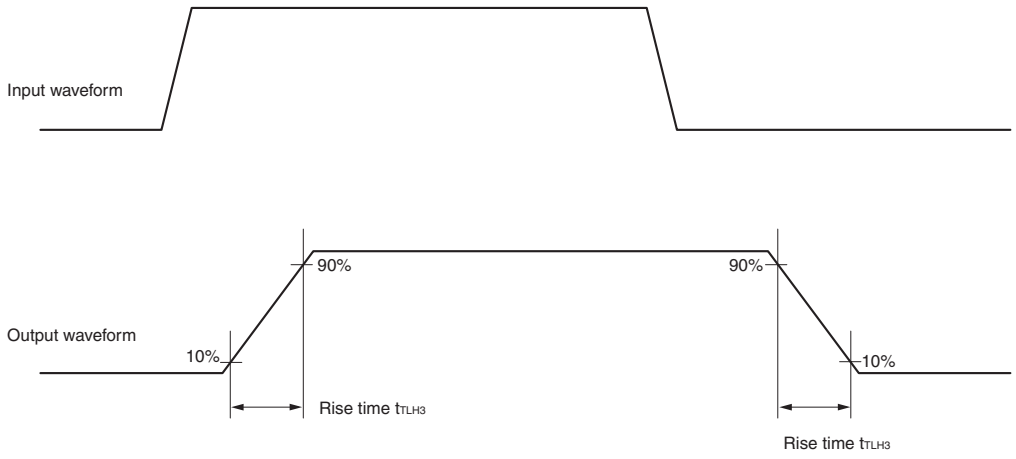
Note Average value of current consumed inside the H bridge when the switching operation is performed without a load.

TIMING CHARTS

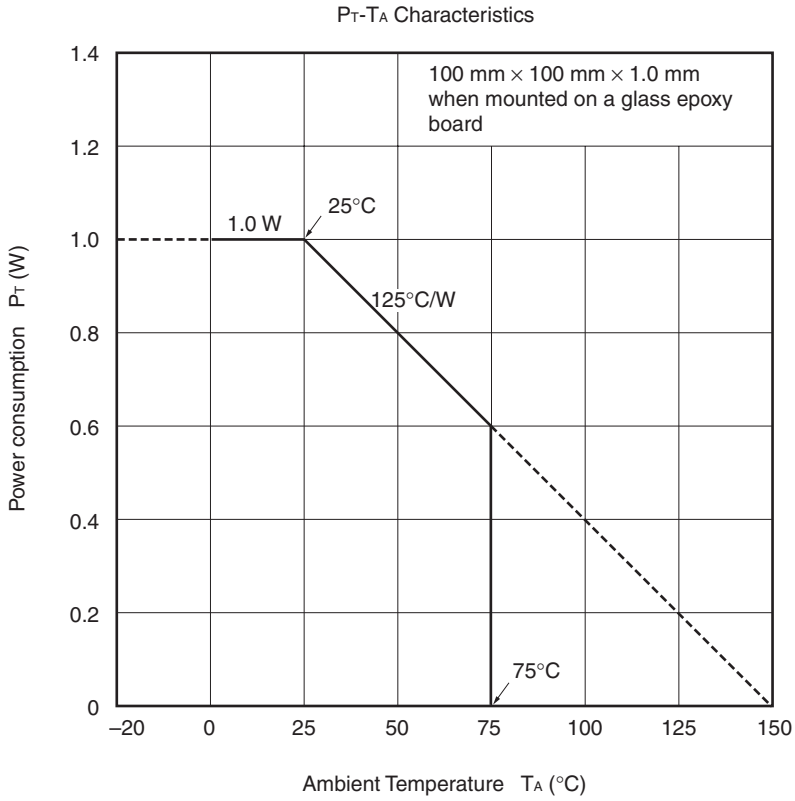
• Channel 1 to Channel 4



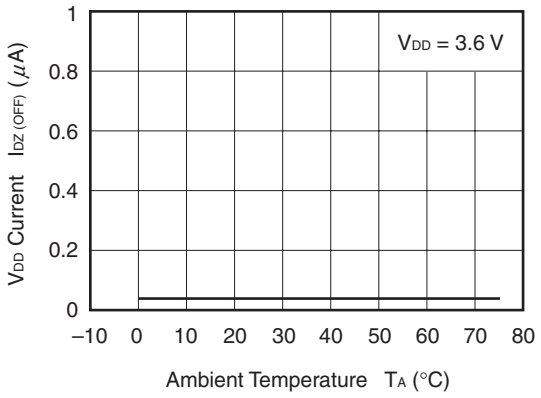
• Channel 5



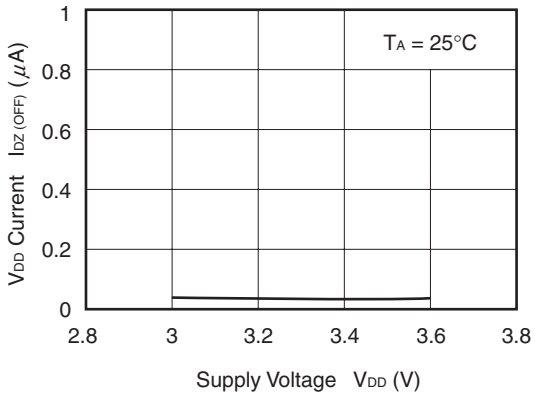
POWER CONSUMPTION CHARACTERISTICS



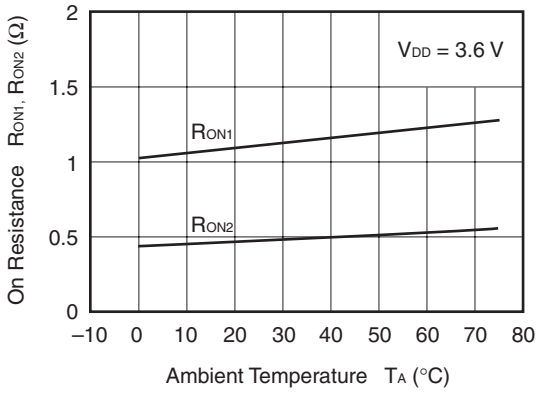
$I_{DZ(OFF)}$ -T_A Characteristics



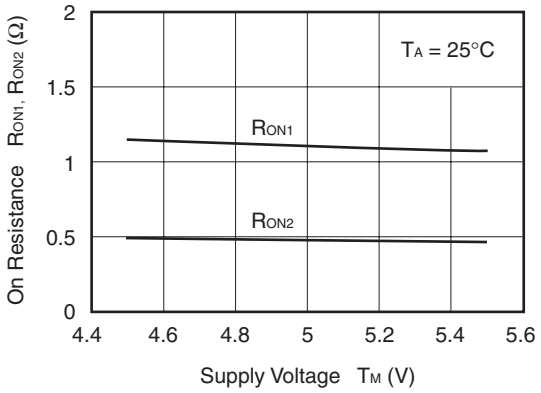
$I_{DZ(OFF)}$ -V_{DD} Characteristics



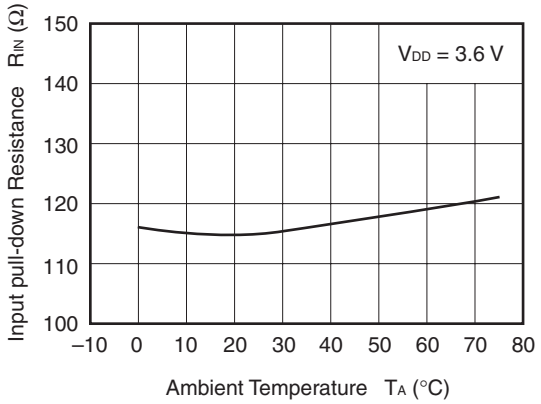
R_{ON1}, R_{ON2} Characteristics



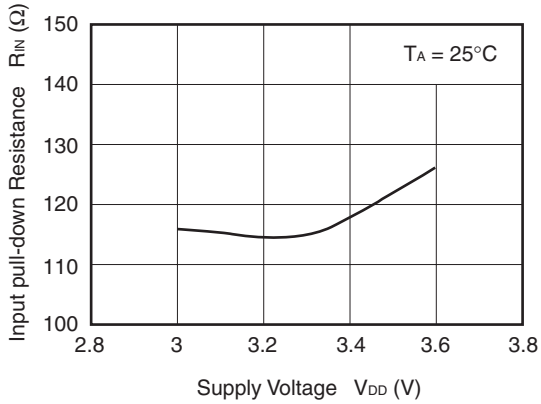
R_{ON1}, R_{ON2}-V_M Characteristics



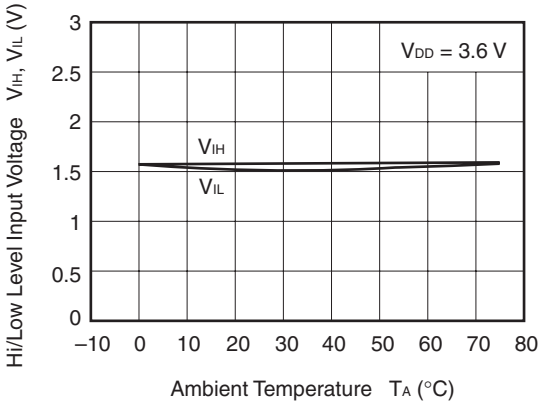
R_{IN}-T_A Characteristics



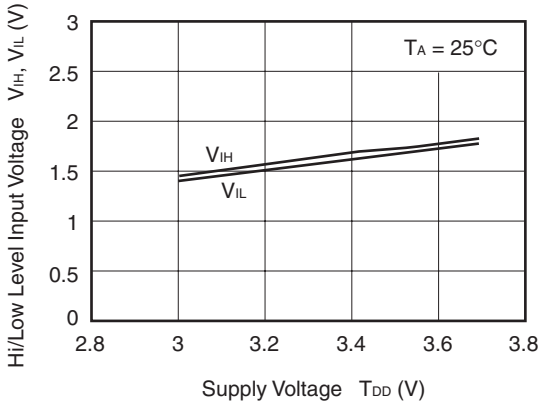
R_{IN}-V_{DD} Characteristics



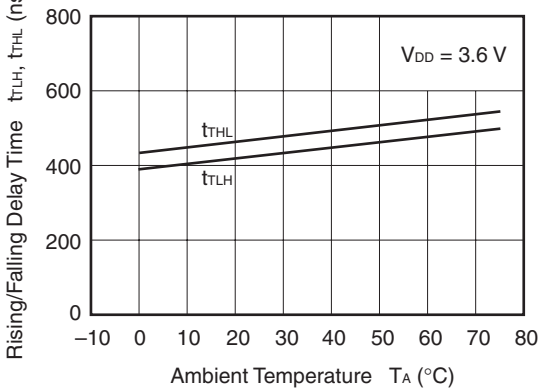
V_{IH}, V_{IL}-T_A Characteristics



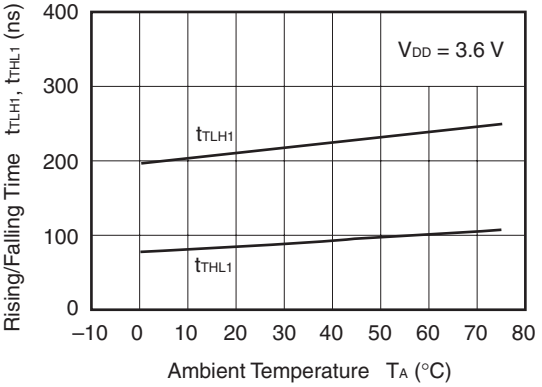
V_{IH}, V_{IL}-V_{DD} Characteristics



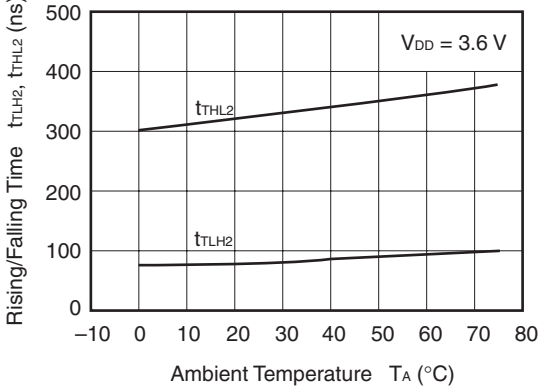
t_{TLH}, t_{THL}-T_A Characteristics



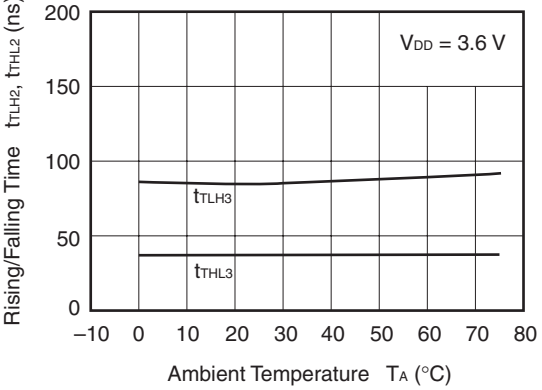
t_{TLH1}, t_{THL1}-T_A Characteristics



t_{TLH2}, t_{THL2}-T_A Characteristics

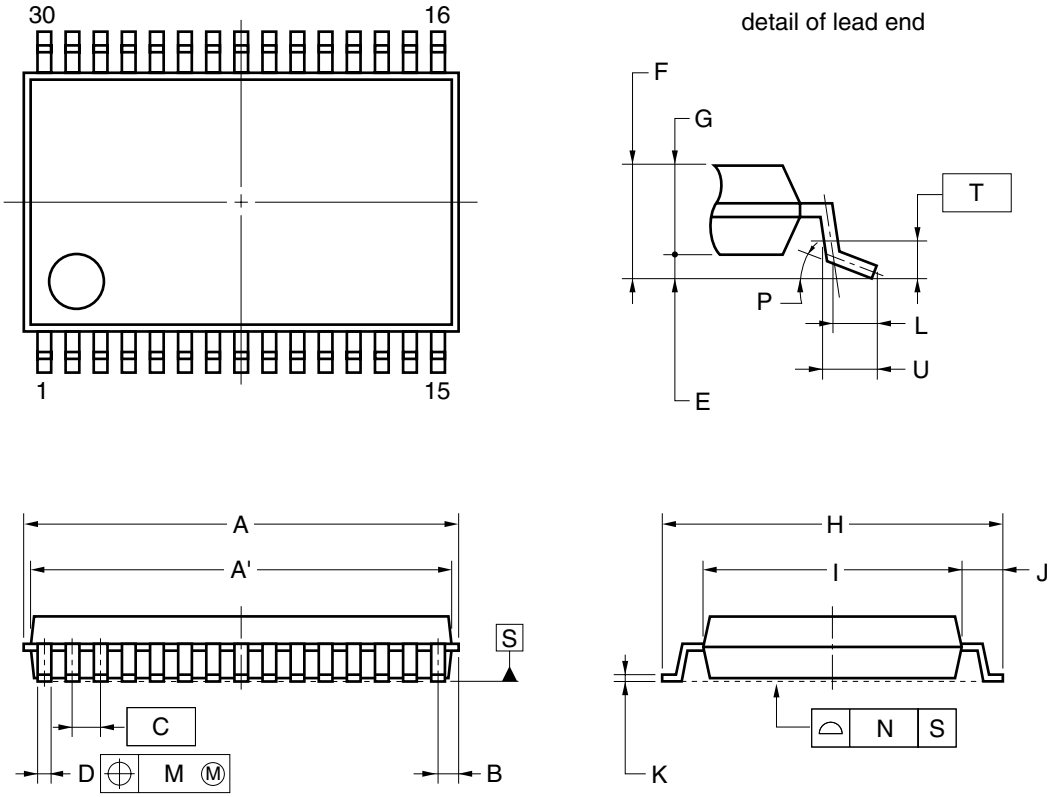


t_{TLH3}, t_{THL3}-T_A Characteristics



PACKAGE DRAWING

30-PIN PLASTIC TSSOP (7.62mm(300))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.10
A'	9.7±0.1
B	0.375
C	0.65 (T.P.)
D	0.24±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
H	8.1±0.1
I	6.1±0.1
J	1.0±0.1
K	0.145±0.025
L	0.5
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S30MC-65-6A4

RECOMMENDED SOLDERING CONDITIONS

The μPD168001 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD168001MC-6A4-A 30pin plastic TSSOP (7.62mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: None, Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended	IR60-00-3

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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