

INTEGRATED CIRCUITS

DATA SHEET

TDA4663T Baseband delay line

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC02

1996 Nov 22

Baseband delay line

TDA4663T

FEATURES

- Two delay lines, using the switched-capacitor technique, for a delay time of one horizontal line (1H) minus 55 ns (64 μ s – 55 ns)
- Adjustment-free application
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals [mostly colour-difference signals $\pm(R-Y)$ and $\pm(B-Y)$]
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 μ s line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Output buffer amplifiers.

GENERAL DESCRIPTION

The TDA4663T is an integrated baseband delay line circuit with a delay time of one horizontal line (1H) minus 55 ns (64 μ s – 55 ns).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{P1}	analog supply voltage (pin 9)	4.75	5	5.25	V
V _{P2}	digital supply voltage (pin 1)	4.75	5	5.25	V
I _{P(tot)}	total supply current	–	5.9	7.0	mA
V _{i(p-p)}	input signal PAL/NTSC (peak-to-peak value)				
	$\pm(R-Y)$; pin 16	–	1.3	–	V
	$\pm(B-Y)$; pin 14	–	1.3	–	V
G _v	gain $\frac{V_o}{V_i}$ of colour-difference output signals for PAL and NTSC				
	$\frac{V_{11}}{V_{16}}$	–1	0	+1	dB
	$\frac{V_{12}}{V_{14}}$	–1	0	+1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4663T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

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BLOCK DIAGRAM

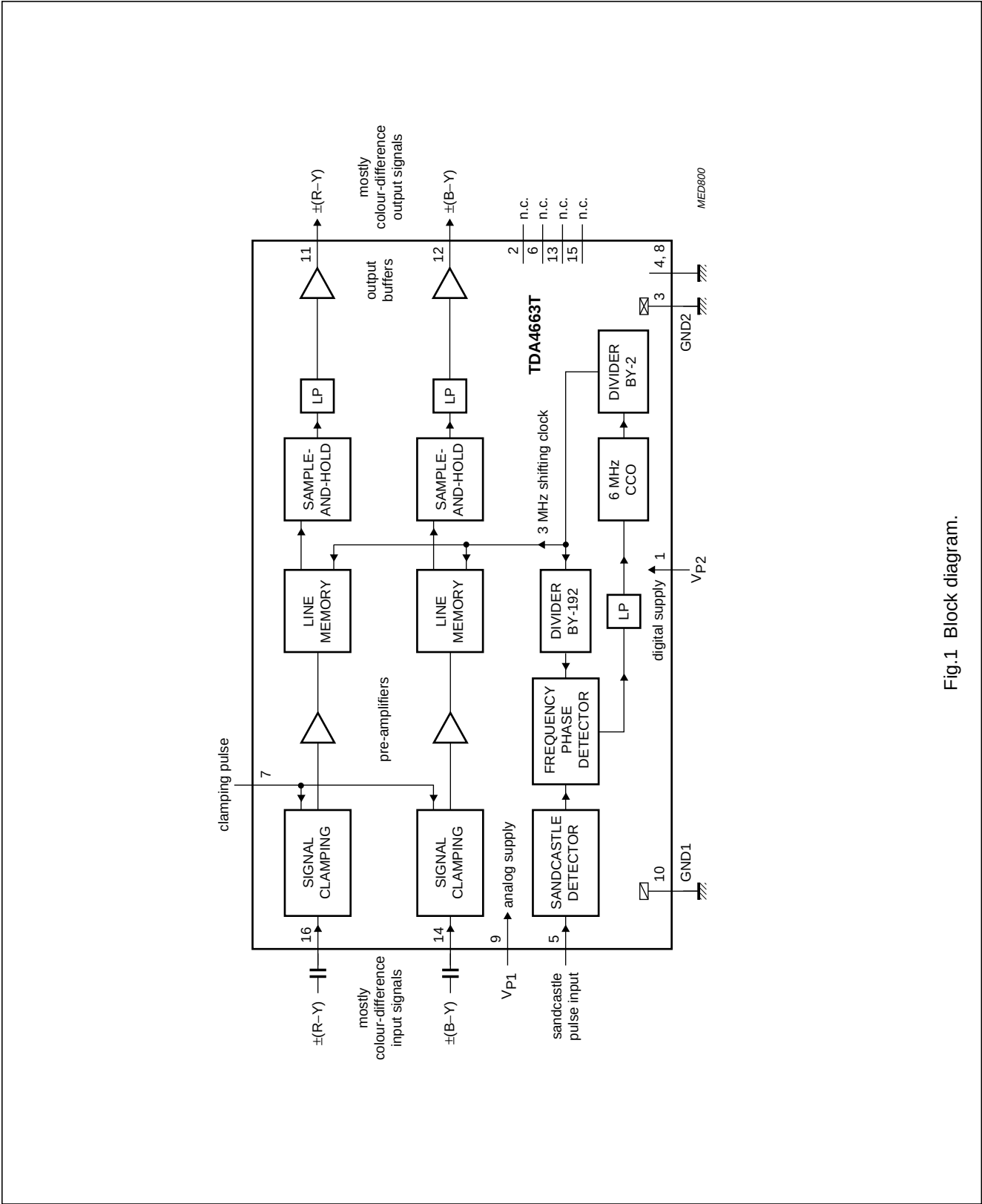


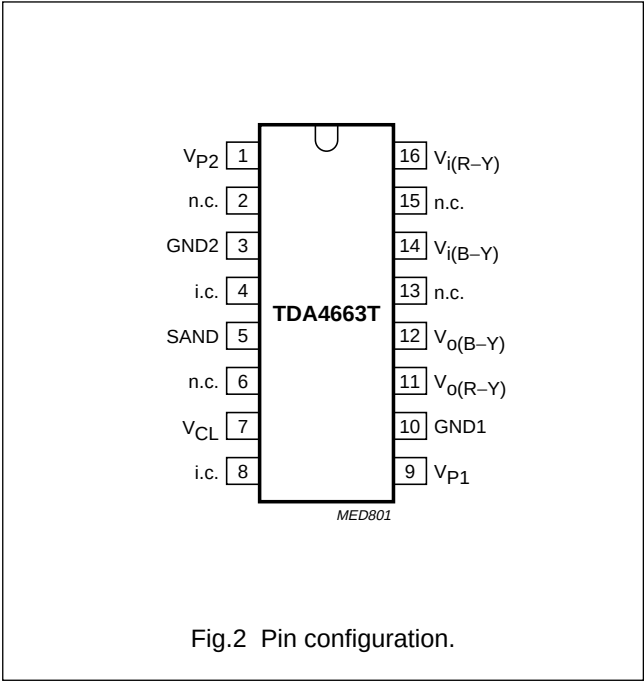
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V _{P2}	1	supply voltage for digital part (+5 V)
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
V _{CL}	7	clamping pulse input
i.c.	8	internally connected
V _{P1}	9	supply voltage for analog part (+5 V)
GND1	10	ground for analog part (0 V)
V _{o(R-Y)}	11	±(R-Y) output signal
V _{o(B-Y)}	12	±(B-Y) output signal
n.c.	13	not connected
V _{i(B-Y)}	14	±(B-Y) input signal
n.c.	15	not connected
V _{i(R-Y)}	16	±(R-Y) input signal



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{P1}	supply voltage (pin 9)		−0.5	+7	V
V _{P2}	supply voltage (pin 1)		−0.5	+7	V
V ₅	voltage on pin 5		−0.5	V _P + 1.0	V
V _n	voltage on pins 7, 11, 12, 14 and 16		−0.5	V _P	V
I _n	current on pins 7, 11 and 12		−	20	mA
T _{stg}	storage temperature		−25	+150	°C
T _{amb}	operating ambient temperature		−20	+70	°C
P _{tot}	total power dissipation		−	100	mW
V _{es}	electrostatic handling for all pins	note 1	−	±500	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air	220	K/W

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CHARACTERISTICS

$V_P = 5.0$ V; input signals as specified in characteristics with 75% colour bars;

super-sandcastle frequency of 15.625 kHz; $T_{amb} = 25$ °C; measurements taken in Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)		4.75	5	5.25	V
V_{P2}	digital supply voltage (pin 1)		4.75	5	5.25	V
I_{P1}	supply current		–	5.1	5.9	mA
I_{P2}	supply current		–	0.8	1.1	mA
Colour-difference input signals						
$V_{i(p-p)}$	input signal (peak-to-peak value) pin 16		–	1.3	–	V
	pin 14		–	1.3	–	V
$V_{i(max)(p-p)}$	maximum symmetrical input signal (peak-to-peak value) pin 16	before clipping	1.6	–	–	V
	pin 14	before clipping	1.6	–	–	V
$I_{14, 16}$	input leakage current (during picture content)		0.06	0.085	0.1	µA
$R_{14, 16}$	input resistance during clamping		–	–	40	kΩ
$C_{14, 16}$	input capacitance		–	–	10	pF
$V_{14, 16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
$V_{o(p-p)}$	output signal (peak-to-peak value) pin 11		–	1.3	–	V
	pin 12		–	1.3	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i14, 16} = 665$ mV (p-p)	–0.4	0	+0.4	dB
$V_{11, 12}$	DC output voltage	proportional to V_P	2.5	2.9	3.3	V
$R_{11, 12}$	output resistance		–	300	400	Ω
G_v	voltage gain $\frac{V_o}{V_i}$		–1	0	+1	dB
$V_{n(rms)}$	noise voltage (RMS value; pins 11 and 12)	$V_{i14, 16} = 0$ V; note 1	–	–	1.2	mV
$S/N(W)$	weighted signal-to-noise ratio (pins 11 and 12)	$V_o = 1$ V (p-p); note 1	–	54	–	dB
t_j	jitter of output signal to external sandcastle reference V_5		–	–	20	ns
$\alpha_{ct(11, 12)}$	crosstalk between channels	$V_{14} = 0$ V; $R_S = 300$ Ω; $V_{11} = 1.35$ V (p-p)	30	–	–	dB
$\alpha_{ct(12, 11)}$	crosstalk between channels	$V_{16} = 0$ V; $R_S = 300$ Ω; $V_{12} = 1.35$ V (p-p)	30	–	–	dB
$\alpha_{ct(14, 12)}$	crosstalk direct from input to output signal	$V_{16} = 0$ V; $R_S = 300$ Ω; $V_{14} = 1.35$ V (p-p)	30	–	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{ct(16, 11)}$	crosstalk direct from input to output signal	$V_{14} = 0 \text{ V}$; $R_S = 300 \Omega$; $V_{16} = 1.35 \text{ V (p-p)}$	30	–	–	dB
SVRR	supply voltage ripple rejection $\Delta V_{11, 12}/V_R$	$V_R = 100 \text{ mV (p-p)}$; $f_R = 10 \text{ Hz to } 1 \text{ kHz}$; $V_{11, 12} = 1.35 \text{ V (p-p)}$	34	–	–	dB
$V_{11, 12(p-p)}$	clamping offset during H-clamp (peak-to-peak value)	$V_{14} = V_{16} = 0 \text{ V}$; $R_S = 300 \Omega$	–	–	5	mV
$V_{11, 12(p-p)}$	unwanted signals (line-locked) (peak-to-peak value)	$V_{14} = V_{16} = 0 \text{ V}$; active video; $R_S = 300 \Omega$				
	residual clock (3 MHz)		–	–	6.25	mV
	meander		–	–	1.5	mV
	needles		–	–	2.5	mV
t_d	line delay time	for PAL signals	64 – 0.125	64 – 0.055	64 + 0.015	μs
		for NTSC signals	63.555 – 0.125	63.555 – 0.055	63.555 + 0.015	μs
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency/sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 2	4.0	–	$V_P + 1.0$	V
t_{BK}	top pulse duration		–	2.5	–	μs
V_{slice}	internal slicing level		$V_5 - 1.0$	–	$V_5 - 0.5$	V
I_i	input current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
t_{li}	lock-in time for PLL		–	–	1	ms
Clamping pulse input (pin 7)						
V_{clamp}	clamping pulse ON		3.5	$V_P - 0.1$	V_P	V
	clamping pulse OFF		–0.5	+0.1	+1.5	V
I_i	input current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
t_{clamp}	clamping pulse duration		0.1	2	3	μs
t_r	rise time		10	–	–	ns
t_f	fall time		10	–	–	ns

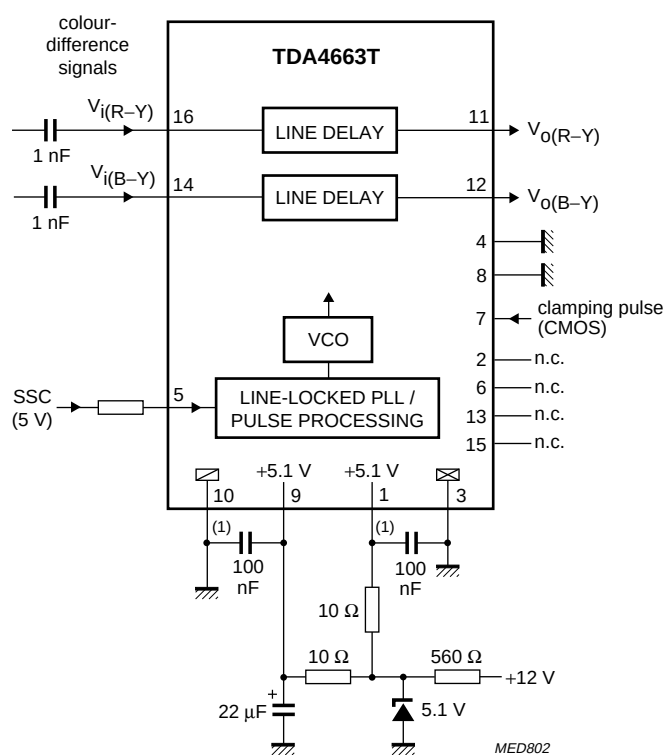
Notes

- Noise voltage at $f = 10 \text{ kHz to } 1 \text{ MHz}$; $R_S < 300 \Omega$.
- The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

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APPLICATION INFORMATION



(1) Positioned close to pins.

Fig.3 Application circuit.

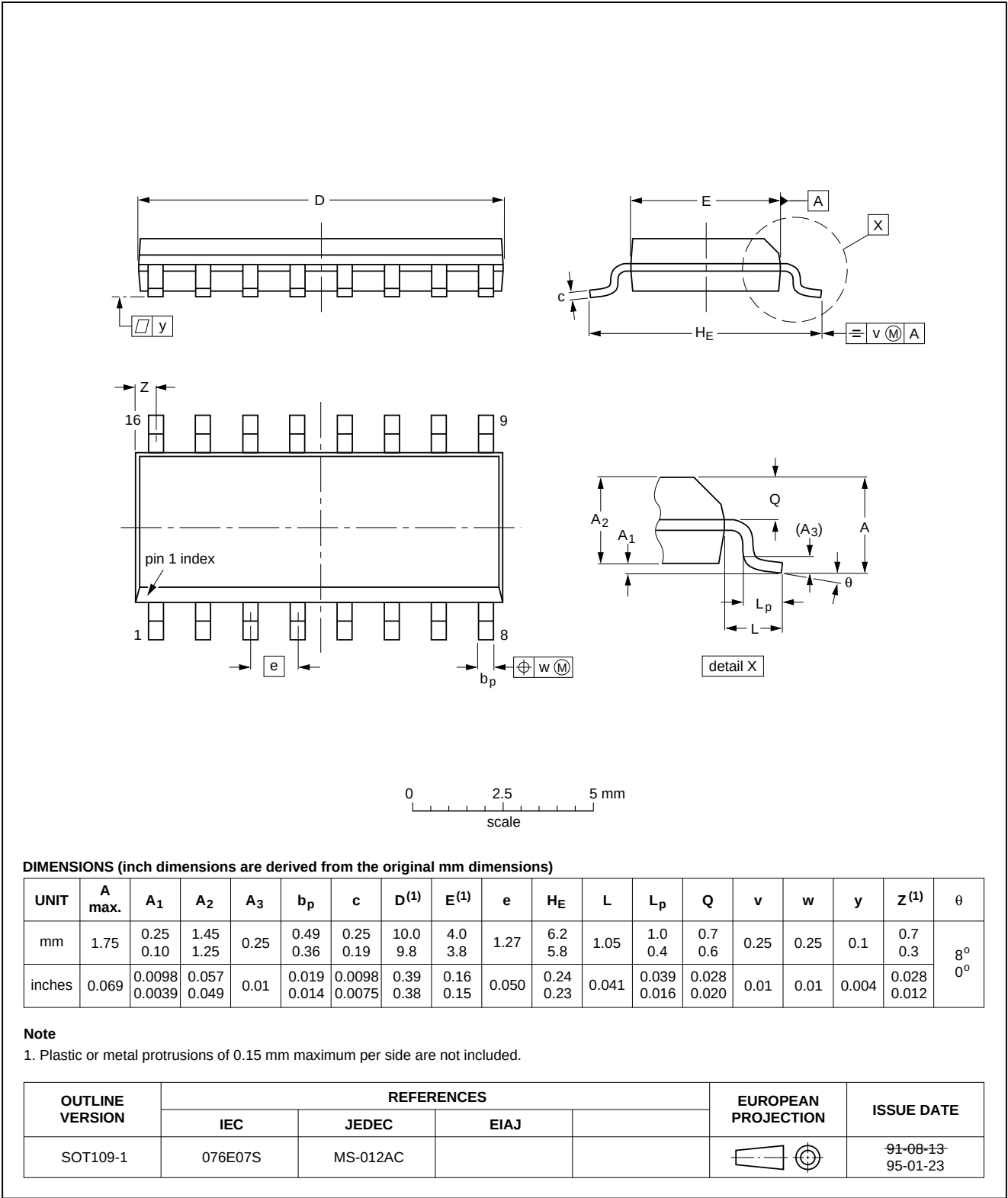
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoprojekt, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

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