

## 5-V Low-Drop Fixed Voltage Regulator

TLE 4270

### Features

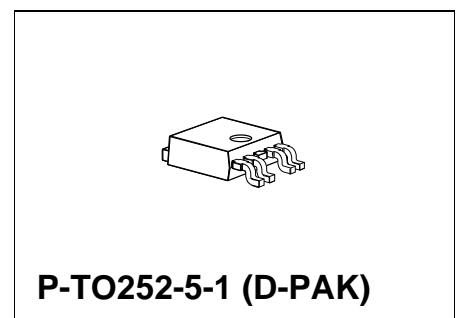
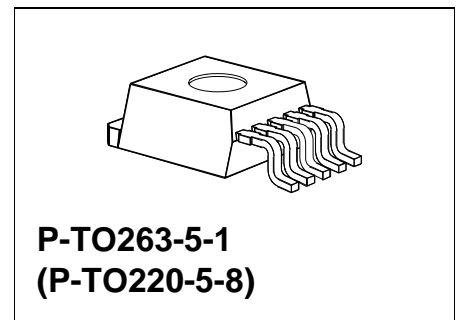
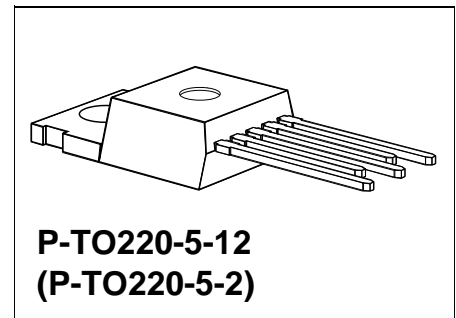
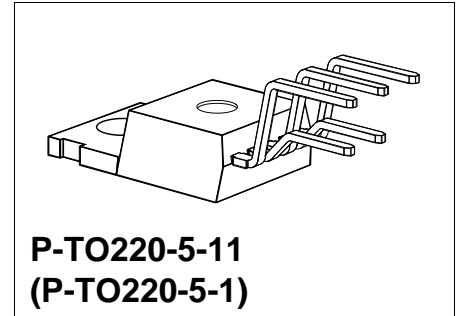
- Output voltage tolerance  $\leq \pm 2\%$
- Low-drop voltage
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V ( $\leq 400$  ms)
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Adjustable reset time
- ESD protection  $> 4000$  V

Type	Ordering Code	Package
TLE 4270	Q67000-A9209-A903	P-TO220-5-11
TLE 4270 S	Q67000-A9243-A904	P-TO220-5-12
TLE 4270 G	Q67006-A9201-A901	P-TO263-5-1
▼ TLE 4270	Q67000-A9209-A801	P-TO220-5-1
▼ TLE 4270 S	Q67000-A9243-A802	P-TO220-5-2
▼ TLE 4270 G	Q67006-A9201-A802	P-TO220-5-8
● TLE 4270 D	Q67006-A9360	P-TO252-5-1

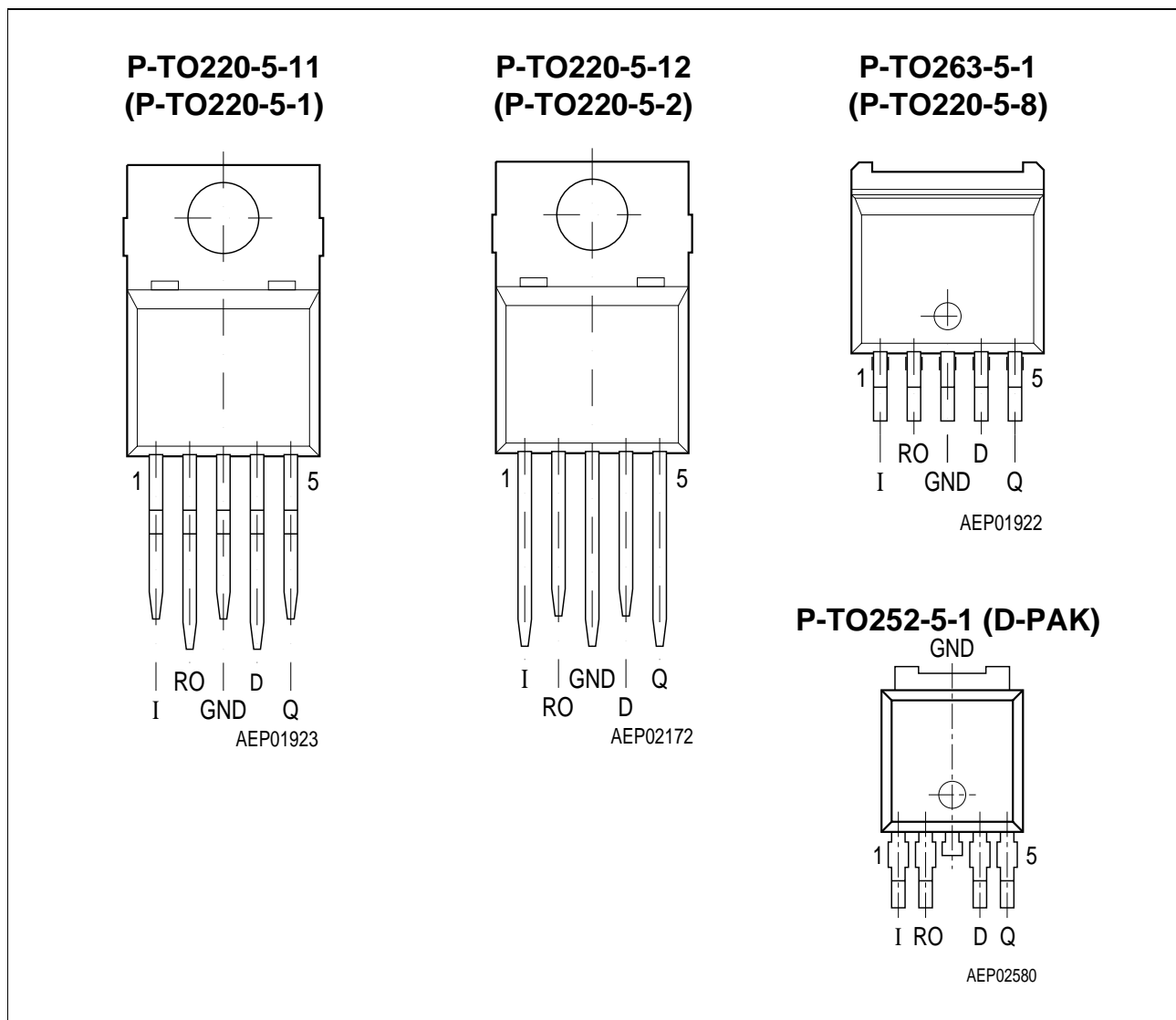
▼ Not for new design      ● New type

### Functional Description

This device is a 5-V low-drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V,  $\leq 400$  ms). Up to an input voltage of 26 V and for an output current up to 550 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and temperature protection that disables the circuit at unpermissibly high temperatures.



## Pin Configuration (top view)



**Figure 1**

## Pin Definitions and Functions

Pin	Symbol	Function
1	I	<b>Input</b> ; block to ground directly on the IC with ceramic capacitor
2	RO	<b>Reset Output</b> ; the open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.
3	GND	<b>Ground</b> ; internally connected to heatsink.
4	D	<b>Reset Delay</b> ; connect a capacitor to ground for delay time adjustment.
5	Q	<b>5-V Output</b> ; block to ground with 22 μF capacitor, ESR < 3 Ω.

### Application Description

The IC regulates an input voltage in the range of  $5.5\text{ V} < V_I < 36\text{ V}$  to  $V_{Qnom} = 5.0\text{ V}$ . Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. A reset signal is generated for an output voltage of  $V_Q < 4.5\text{ V}$ . The delay for power-on reset can be set externally with a capacitor.

### Design Notes for External Components

An input capacitor  $C_I$  is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx.  $1\ \Omega$  in series with  $C_I$ . An output capacitor  $C_Q$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values of  $C_Q \geq 22\ \mu\text{F}$  and an ESR of  $< 3\ \Omega$ .

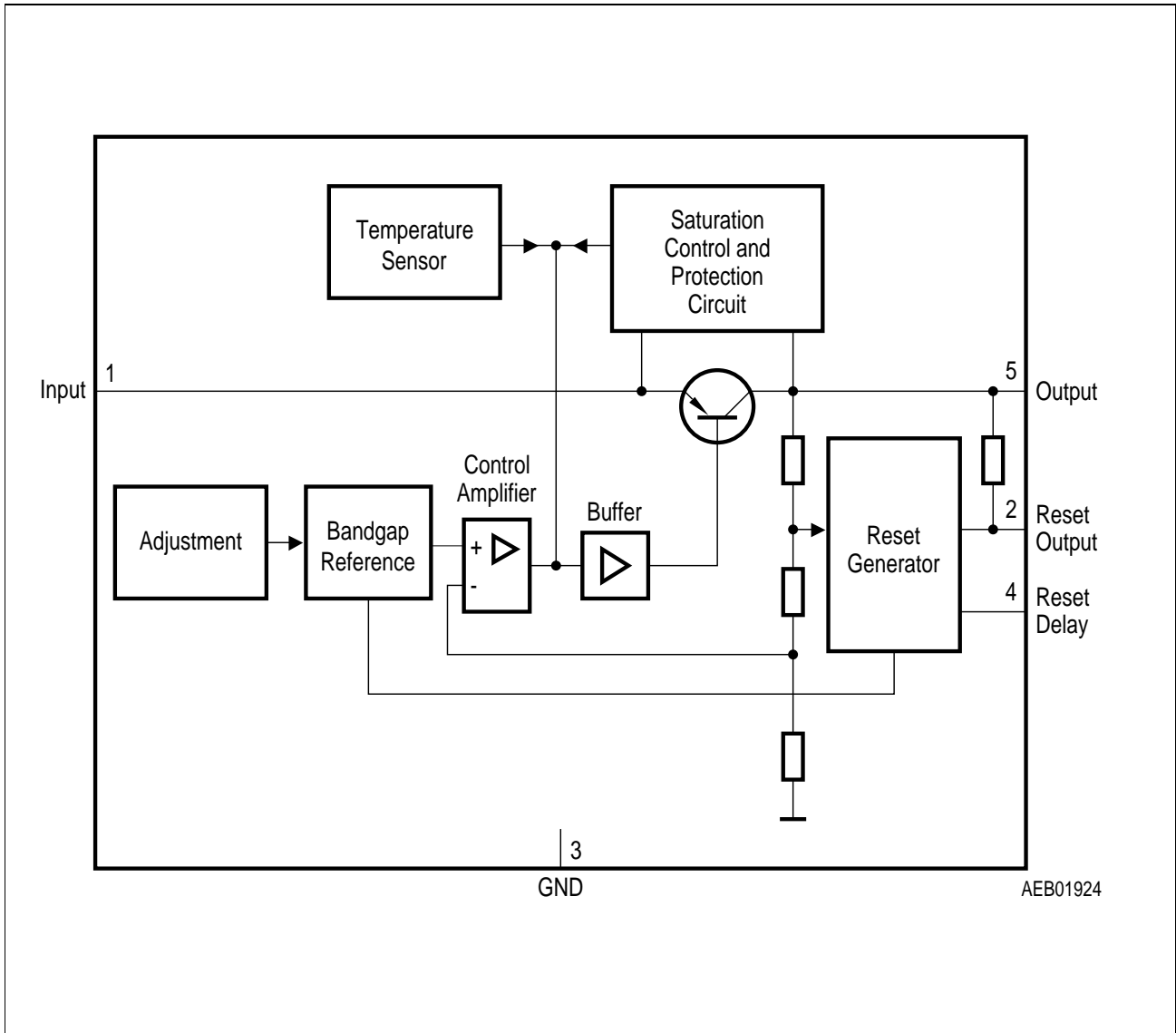
### Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

If the output voltage decreases below 4.5 V, an external capacitor  $C_D$  on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below  $V_{DRL}$ , a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above 4.5 V,  $C_D$  will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches  $V_{DU}$  and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of  $C_D$ .

The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity



**Figure 2**  
**Block Diagram**

**Absolute Maximum Ratings** $T_j = -40$  to  $150$  °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		

**Input**

Voltage	$V_I$	- 42	42	V	$t \leq 400$ ms internally limited
Voltage	$V_I$		65	V	
Current	$I_I$				

**Reset Output**

Voltage	$V_R$	- 0.3	7	V	Internally limited
Current	$I_R$				

**Reset Delay**

Voltage	$V_D$	- 0.3	7	V	Internally limited
Current	$I_D$				

**Output**

Voltage	$V_Q$	- 1.0	16	V	Internally limited
Current	$I_Q$				

**Ground**

Current	$I_{GND}$	- 0.5	-	A	-
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**Temperatures**

Junction temperature	$T_j$		150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	

Optimum reliability and life time are guaranteed if the junction temperature does not exceed  $125$  °C in operating mode. Operation at up to the maximum junction temperature of  $150$  °C is possible in principle. Note, however, that operation at the maximum permitted ratings could affect the reliability of the device.

## Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage	$V_I$	6	42	V	–
Junction temperature	$T_j$	– 40	150	°C	–

## Thermal Resistance

Junction ambient	$R_{thja}$	–	65 70	K/W K/W	TO263, TO252 <sup>1)</sup>
Junction case	$R_{thjc}$ $Z_{thjc}$	–	3 2	K/W K/W	$t < 1$ ms (TO-220/263 Packages)

1) Soldered in, min. footprint

## Characteristics

$V_I = 13.5$  V;  $-40$  °C  $\leq T_j = \leq 125$  °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage	$V_Q$	4.90	5.00	5.10	V	$5$ mA $\leq I_Q \leq 550$ mA; $6$ V $\leq V_I \leq 26$ V
Output voltage	$V_Q$	4.90	5.00	5.10	V	$26$ V $\leq V_I \leq 36$ V; $I_Q \leq 300$ mA
Output current limiting	$I_{Qmax}$	650	850	–	mA	$V_Q = 0$ V
Current consumption $I_q = I_I - I_Q$	$I_q$	–	1	1.5	mA	$I_Q = 5$ mA
Current consumption $I_q = I_I - I_Q$	$I_q$	–	55	75	mA	$I_Q = 550$ mA
Current consumption $I_q = I_I - I_Q$	$I_q$	–	70	90	mA	$I_Q = 550$ mA; $V_I = 5$ V
Drop voltage	$V_{dr}$	–	350	700	mV	$I_Q = 550$ mA <sup>1)</sup>

## Characteristics (cont'd)

$V_I = 13.5 \text{ V}$ ;  $-40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Load regulation	$\Delta V_Q$	–	25	50	mV	$I_Q = 5 \text{ to } 550 \text{ mA}$ ; $V_I = 6 \text{ V}$
Supply voltage regulation	$\Delta V_Q$	–	12	25	mV	$V_I = 6 \text{ to } 26 \text{ V}$ $I_Q = 5 \text{ mA}$
Power supply Ripple rejection	$PSRR$	–	54	–	dB	$f_r = 100 \text{ Hz}$ ; $V_r = 0.5 V_{SS}$

## Reset Generator

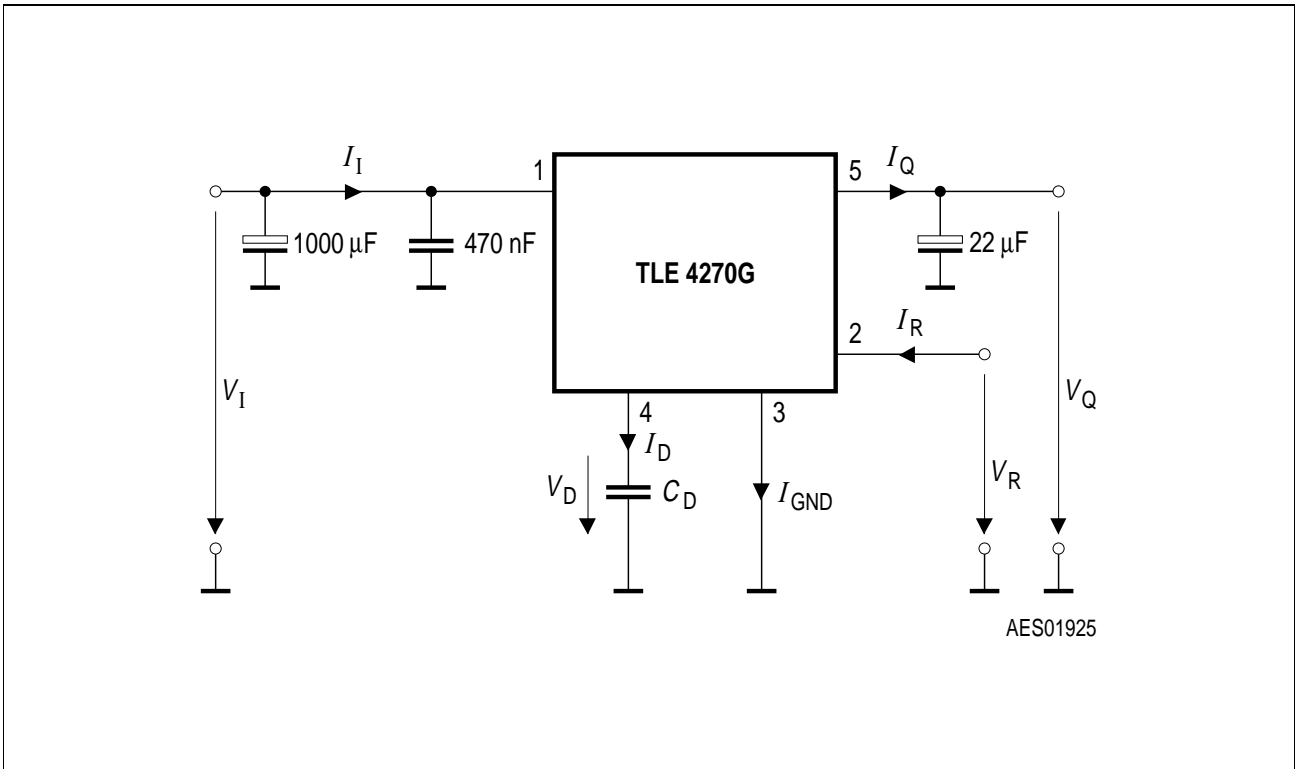
Switching threshold	$V_{RT}$	4.5	4.65	4.8	V	–
Reset High voltage	$V_{ROH}$	4.5	–	–	V	–
Reset low voltage	$V_{ROL}$	–	60	–	mV	$R_{\text{intern}} = 30 \text{ k}\Omega^2$ ); $1.0 \text{ V} \leq V_Q \leq 4.5 \text{ V}$
Reset low voltage	$V_{ROL}$	–	200	400	mV	$I_R = 3 \text{ mA}$ , $V_Q = 4.4 \text{ V}$
Reset pull-up	$R$	18	30	46	k $\Omega$	internally connected to Q
Lower reset timing threshold	$V_{DRL}$	0.2	0.45	0.8	V	$V_Q < V_{RT}$
Charge current	$I_d$	8	14	25	$\mu\text{A}$	$V_D = 1.0 \text{ V}$
Upper timing threshold	$V_{DU}$	1.4	1.8	2.3	V	–
Delay time	$t_d$	–	13	–	ms	$C_D = 100 \text{ nF}$
Reset reaction time	$t_{RR}$	–	–	3	$\mu\text{s}$	$C_D = 100 \text{ nF}$

## Overvoltage Protection

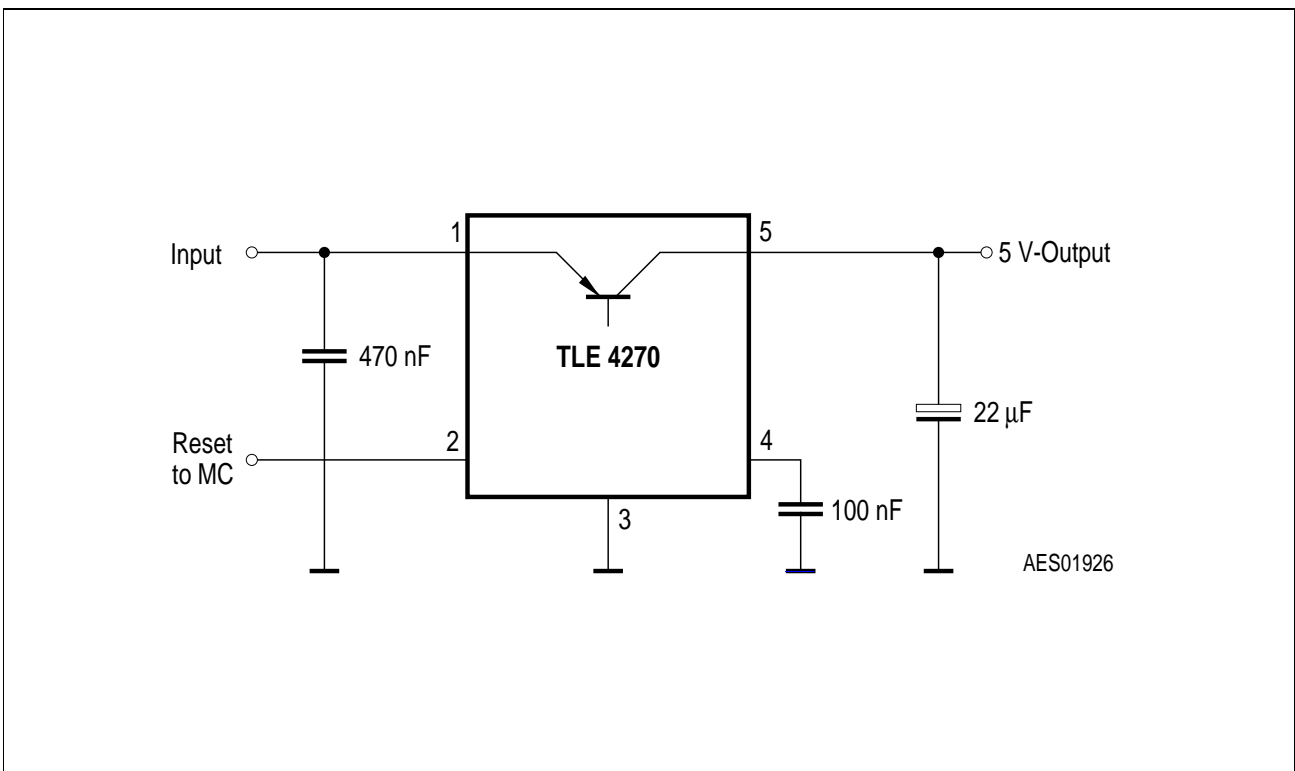
Turn-Off voltage	$V_{I,ov}$	42	44	46	V	–
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<sup>1)</sup> Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

<sup>2)</sup> Reset peak is always lower than 1.0 V.

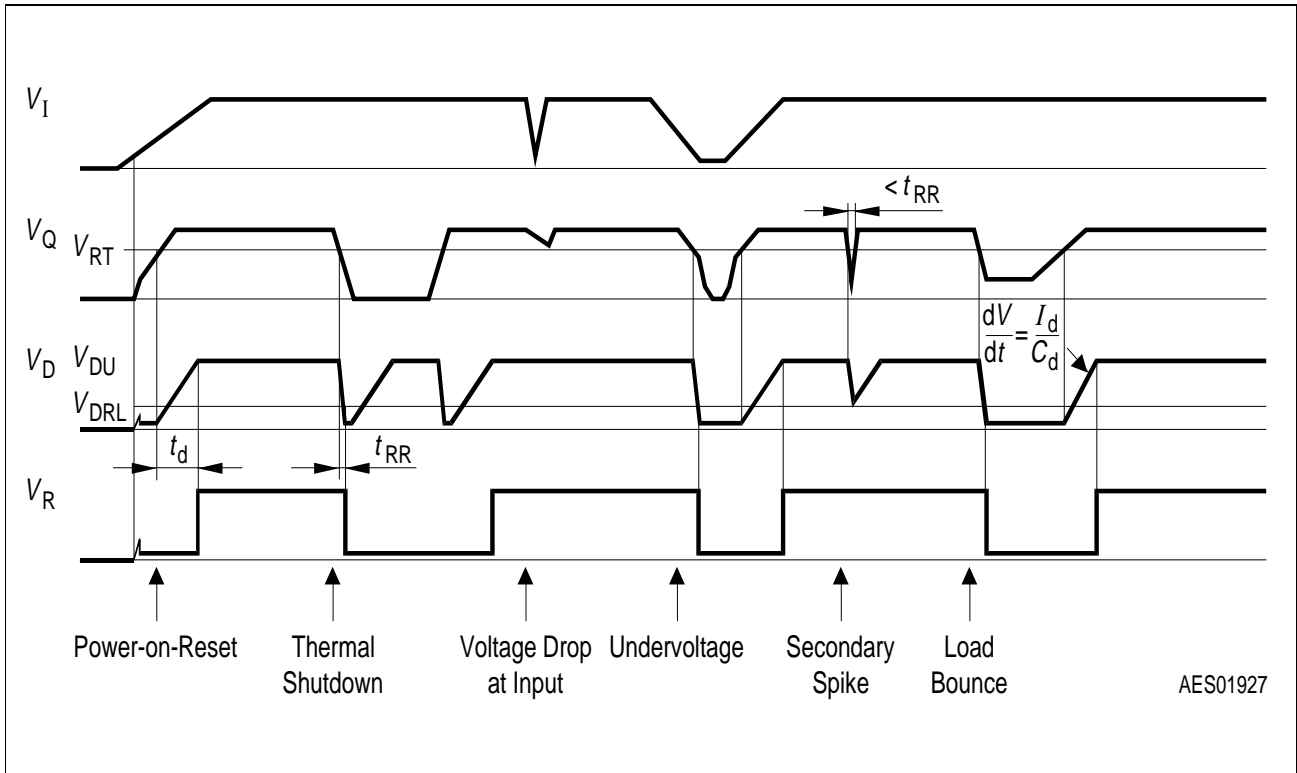


**Figure 3**  
**Test Circuit**



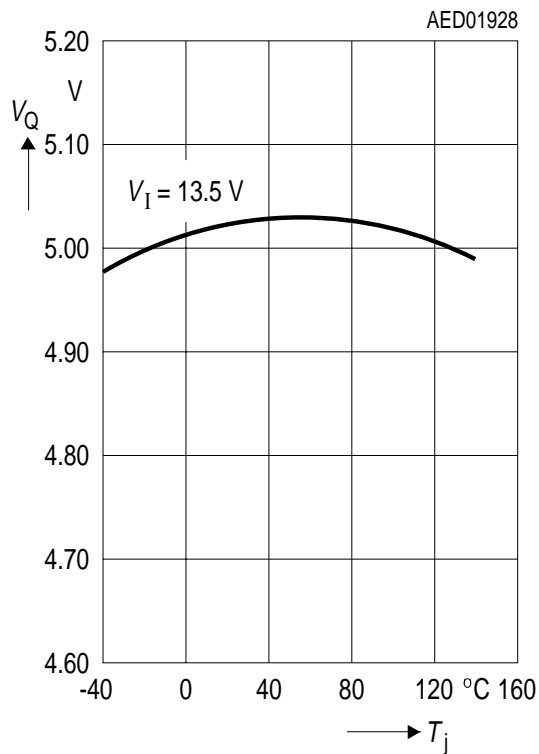
**Figure 4**  
**Application Circuit**



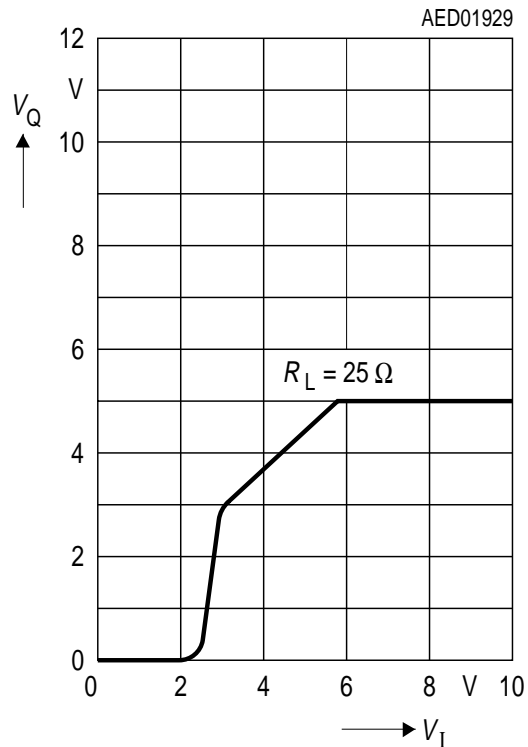


**Figure 5**  
**Time Response**

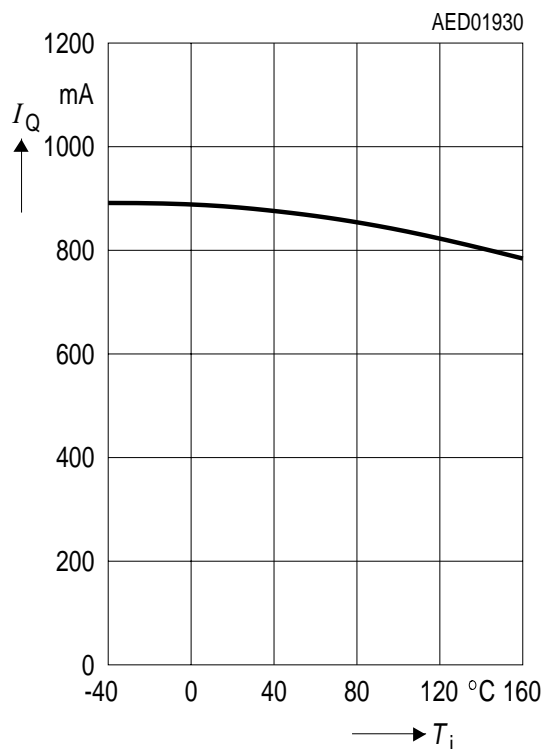
Output Voltage  $V_Q$  versus Temperature  $T_j$



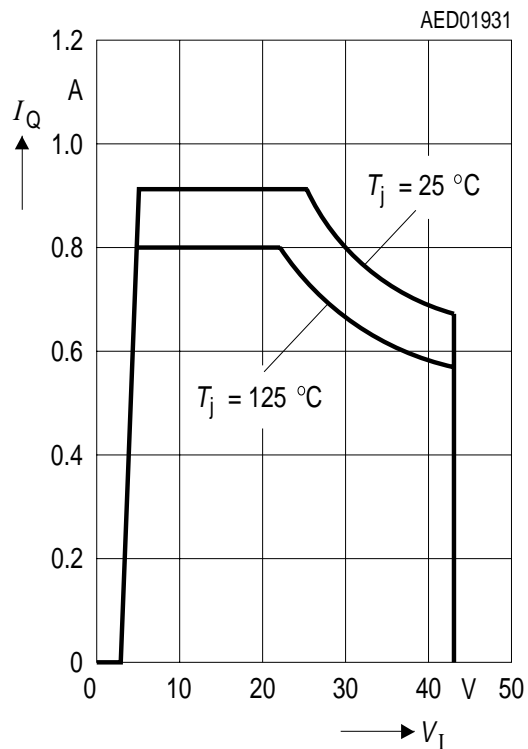
Output Voltage  $V_Q$  versus Input Voltage  $V_I$



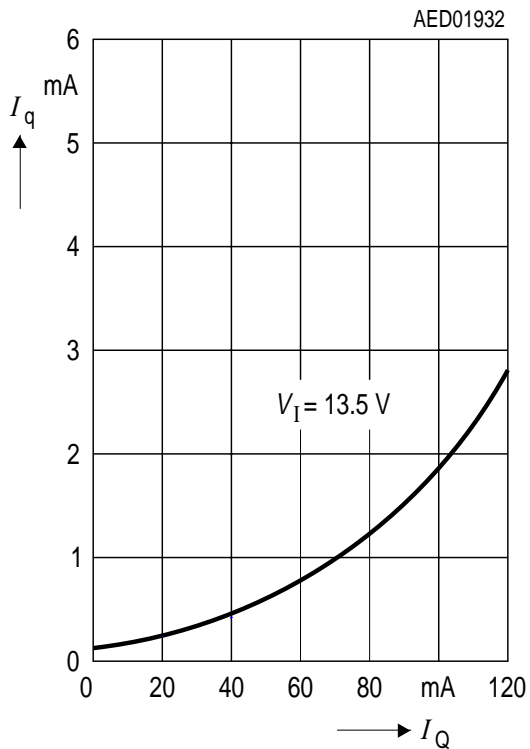
Output Current  $I_Q$  versus Temperature  $T_j$



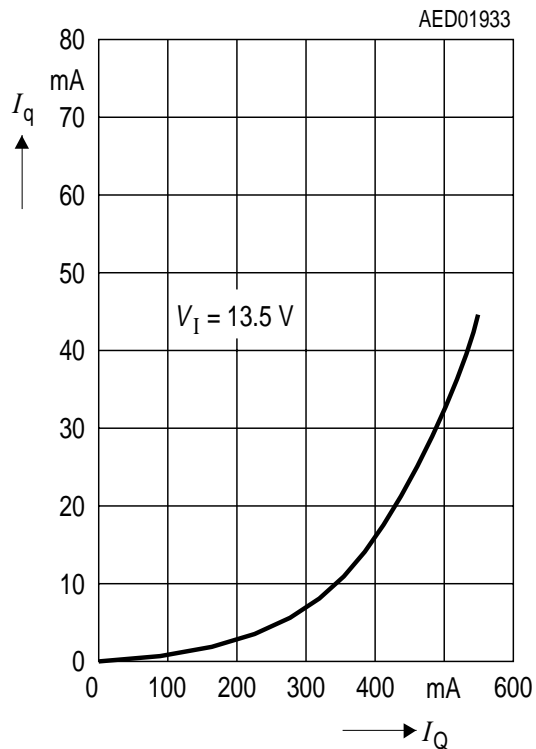
Output Current  $I_Q$  versus Input Voltage  $V_I$



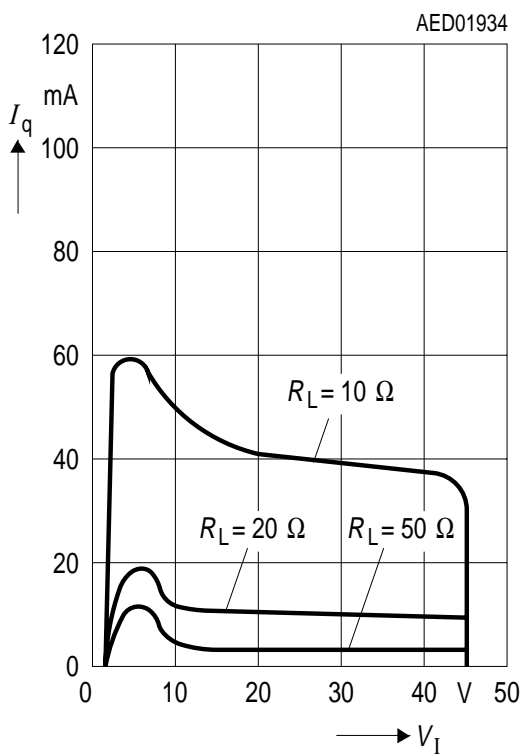
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



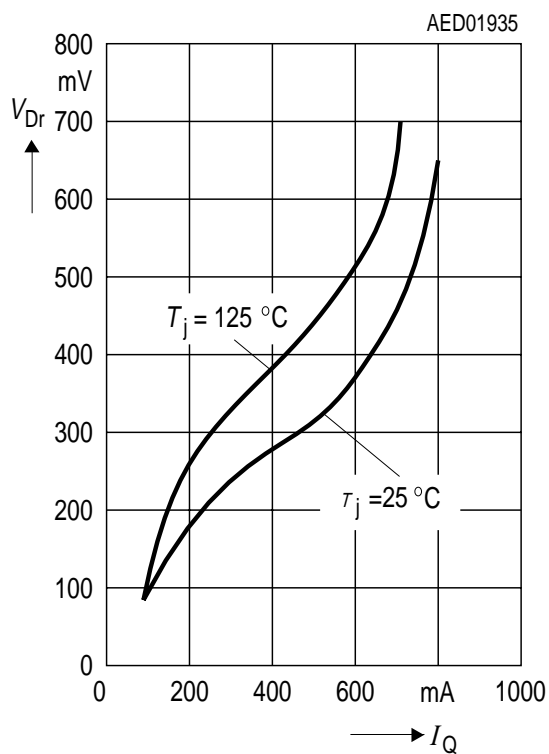
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



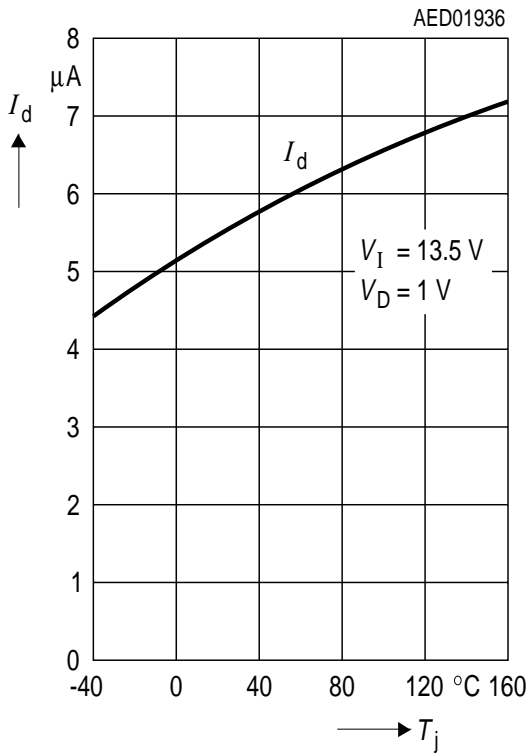
**Current Consumption  $I_q$  versus Input Voltage  $V_I$**



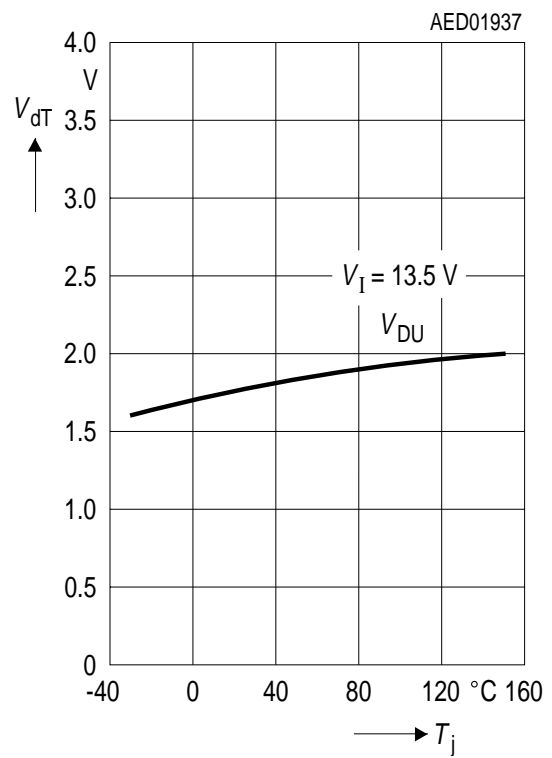
**Drop Voltage  $V_{Dr}$  versus Output Current  $I_Q$**



Charge Current  $I_d$   
versus Temperature  $T_j$



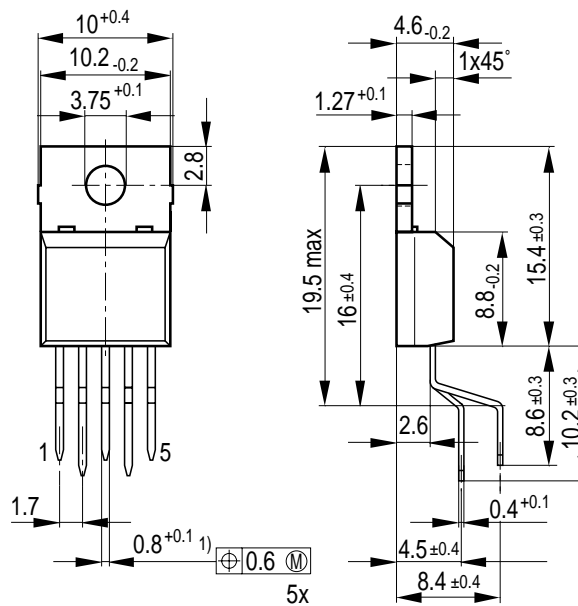
Delay Switching threshold  $V_{dU}$   
versus Temperature  $T_j$



## Package Outlines

### P-TO220-5-1

(Plastic Transistor Single Outline)



- 1) 1<sub>-0.15</sub> at dam bar (max 1.8 from body)
- 1) 1<sub>-0.15</sub> im Dichtstegbereich (max 1.8 vom Körper)

GPT05107

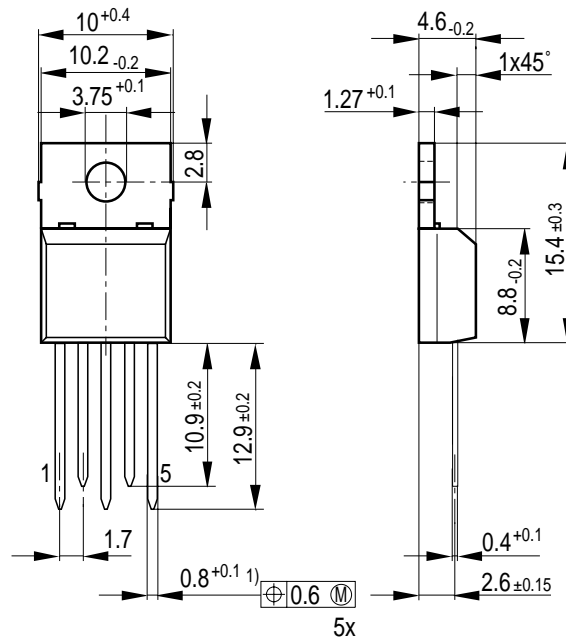
### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

**P-TO220-5-2**

(Plastic Transistor Single Outline)



- 1)  $1_{-0.15}$  at dam bar (max 1.8 from body)
- 1)  $1_{-0.15}$  im Dichtstegbereich (max 1.8 vom Körper)

GPT05256

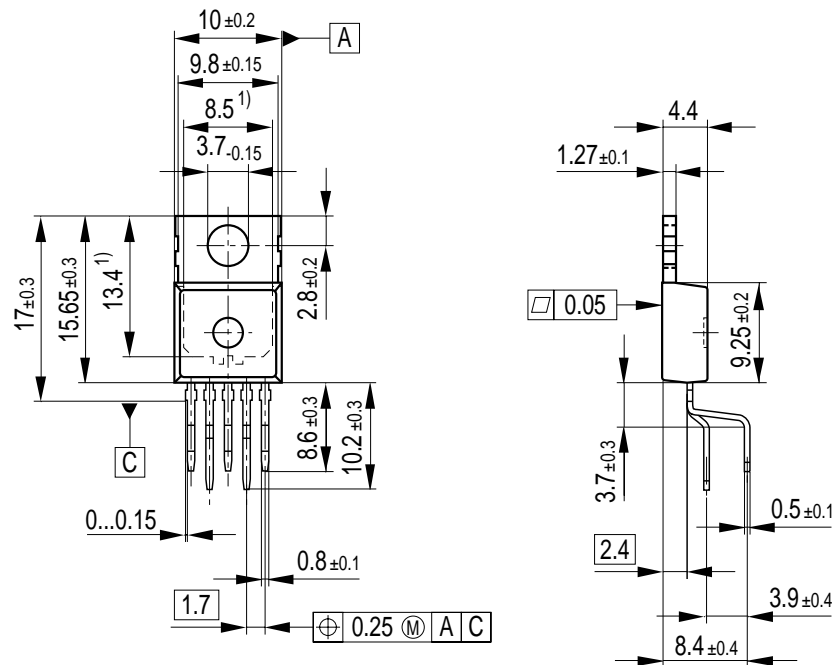
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

**P-TO220-5-11**

(Plastic Transistor Single Outline)



1) Typical  
All metal surfaces tin plated, except area of cut.

GPT09064

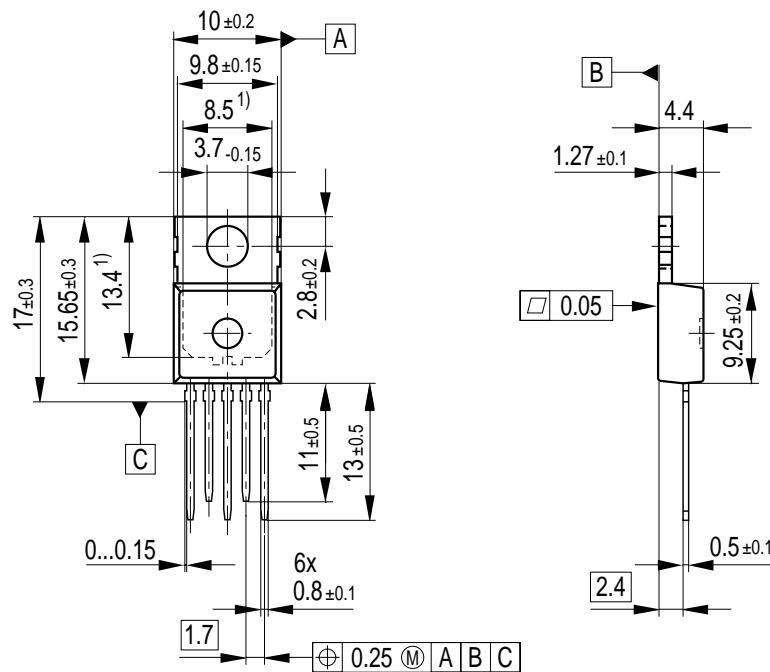
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

**P-TO220-5-12**

(Plastic Transistor Single Outline)



Typical

1) All metal surfaces tin plated, except area of cut.

GPT09065

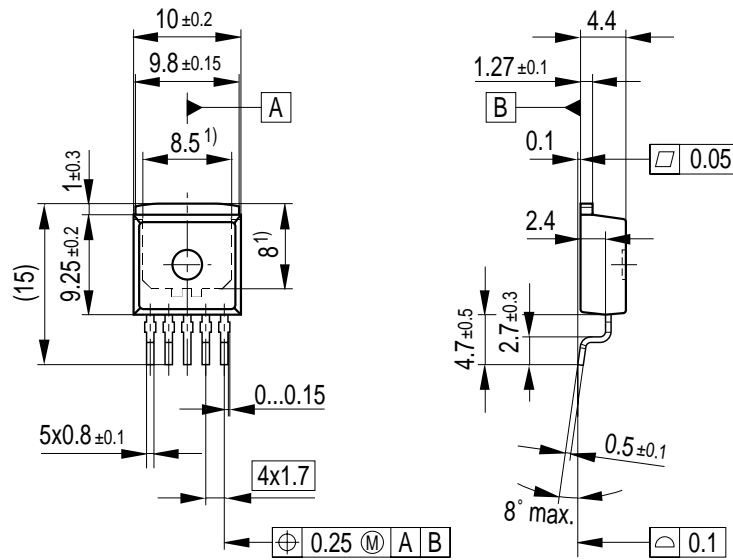
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm



**P-TO263-5-1**  
(Plastic Transistor Single Outline)



1) Typical  
All metal surfaces tin plated, except area of cut.

GPT09113

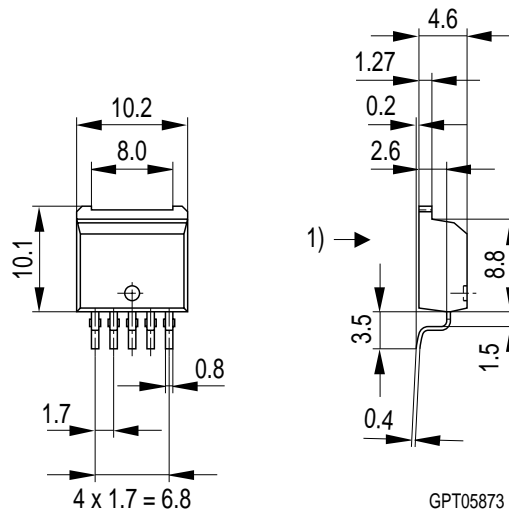
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**P-TO220-5-8**  
(Plastic Transistor Single Outline)



1) shear and punch direction burr free surface

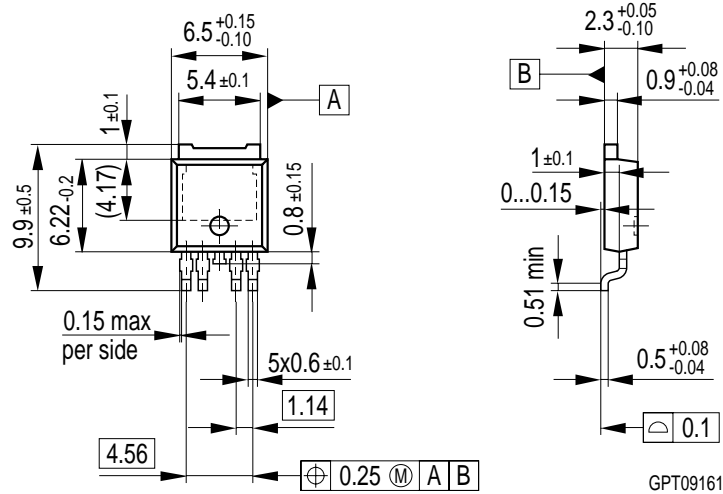
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**P-TO252-5-1**  
(Plastic Transistor Single Outline)



All metal surfaces tin plated, except area of cut.

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm