SIEMENS

Smart Quad Channel Low-Side Switch

Features

- Low ON-resistance 2 x 0.2 Ω , 2 x 0.35 Ω (typ.)
- Power - SO 20 - Package with integrated cooling area
- Overload shutdown
- Selective thermal shutdown
- Status monitoring
- Overvoltage protection
- Shorted circuit protection
- Standby mode with low current consumption
- µC compatible input
- **E**lecto**s**tatic **d**ischarge (ESD) protection

Product Summary

Supply voltage	V_S	4.8 - 32	V
Drain source voltage	$V_{DS(AZ)max}$	60	V
On resistance	$R_{ON(typ)\ 1,2}$	0.2	Ω
	$R_{ON(typ)\ 3,4}$	0.35	Ω
Output current	$I_{D\ 1,2}$	2 x 5	A
	$I_{D\ 3,4}$	2 x 3	A

P-DSO-20-10

Application

- All kinds of resistive and inductive loads (relays,electromagnetic valves)
- µC compatible power switch for 12 and 24 V applications
- Solenoid control switch in automotive and industrial control systems

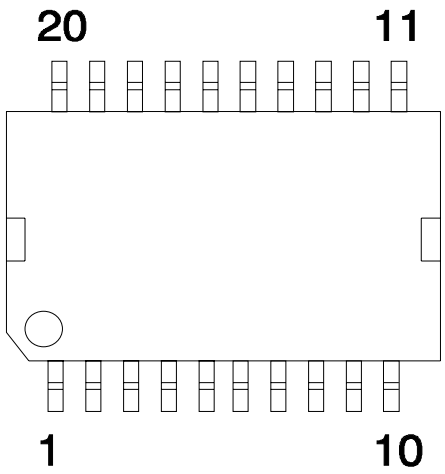
General description

Quad channel Low-Side-Switch (2x5A/2x3A) in Smart Power Technology (SPT) with four seperate inputs and four open drain DMOS output stages. The TLE 5226 is fully protected by embedded protection functions and designed for automotive and industrial applications.

Pin Description

Pin	Symbol	Function
1	GND	Ground
2	OUT1	Power Output channel 1
3	ST1	Status Output channel 1
4	IN4	Control Input channel 4
5	VS	Supply Voltage
6	STBY	Standby
7	IN3	Control Input channel 3
8	ST2	Status Output channel 2
9	OUT2	Power Output channel 2
10	GND	Ground
11	GND	Ground
12	OUT3	Power Output channel 3
13	ST3	Status Output channel 3
14	IN2	Control Input channel 2
15	GND	Ground Logic
16	ENA	Enable Input for all four channels
17	IN1	Control Input channel 1
18	ST4	Status Output channel 4
19	OUT4	Power Output channel 4
20	GND	Ground

Pin Configuration (Top view)



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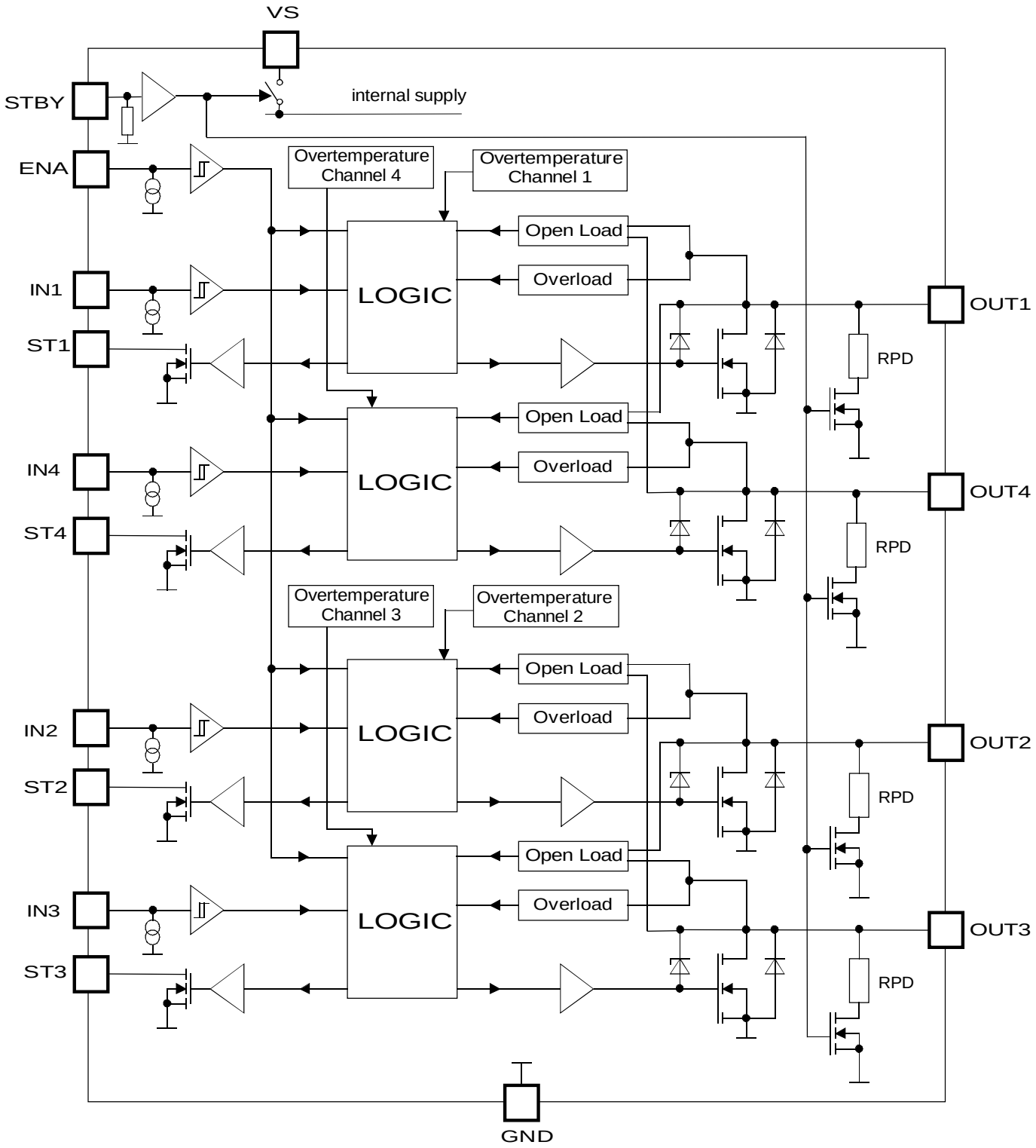
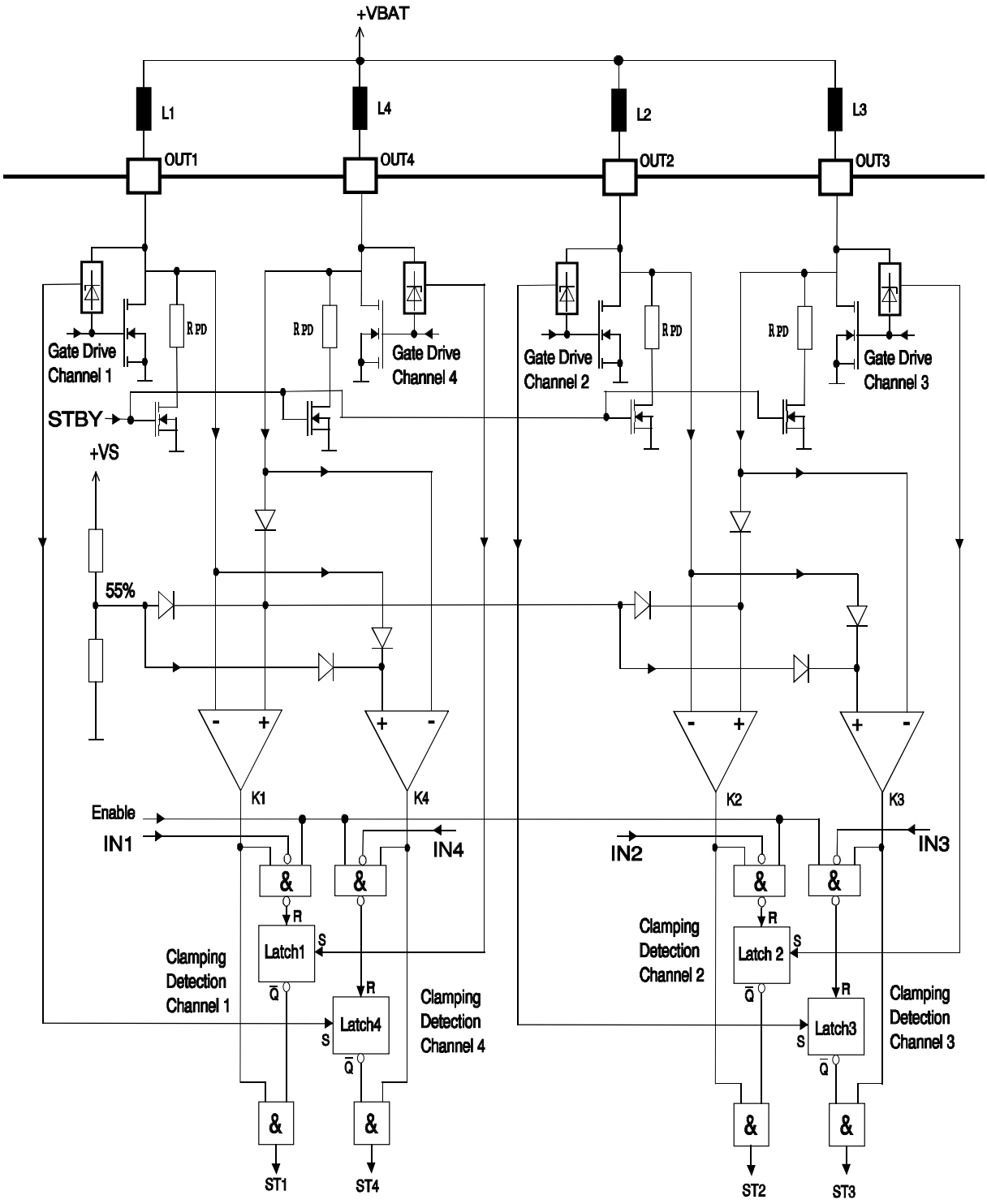
Block Diagram



Block Diagram of Open Load Detection



Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply voltage	V_S	-0.3 ... + 40	V
Supply voltage operational range	V_S	+ 4.8 ... + 32	V
Continuous drain source voltage (OUT1...OUT4)	V_{DS}	40	V
Input voltage IN1 to IN4, ENA	V_{IN} , V_{ENA}	- 0.3 ... + 6	V
Input voltage STBY	V_{STBY}	- 0.3 ... + 40	
Status output voltage	V_{ST}	- 0.3 ... + 32	V
Operating temperature range	T_j	- 40 ... + 150	°C
Storage temperature range	T_{stg}	- 55 ... + 150	
Output current per channel	$I_{D(lim)}$	self limited	A
Output current at reversal supply	$I_{D\ 1,2}$	- 4	A
	$I_{D\ 3,4}$	- 2	
Status output current	I_{ST}	- 5 ... + 5	mA
Inductive load switch off dissipation energy T_j = 25°C	E_{AS}	50	mJ
Thermal resistance			K/W
junction - case	R_{thJC}	4.5	
junction - ambient @ min. footprint	R_{thJA}	50	
junction - ambient @ 6 cm^2 cooling area		40	

Test board for

6 cm^2 cooling area

min. footprint

Electrical Characteristics

Parameter and Conditions V_S = 4.8 to 18 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
1. Power Supply (V_S)						
Supply current (Outputs ON)		I_S			8	mA
Supply current (Outputs OFF) V_{ENA} = L, V_{STBY} = H		I_S			4	mA
Operating voltage		V_S	4.8		32	V
Standby current	V_{STBY} = L	I_S			10	µA
2. Power Outputs						
ON state resistance Channel 1,2	T_j = 25 ° C	$R_{DS(ON)}$		0.2		Ω
I_D = 1A; $V_S \geq$ 9.5 V	T_j = 125°C [1]				0.5	
ON state resistance Channel 3,4	T_j = 25 ° C	$R_{DS(ON)}$		0.35		Ω
I_D = 1A; $V_S \geq$ 9.5 V	T_j = 125°C [1]				0.75	
Z-Diode clamping voltage (OUT1...4)	$I_D \geq$ 100 mA	$V_{DS(AZ)}$	45		60	V
Pull down resistor	T_j = 25 °C	R_{PD}	14	20	26	kΩ
V_{STBY} = H, V_{IN} = L	T_j = -40 °C ...150°C		10		40	
Output leakage current	V_{STBY} = L	I_{Dlk}			20	µA
Output on delay time [2]	I_D = 1 A	t_{on}			65	µs
Output off delay time [2]	I_D = 1 A	t_{off}	10		80	
Output on fall time [2]	I_D = 1 A	t_{fall}	5		40	
Output off rise time [2]	I_D = 1 A	t_{rise}	5		40	
Output off status delay time [2]	I_D = 1 A	t_4	10		60	
Output on status delay time [3]		t_5			50	
Overload switch-off delay time		t_{DSO}	50	100	300	
3. Digital Inputs (IN1, IN2, IN3, IN4, ENA)						
Input low voltage		V_{INL}	- 0.3		1.0	V
Input high voltage		V_{INH}	2.0		6.0	V
Input voltage hysteresis [3]		V_{INHys}	50	100		mV
Input pull down current	V_{IN} = 5 V; $V_S \geq$ 6.5 V	I_{IN}	10	30	60	µA
Enable pull down current	V_{ENA} = 5 V; $V_S \geq$ 6.5 V	I_{ENA}	10	20	40	µA
4. Digital Status Outputs (ST1 - ST4) open Drain						
Output voltage low	I_{ST} = 2 mA	V_{STL}			0.5	V
Leakage current high		I_{STH}			10	µA

[1] Measured on P-DSO-20 devices
[2] See timing diagram, resitive load condition; $V_S \geq$ 9 V
[3] This parameter will not be tested but assured by design

Electrical Characteristics

Parameter and Conditions V_S = 4.8 to 18 V ; T_j = – 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
5. Standby Input (STBY)						
Input low voltage		V_{STBY}	0		1	V
Input high voltage		V_{STBY}	3.5		V_S	V
Input current	V_{STBY} = 18 V	I_{STBY}			300	µA
6. Diagnostic Functions						
Open load detection voltage V_{ENA} = X, V_{IN} = L, V_{DC} = 0 [4]	$V_S \geq$ 6.5 V	$V_{DS(OL)}$	0.52*V_S		0.57*V_S	V
Open load compare voltage V_{ENA} = X, V_{IN} = L, 18V ≥ V_{DSC} ≥ $V_{DS(OL)}$ [4]	$V_S \geq$ 6.5 V	$V_{DS(OL)C}$	V_{DSC}-1.5		V_{DSC}-1.0	V
Open load detection current channel 1,2 V_{ENA} = X, V_{IN} = H	$V_S \geq$ 6.5 V	$I_{D(OL)\ 1,2}$	160		480	mA
Open load detection current channel 3,4 V_{ENA} = X, V_{IN} = H	$V_S \geq$ 6.5 V	$I_{D(OL)\ 3,4}$	160		480	mA
Overload threshold current channel 1,2	$V_S \geq$ 6.5 V	$I_{D(lim)\ 1,2}$	5	7.5		A
Overload threshold current channel 3,4	$V_S \geq$ 6.5 V	$I_{D(lim)\ 3,4}$	3	5		A
Overtemperature shutdown threshold [5]		T_{th}	170		200	°C
Hysteresis		T_{hys}		10		K

Table 1:

Channel	Compared with Channel
$V_{DS(OL)}$ 1	4
$V_{DS(OL)}$ 2	3
$V_{DS(OL)}$ 3	2
$V_{DS(OL)}$ 4	1

[4] V_{DSC} is the output voltage of the corresponding channel, paired for open load detection Corresponding outputs are channel 1 and 4, channel 2 and 3 (see table 1).

[5] This parameter will not be tested but assured by design

Application Description

This IC is especially designed to drive inductive loads (relays, electromagnetic valves).
Integrated clamp-diodes limit the output voltage when inductive loads are discharged.

Four open-drain logic outputs indicate the status of the integrated ciruit. The following conditions are monitored and signalled:

- overloading of output (also shorted load to supply) in active mode
- open and shorted load to ground in active and inactive mode
- overtemperature

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Not connected inputs are interpreted as LOW.

In standby mode (STBY = LOW) the current consumption is greatly reduced. The circuit is active when STBY = HIGH.
If the standby function is not used, it is allowed to connect the standby pin directly to V_S.

Switching Stages

The four power outputs consist of DMOS-power transistors with open drains. The output stages are shorted loads protected throughout the operating range. Integrated clamp-diodes limit voltage overshoots produced when inductive loads are demagnetized.
Parallel to the DMOS transistors there are internal pull down resistors. They are provided to detect an open load condition in the off state. They will be disconnected in the standby mode.

Protective Circuits

The outputs are protected against current overload and overtemperature.
There is no protection against reverse polarity of the supply voltage.

Error Detection

The status outputs indicate the switching state under normal conditions (LOW = off; HIGH = on). If an error occurs, the logic level of the status output is inverted, as listed in the diagnostic table below.
The state of the error detection circuits is directly dependent on the input status.

If current overload or overtemperature occurs, the error condition is stored into an internal register and the output is shutdown. The reset is done by switching off the corresponding control input.

Open load is detected for all four channels in on and off mode. In the on mode the load current is monitored. If it drops below the specified threshold value, then an open load condition is detected.
In the off mode, the ouput voltage is monitored.

An open load condition is detected when the output voltage of a given channel is below 55 % of the supply voltage Vs. Also the output voltages of two outputs are compaired against each other in off condition with a fixed offset of typ. 1.25 V to recognize GND bypasses. To suppress fault diagnosis during the flyback phase of the compared output, the diagnostic circuit includes a latch function.

Reset of this latch is done at end of the flyback phase, additionally it can be reseted by a low signal on the enable input or a high signal of the input line.

See block diagramm of open load detection on page 3.

Diagnostic Table

In general the status follows the input signal in normal operating conditions.

If any error is detected the status is inverted.

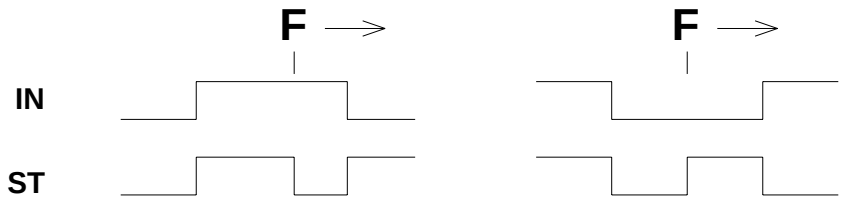
Operating Condition	Standby Input	Enable Input	Control Input	Power Output	Status Output
	STBY	**ENA**	**IN**	**OUT**	**ST**
Standby	L	X	X	OFF	H
Normal function	H	L	L	OFF	L
	H	L	H	OFF	L
	H	H	L	OFF	L
	H	H	H	ON	H
Open load or short to ground	H	L	L	OFF	H
	H	L	H	OFF	H
	H	H	L	OFF	H
	H	H	H	ON	L
Overload or short to supply	H	H	H	OFF	L
latched overload	H	H	H	OFF	L
	H	L	H	OFF	H
reset latch	H	X	H $\rightarrow$ L	OFF	L
Overtemperature	H	H	H	OFF	L
latched overtemperature	H	H	H	OFF	L
	H	L	H	OFF	H
reset latch	H	X	H $\rightarrow$ L	OFF	L

Diagnostic (continued)

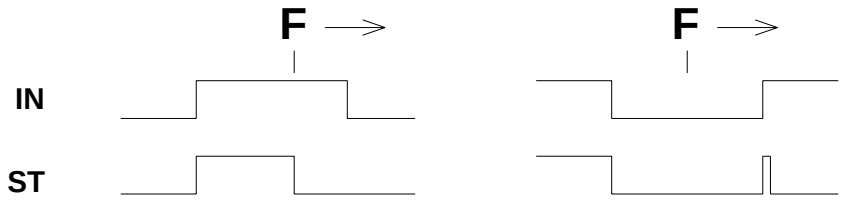
The following diagrams show the dynamical behaviour of the status output in case of different errors.

The symbol **F** defines the moment of failure occurence.

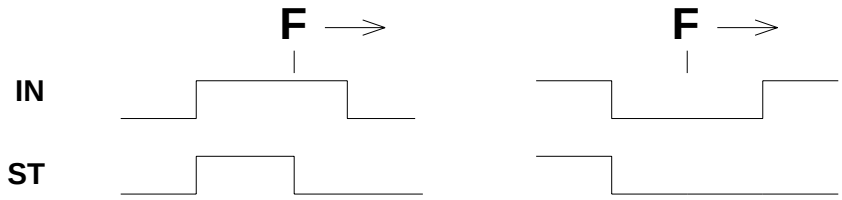
Output open load or short circuit to GND



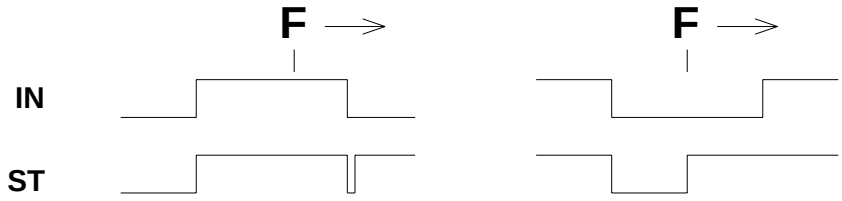
Output overload



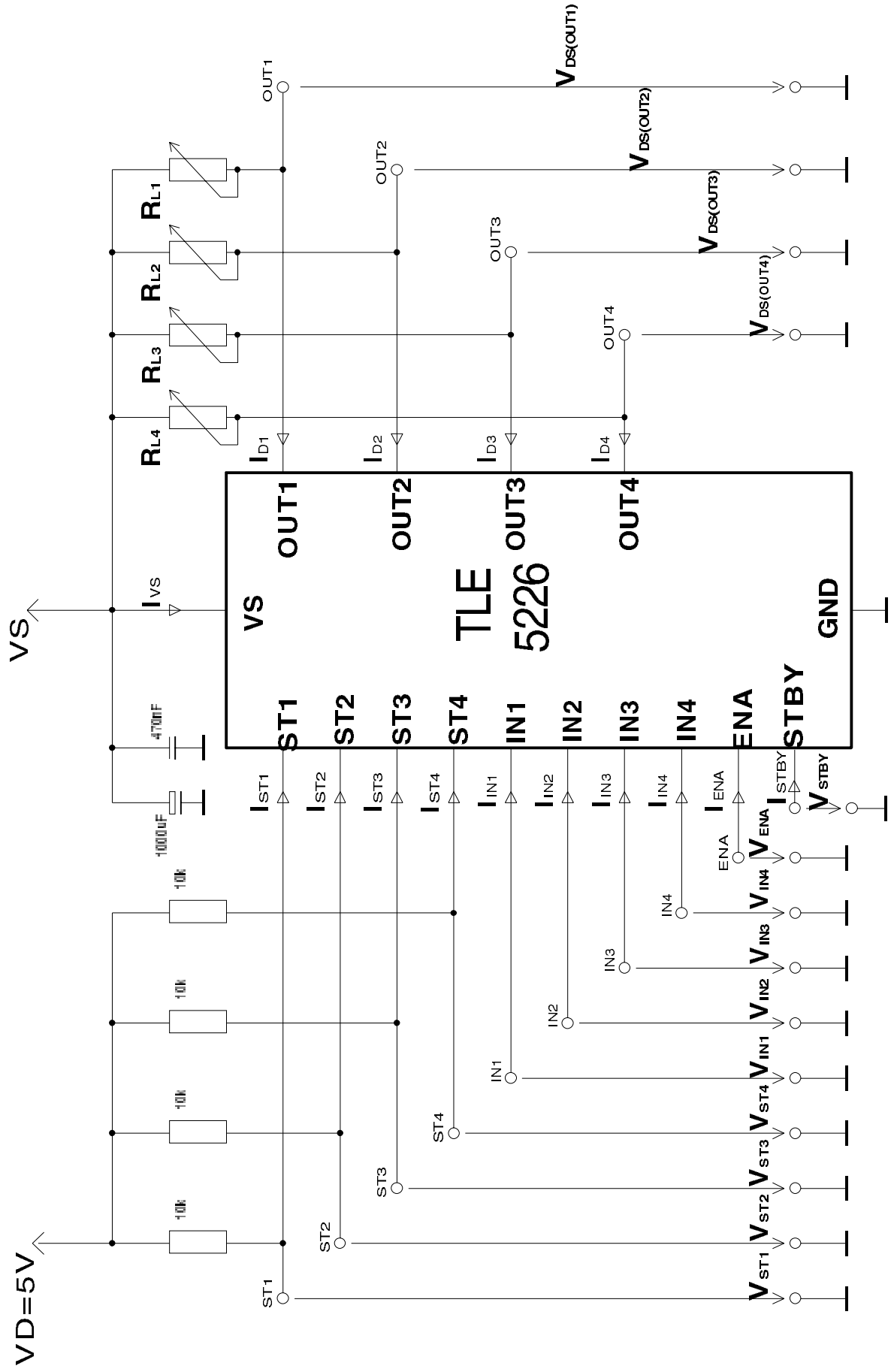
Overtemperature of the chip



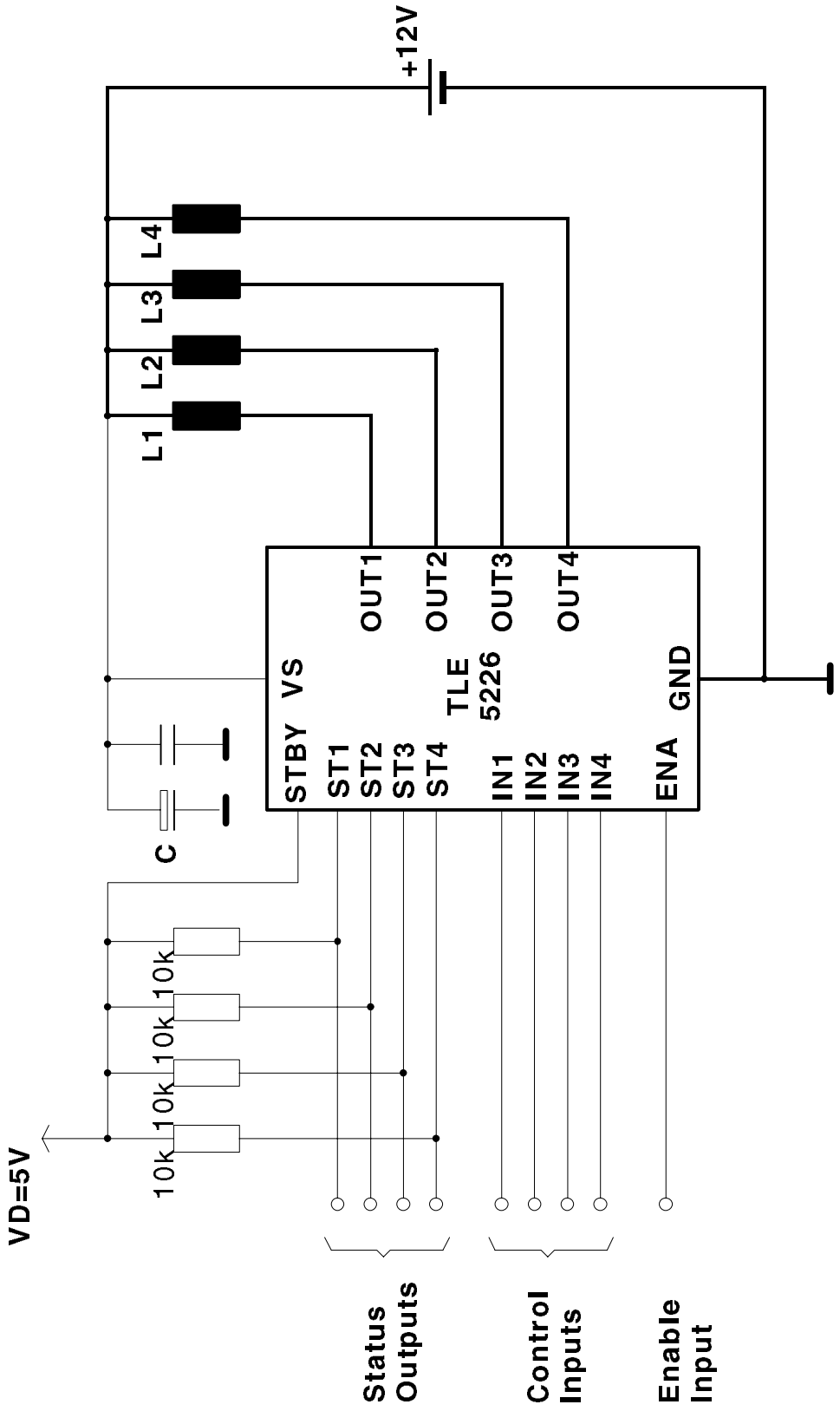
Load Bypass



Test Ciruit


OUT1
OUT2
OUT3
OUT4
VDS(OUT1)
VDS(OUT2)
VDS(OUT3)
VDS(OUT4)
RL1
RL2
RL3
RL4
ID1
ID2
ID3
ID4
TLE 5226
VS
GND
ST1
ST2
ST3
ST4
IN1
IN2
IN3
IN4
ENA
STBY
IVS
ISTBY
VSTBY
VENA
VIN4
VIN3
VIN2
VIN1
VST4
VST3
VST2
VST1
470nF
1000uF
10k
VD=5V

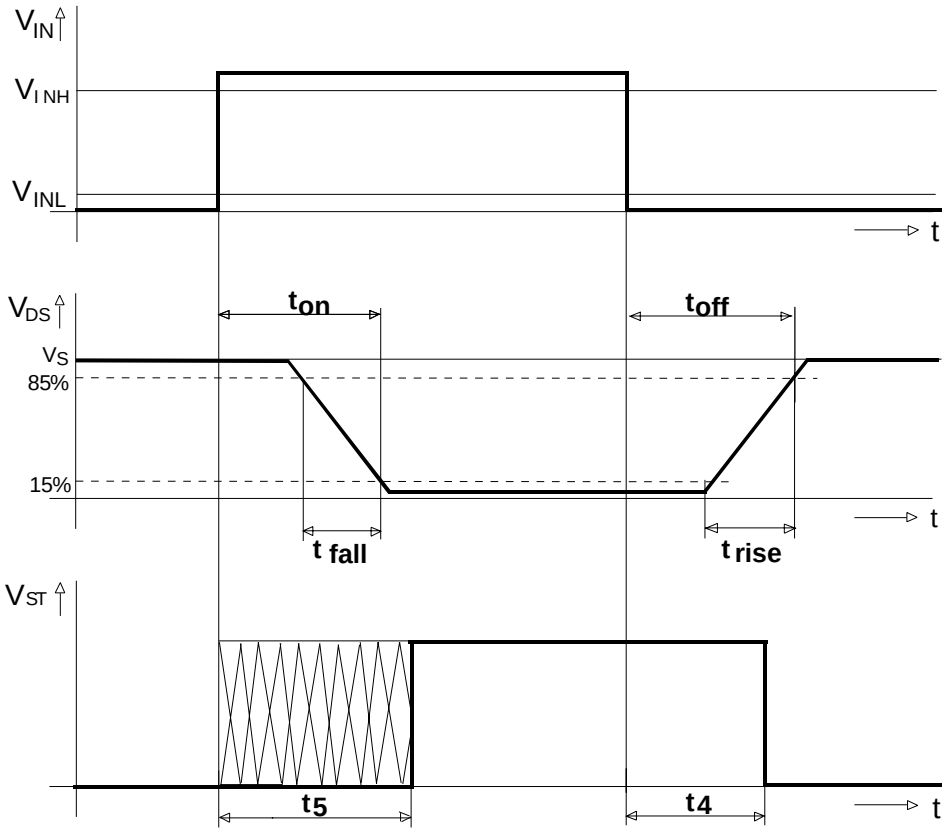
Application Circuit



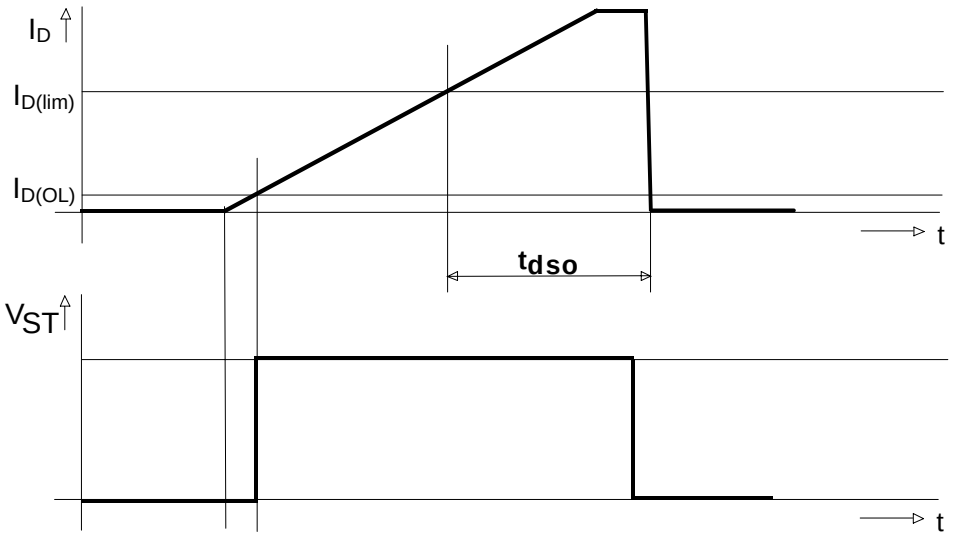
The blocking capacitor C is recommended to avoid critical negative voltage spikes on VS in case of battery interruption during OFF-commutation.

Timing Diagrams

Output Slope



Overload Switch OFF Delay



Package and ordering code

all dimensions in mm

P - DSO - 20 - 10	Ordering code
	Q67006-A9207