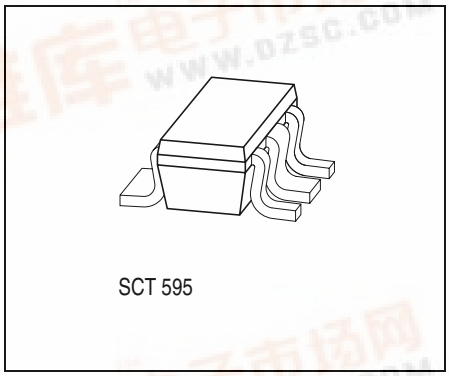
Low-Drop Voltage Regulator TLE 4295

Data Sheet

Features



- Three versions: 3.0 V, 3.3 V, 5.0 V
- Output voltage tolerance ≤ ± 4%
- Very low drop voltage
- Output current: 30 mA
- Power fail output
- Low quiescent current consumption
- Wide operation range: up to 45 V
- Wide temperature range: – 40 °C ≤ T_j ≤ 150 °C
- Output protected against short circuit
- Overtemperature protection
- Reverse polarity proof
- Very small SMD-Package SCT-595

Type	Ordering Code	Package
▼ TLE 4295G V30	Q67006-A9410	SCT-595 (SMD)
▼ TLE 4295G V33	Q67006-A9409	SCT-595 (SMD)
▼ TLE 4295G V50	Q67006-A9395	SCT-595 (SMD)

▼ New type

Functional Description

The **TLE 4295 G** is a monolithic integrated low-drop voltage regulator in the very small SMD package SCT-595. It is designed to supply e.g. microprocessor systems under the severe conditions of automotive applications. Therefore the device is equipped with additional protection functions against over load, short circuit and reverse polarity. At overtemperature the regulator is automatically turned off by the integrated thermal protection circuit.

Input voltages up to 40 V are regulated to $V_{Q,nom}$ = 3.0 V (V30 version) 3.3 V (V33 version) or 5.0 V (V50 version). The output is able to drive a load of more than 30 mA while it regulates the output voltage within a 4% accuracy.

The power fail output (open collector) is switched to low in case of undervoltage overload or saturation of the output transistor.

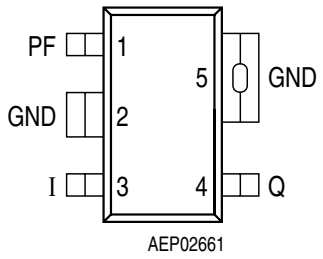


Figure 1 **Pin Configuration** (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	PF	**Power Fail;** L for under-voltage
2	GND	**Ground**; connected to pin 5
3	I	**Input voltage**
4	Q	**Output voltage**; must be blocked by a capacitor $C_Q \geq 2.2\ \mu F$, ESR $\leq 5\ \Omega$ to GND
5	GND	**Ground**; connected to pin 2

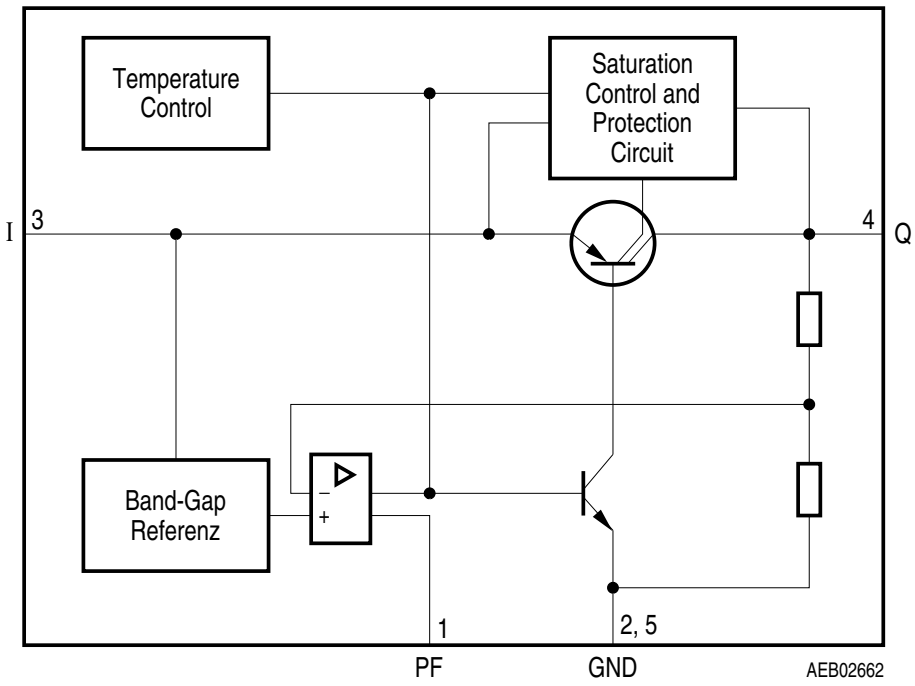


Figure 2 Block Diagram

Absolute Maximum Ratings

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input					
Voltage	V_I	– 42	45	V	–
Current	I_I	–	–	mA	internally limited
Output					
Voltage	V_Q	– 6	30	V	–
Current	I_Q	–	–	mA	internally limited
Power Fail					
Voltage	V_{PF}	– 0.3	45	V	–
Current	I_{PF}	– 500	*	µA	* internally limited
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistances					
Junction pin	$R_{thj\text{-}pin}$	–	30	K/W	measured to pin 5
Junction ambient[1)]	R_{thja}	–	179	K/W	zero airflow zero heat sink area

1) Worst case regarding peak temperature.

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input voltage	V_I	$V_{Q,nom}$ + 0.5 V	45	V	–
Output current	I_Q	–	–	mA	internally limited
Junction temperature	T_j	– 40	150	°C	–

Electrical Characteristics

V_I = 13.5 V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output						
Output voltage V30 version	V_Q	2.88	3.0	3.12	V	1 mA < I_Q < 30 mA V_I = 13.5 V
Output voltage V30 version	V_Q	2.88	3.0	3.12	V	I_Q = 10 mA 4 V < V_I < 40 V
Output voltage V33 version	V_Q	3.17	3.30	3.43	V	1 mA < I_Q < 30 mA V_I = 13.5 V
Output voltage V33 version	V_Q	3.17	3.30	3.43	V	I_Q = 10 mA 4.3 V < V_I < 40 V
Output voltage V50 version	V_Q	4.80	5.00	5.20	V	1 mA < I_Q < 30 mA V_I = 13.5 V
Output voltage V50 version	V_Q	4.80	5.00	5.20	V	I_Q = 10 mA 6 V < V_I < 40 V
Output current limitation	I_Q	30	–	–	mA	1)
Drop voltage	V_{dr}	–	0.25	0.40	V	I_Q = 20 mA 1)
Output capacitor	C_Q	2.2	–	–	µF	ESR ≤ 5 Ω at 10 kHz
Current Consumption						
Current consumption $I_q = I_I - I_Q$	I_q	–	2	4	mA	I_Q < 30 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	120	200	µA	I_Q < 1 mA

Electrical Characteristics (cont'd)

V_I = 13.5 V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Regulator Performance						
Load regulation	$\|\Delta V_Q\|$	–	10	25	mV	1 mA < I_Q < 25 mA; T_j = 25 °C
Load regulation	$\|\Delta V_Q\|$	–	10	30	mV	1 mA < I_Q < 25 mA
Line regulation	$\|\Delta V_Q\|$	–	5	25	mV	ΔV_I = $V_{Q,nom}$ + 0.5 V to 36 V; I_Q = 5 mA; T_j = 25 °C
Line regulation	$\|\Delta V_Q\|$	–	10	30	mV	ΔV_I = $V_{Q,nom}$+ 0.5 V to 36 V; I_Q = 5 mA
Power-Supply-Ripple-Rejection	PSRR	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 V_{SS}
Power Fail Output						
Power fail threshold	V_{QPF}	–	4.86	–	V	TLE 4295GV50
		–	3.20	–	V	TLE 4295GV33
		–	2.91	–	V	TLE 4295GV30
Power Fail Headroom	V_{Qnom}-V_{QPF}	50	140	300	mV	TLE 4295GV50
		33	100	200	mV	TLE 4295GV33
		30	90	180	mV	TLE 4295GV30
Power fail low voltage	V_{PFL}	–	150	300	mV	I_{PF} = 0.1 mA
Pull up resistor	R_{PF}	70	100	130	kΩ	internal connected to V_Q

[1] Measured when the output voltage V_Q has dropped 100 mV from the nominal value.

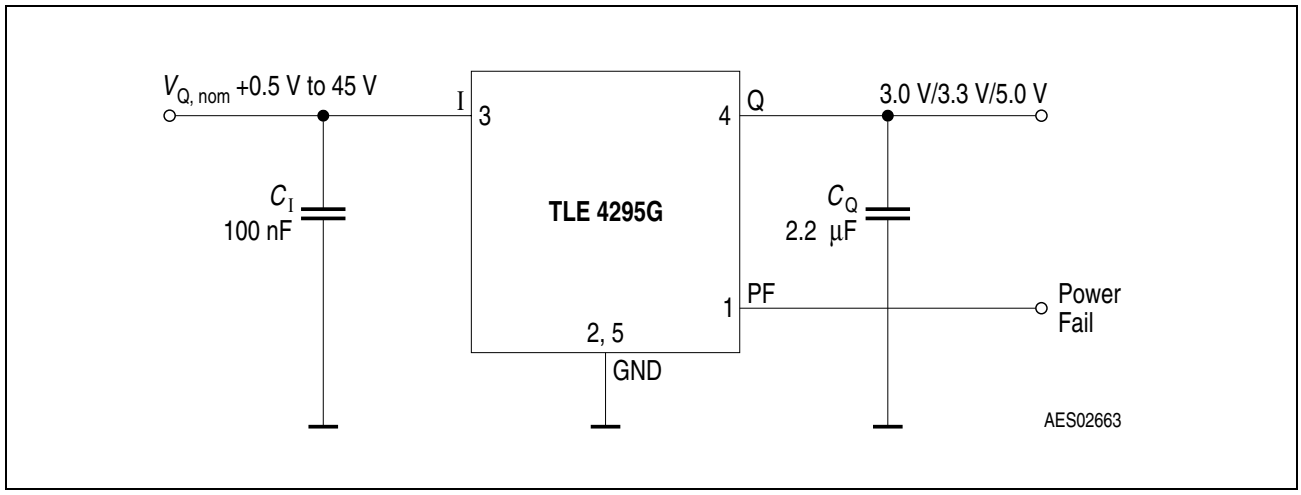
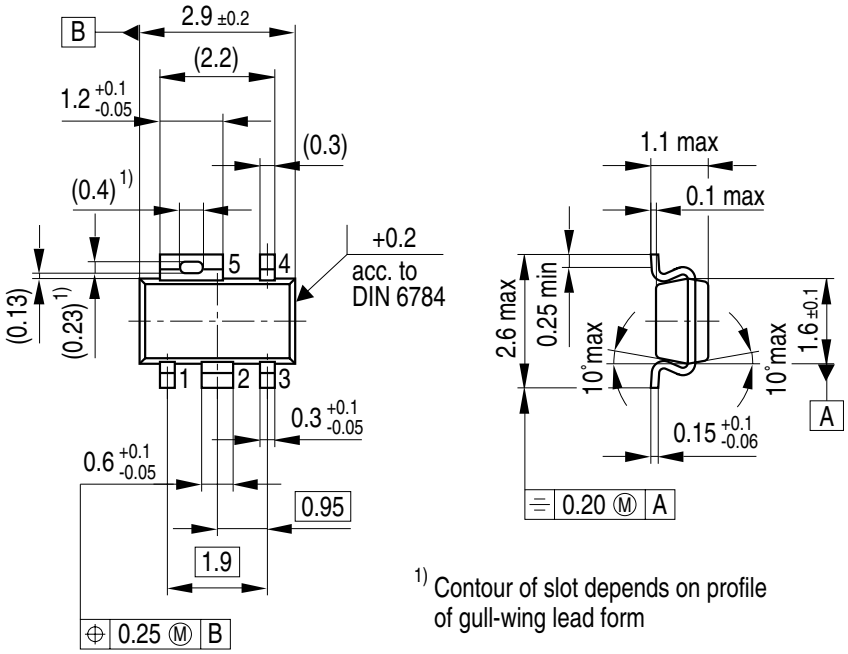


Figure 3 Application Circuit

Package Outlines

SCT-595
(Plastic Dual Small Outline)



1) Contour of slot depends on profile of gull-wing lead form

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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