DATA SHEET

PCA9513; PCA9514

Hot swappable I^2C and SMBus bus buffer

Product data sheet
Supersedes data of 2004 Jan 07

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Philips Semiconductors

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Hot swappable I²C and SMBus bus buffer PCA9513; PCA9514

DESCRIPTION

The PCA9513 and PCA9514 are hot swappable I²C and SMBus buffers that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511, PCA9513, and PCA9514 provides bi-directional buffering, keeping the backplane and card capacitances isolated.

Rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9513 and PCA9514 incorporate a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

The PCA9513 supplies a 92 μA current source to SCLIN and SDAIN in lieu of using pull-up resistors for PICMG backplane applications. Including the current source in the device provides for a consistent RC time constant as cards are removed and inserted into the backplane. The current source is high-impedance whenever the pin voltage is greater than the part V_{CC}.

PCA9513 and PCA9514 rise time accelerator threshold is 0.8 V to provide improved noise margin over the PCA9510 and PCA9511.

The dynamic offset design of the PCA9510/11/12/13/14 I/O drivers allow them to be connected to another PCA9510/11/12/13/14 device in series or in parallel and to the A side of the PCA9517. The PCA9510/11/12/13/14 can **not** connect to the static offset I/Os used on the PCA9515/15A/16/16A/17 B side and PCA9518.

APPLICATION

- cPCI, VME, AdvancedTCA cards and other multi-point backplane cards that are required to be inserted or removed from an operating system.

FEATURES

- Bi-directional buffer for SDA and SCL lines increases fanout and prevents SDA and SCL corruption during live board insertion and removal from multi-point backplane systems
- Compatible with I²C standard mode, I²C fast mode, and SMBus standards
- ΔV/Δt rise time accelerators on all SDA and SCL lines
- Rise time accelerator threshold moved from 0.6 V to 0.8 V for improved noise margin
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for V_{CC} = 0 V
- 92 μA current source on SCLIN and SDAIN for PICMG backplane applications (PCA9513 only)
- Supports clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 5.5 V tolerant I/Os
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic SO	–40 °C to +85 °C	PCA9513D	PCA9513	SOT96-1
8-pin plastic SO	–40 °C to +85 °C	PCA9514D	PCA9514	SOT96-1
8-pin plastic TSSOP (MSOP)	–40 °C to +85 °C	PCA9513DP	9513	SOT505-1
8-pin plastic TSSOP (MSOP)	–40 °C to +85 °C	PCA9514DP	9514	SOT505-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION

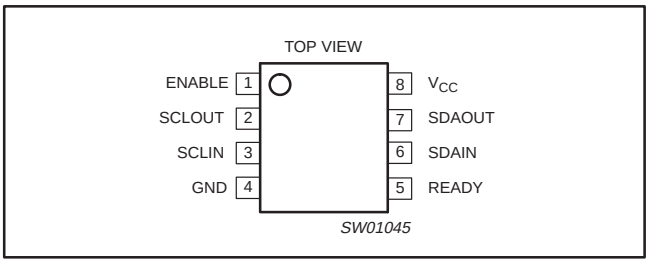


Figure 1. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	ENABLE	Chip enable pin. Grounding this pin puts the part in a low current (< 1 μA) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	READY	This is an open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and turns off when the two sides are connected.
6	SDAIN	Serial data input to and from the SDA bus on the backplane.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply.

FEATURE SELECTION CHART

FEATURES	PCA9510	PCA9511	PCA9512	PCA9513	PCA9514
Idle detect	Yes	Yes	Yes	Yes	Yes
high-impedance SDA, SCL pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
Rise time accelerator circuitry on all SDA and SCL lines	—	Yes	Yes	Yes	Yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	—	—	Yes	—	—
Rise time accelerator threshold 0.8 V vs 0.6 V improves noise margin	—	—	—	Yes	Yes
Ready open drain output	Yes	Yes	—	Yes	Yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	—	—	Yes	—	—
1 V precharge on all SDA and SCL lines	IN only	Yes	Yes	—	—
92 μA current source on SCLIN and SDAIN for PICMG applications	—	—	—	Yes	—

TYPICAL APPLICATION — PCA9513

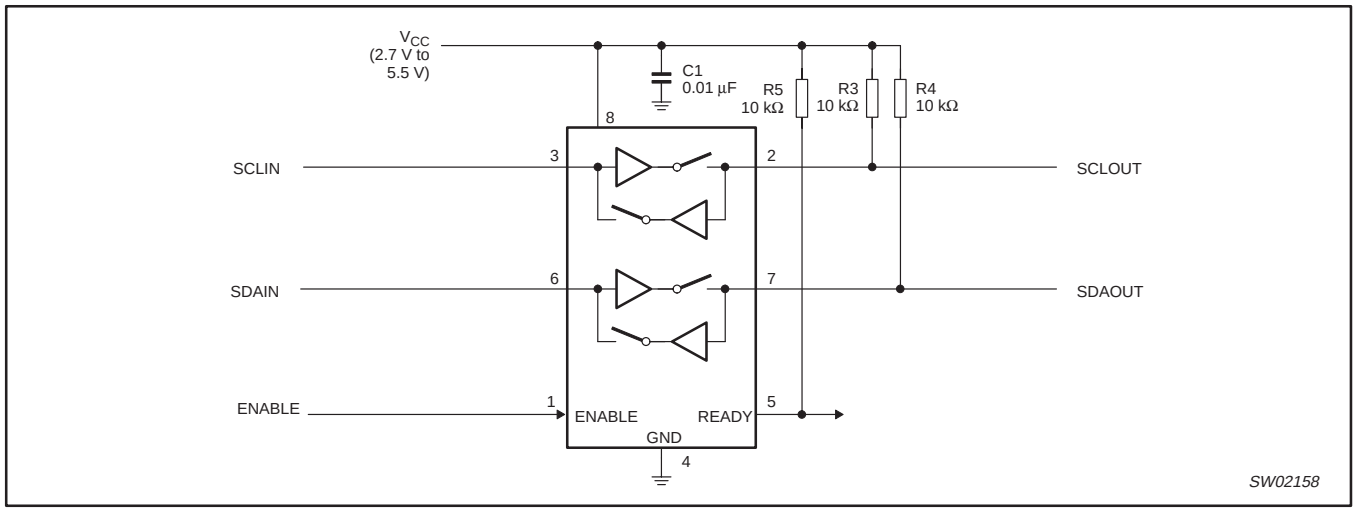


Figure 2. Typical application — PCA9513

BLOCK DIAGRAM — PCA9513

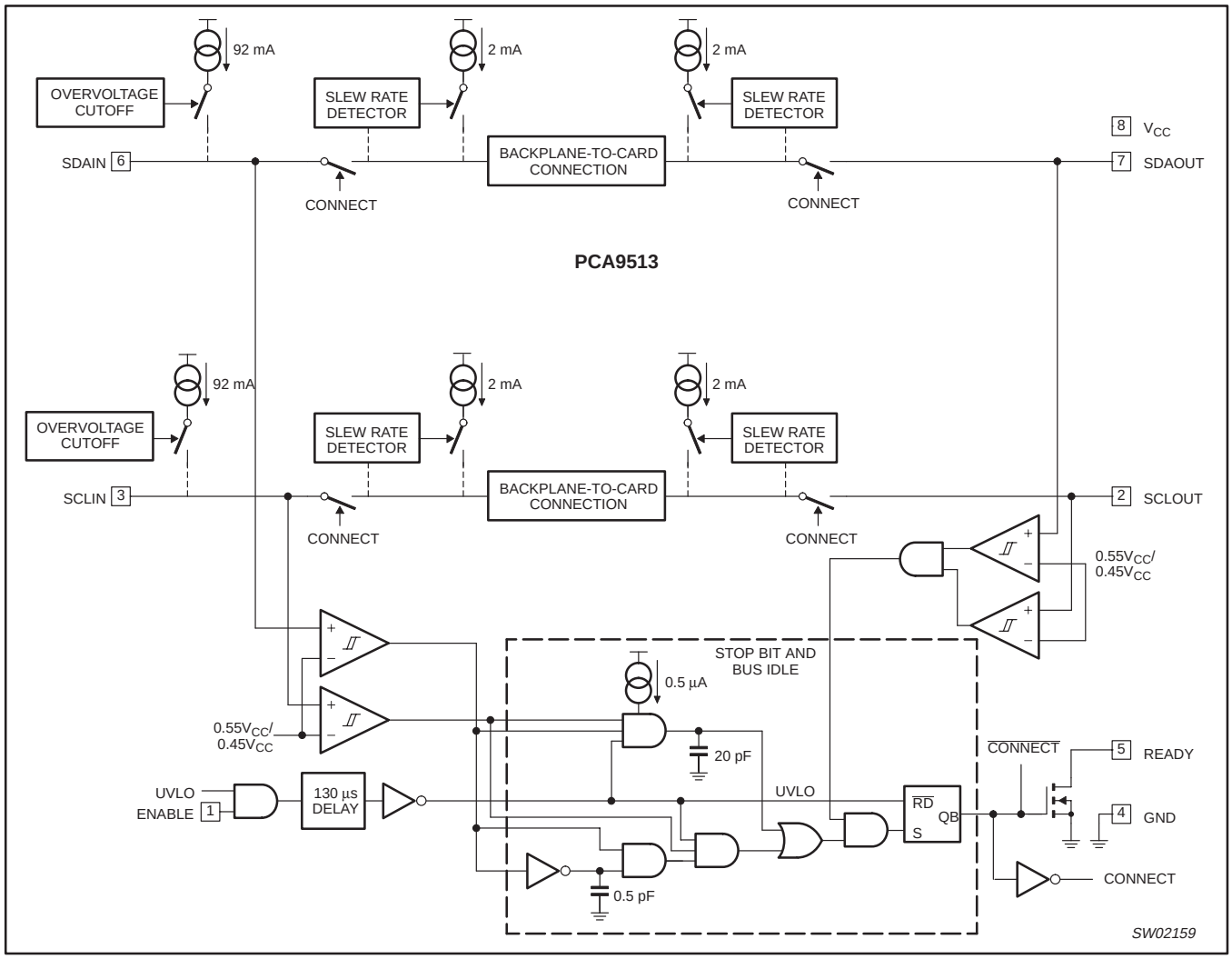


Figure 3. Block diagram — PCA9513

TYPICAL APPLICATION — PCA9514

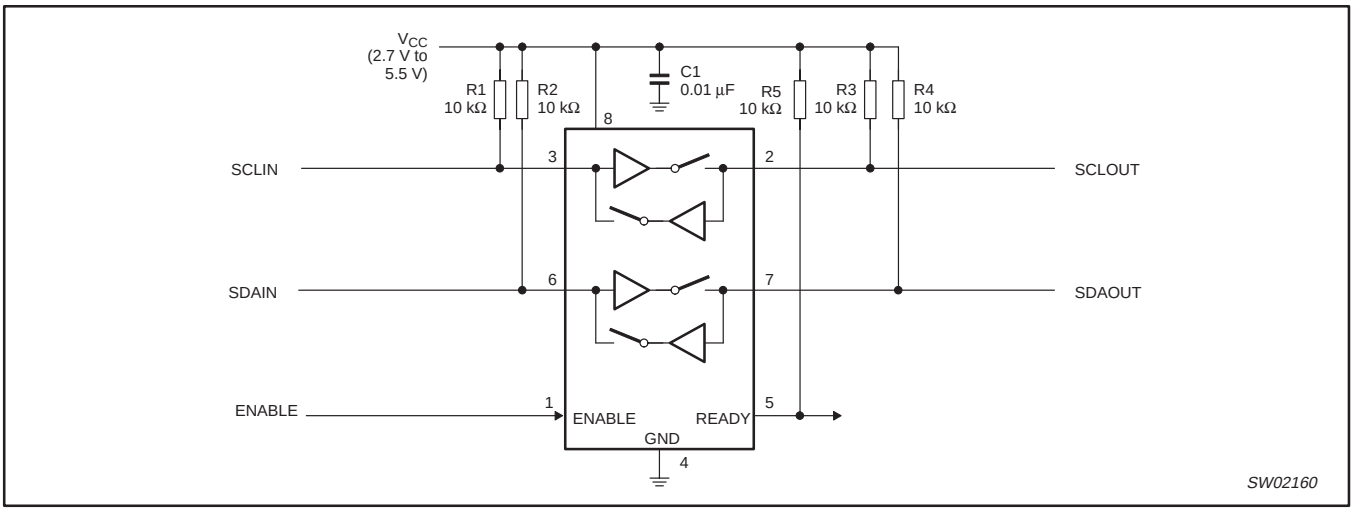


Figure 4. Typical application — PCA9514

BLOCK DIAGRAM — PCA9514

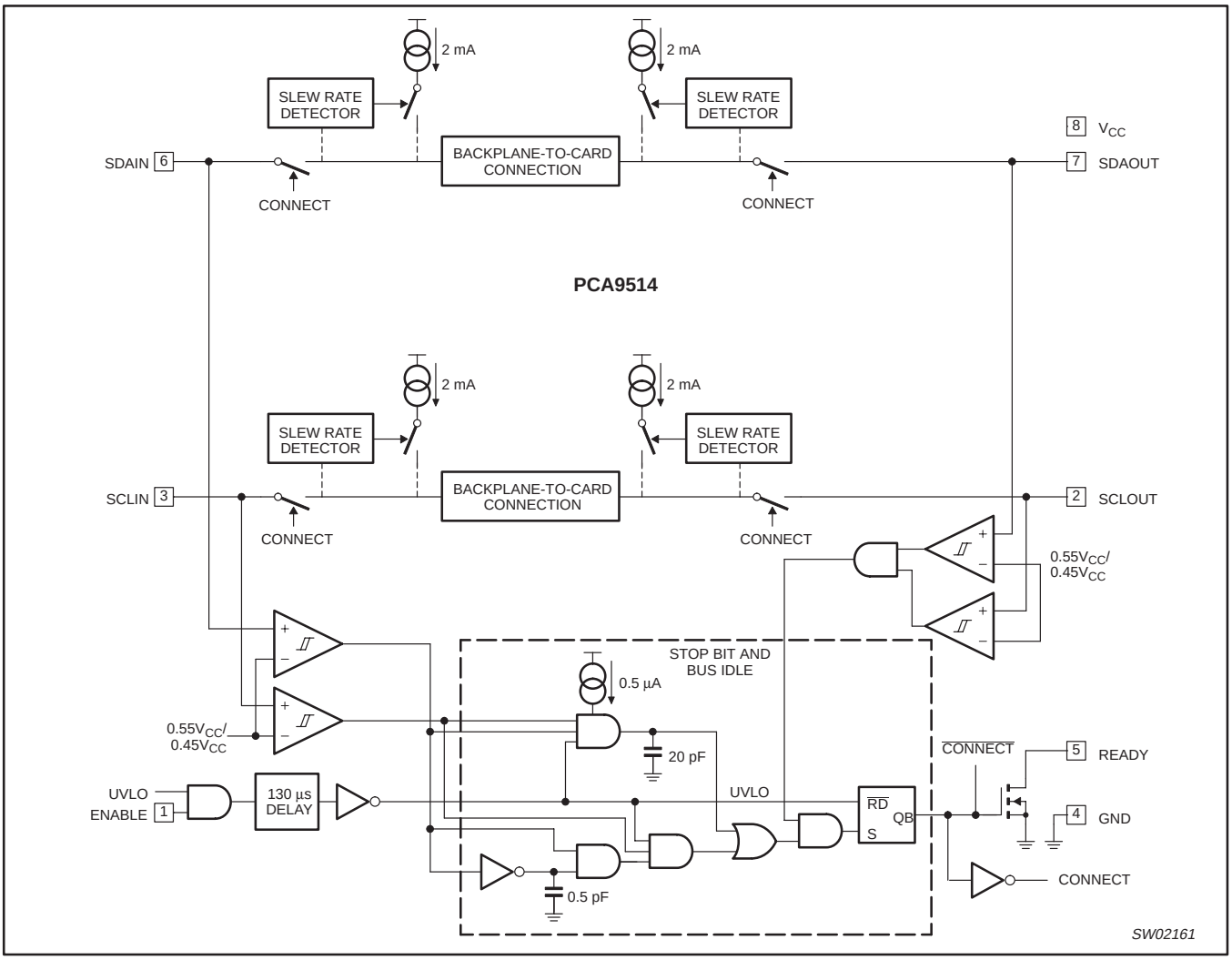


Figure 5. Block diagram — PCA9514

OPERATION

Start-up

An under voltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the enable pin also forces the parts into the low current disconnected state when the I_{CC} is essentially zero. As the power supply is brought up and the enable is HIGH or the part is powered and the enable is taken from LOW to HIGH it enters an initialization state where the internal references are stabilized. The 92 µA input pull-ups on PCA9513 are also enabled in the initialization state. At the end of the initialization state the “Stop Bit And Bus Idle” detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state and remaining HIGH when all the SDA and SCl pins have been HIGH for the bus idle time or when all pins are HIGH and a stop condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT.

A 92 µA pull-up current source on SDAIN and SCLIN of PCA9513 is activated during the initialization state and remain active until the power is removed or the enable is taken LOW. When the 92 µA pull-up is active it will become high-impedance any time the pin voltage is greater than V_{CC}, otherwise it provides current to pull the pin up to V_{CC}.

Connect Circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between $0.7V_{CC}$ and V_{CC} is generally ignored because a falling edge is only recognized when it falls below $0.7V_{CC}$ with a slew rate of at least 1.25 V/µs. When a falling edge is seen on one pin the other pin in the pair turns on a pull down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below $0.7V_{CC}$. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage the they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise and rise above the nominal offset voltage until the internal driver catches up and pulls it back down to the offset voltage. This bounce is worst for low capacitances and low resistances, and may become excessive. When the last external driver stops driving a LOW, that pin will bounce up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/µs, when the pin voltage exceeds 0.8 V for PCA9513 and PCA9514, rise time accelerators circuits are turned on and the pull down driver is turned off.

Maximum number of devices in series

Each buffer adds about 0.065 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{OS}) is 0.150 V. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I²C-bus specification of 3 mA will produce V_{OL} < 0.4 V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming V_{OL} = 0.1 V and V_{OS} = 0.1 V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two.

The PCA9510 (rise time accelerator is permanently disabled) and the PCA9512 (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull-down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected; so if the noise is small enough it may be possible to use more than two PCA9510 or PCA9512 parts in series but is not recommended.

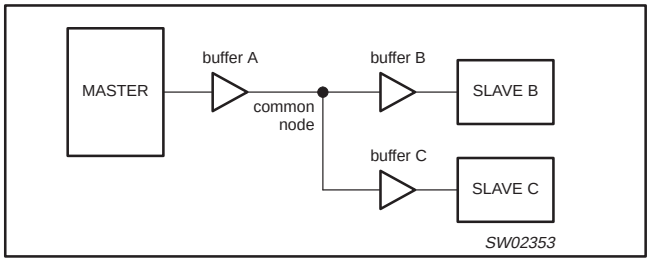


Figure 6.

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of Buffer A and Buffer B in series as shown in Figure 6. Consider if the V_{OL} at the input of Buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of Buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of Buffer B and Buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of Buffer C is ~0.5 V. When the Master pull-down turns off, the input of Buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before Buffer B’s output turns on, if the pull-up is strong the node will bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both Buffer A and Buffer C will fire contending with the output of Buffer B. The node on the input of Buffer A will go HIGH as will the input node of Buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the Buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on Buffer A and Buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Propagation Delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$, and the output turn on has a non zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, V_{CC}, and process, as well as the load current and the load capacitance.

Rise Time Accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.8 V for the PCA9513 and PCA9514 are exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators. The 0.8 V threshold of PCA9513 and PCA9514 allows for larger bounce-or-noise without falsely triggering the rise time accelerators.

READY Digital Output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to V_{CC} to provide the pull-up.

ENABLE Low Current Disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a LOW current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

Resistor Pull-up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula:

$$R \leq 800 \cdot 10^3 \times \frac{V_{CC(MIN)} - 0.6}{C}$$

where R is the pull-up resistor value in Ω, $V_{CC(MIN)}$ is the minimum V_{CC} voltage in volts and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R ≤ 16 kΩ for V_{CC} = 5.5 V maximum, R ≤ 24 kΩ for V_{CC} = 3.6 V maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage (PCA9511 only). See the curves in Figures 7 and 8 for guidance in resistor pull-up selection.

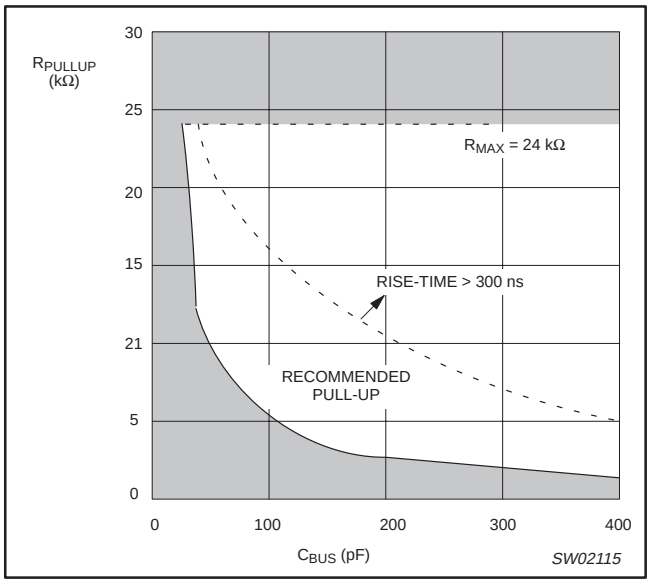


Figure 7. Bus requirements for 3.3 V systems

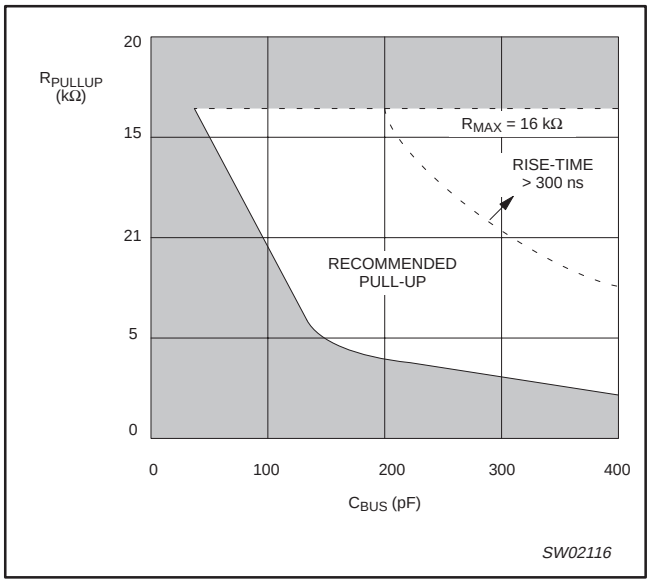


Figure 8. Bus requirements for 5 V systems

Minimum SDA and SCL Capacitance Requirements

The device connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of V_{CC} and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock buses, and refer to Figures 7 and 8 to choose appropriate pull-up resistor values. Note from the figures that 5 V systems should have at least 47 pF capacitance on their buses and 3.3 V systems should have at least 22 pF capacitance for proper operation. Although the device has been designed to be marginally stable with smaller capacitance loads, for applications with less capacitance, provisions need to be made to add a capacitor to ground to ensure these minimum capacitance conditions if oscillations are noticed during initial signal integrity verification.

Hot Swapping and Capacitance Buffering Application

Figures 9 through 12 illustrate the usage of the PCA9513 and PCA9514 in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9513 or PCA9514 drives the capacitance of everything on the card and the backplane must drive only the the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note *AN10160, Hot Swap Bus Buffer* for more information on applications and technical assistance.

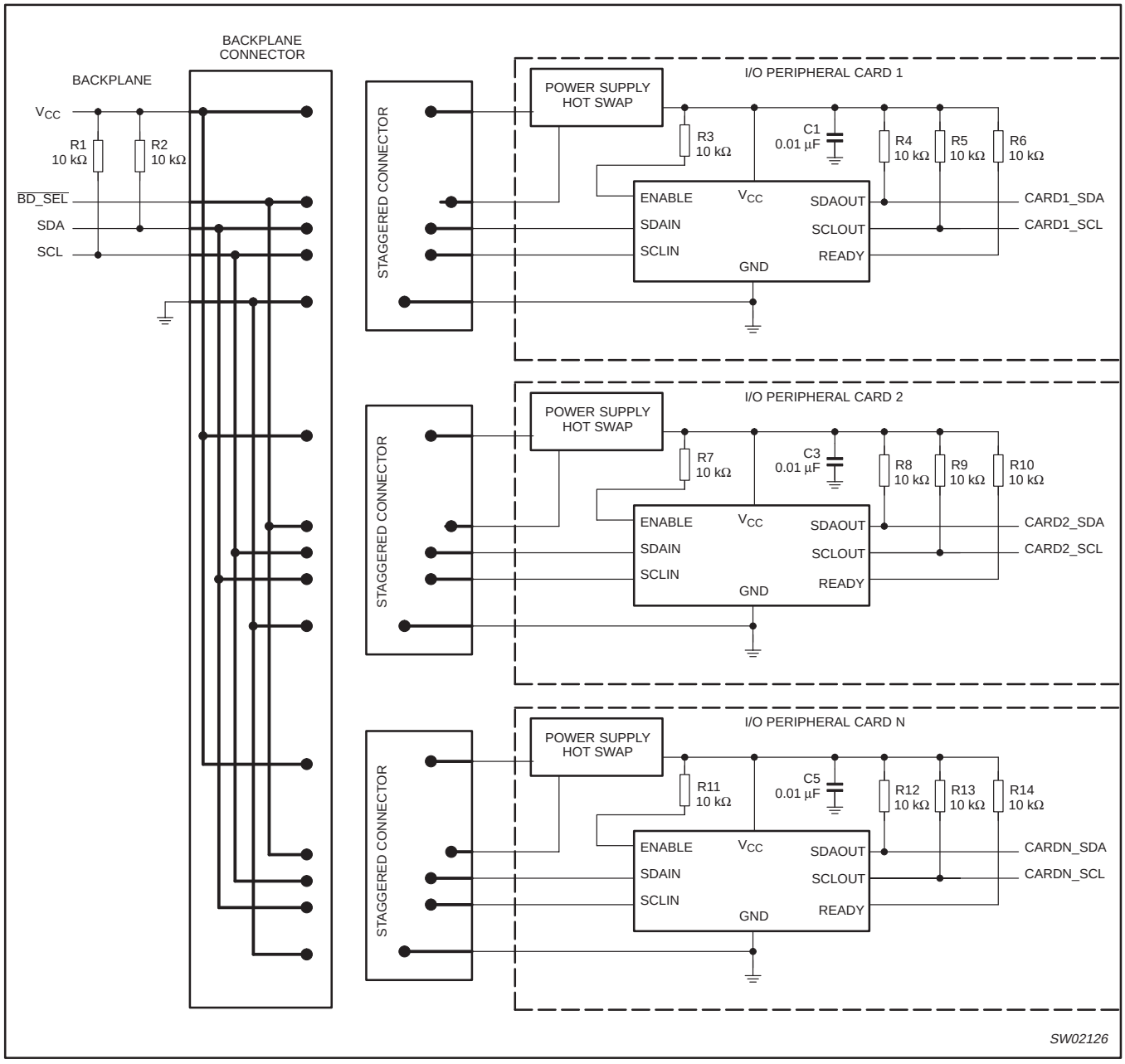


Figure 9. Hot swapping multiple I/O cards into a backplane using the PCA9514 in a CompactPCI, VME, and AdvancedTCA system

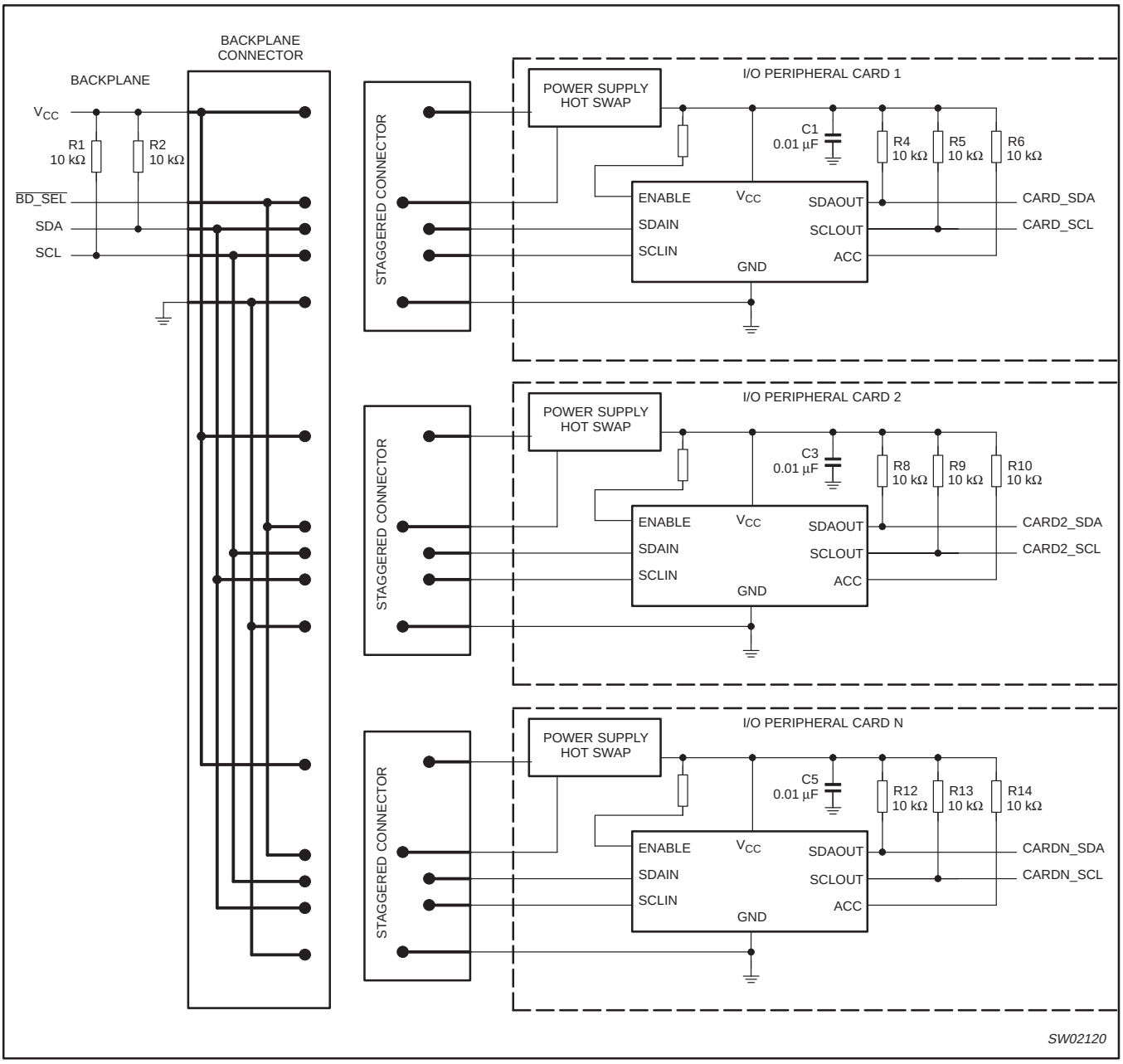


Figure 10. Hot swapping multiple I/O cards into a backplane using the PCA9513 in a CompactPCI, VME, and AdvancedTCA system

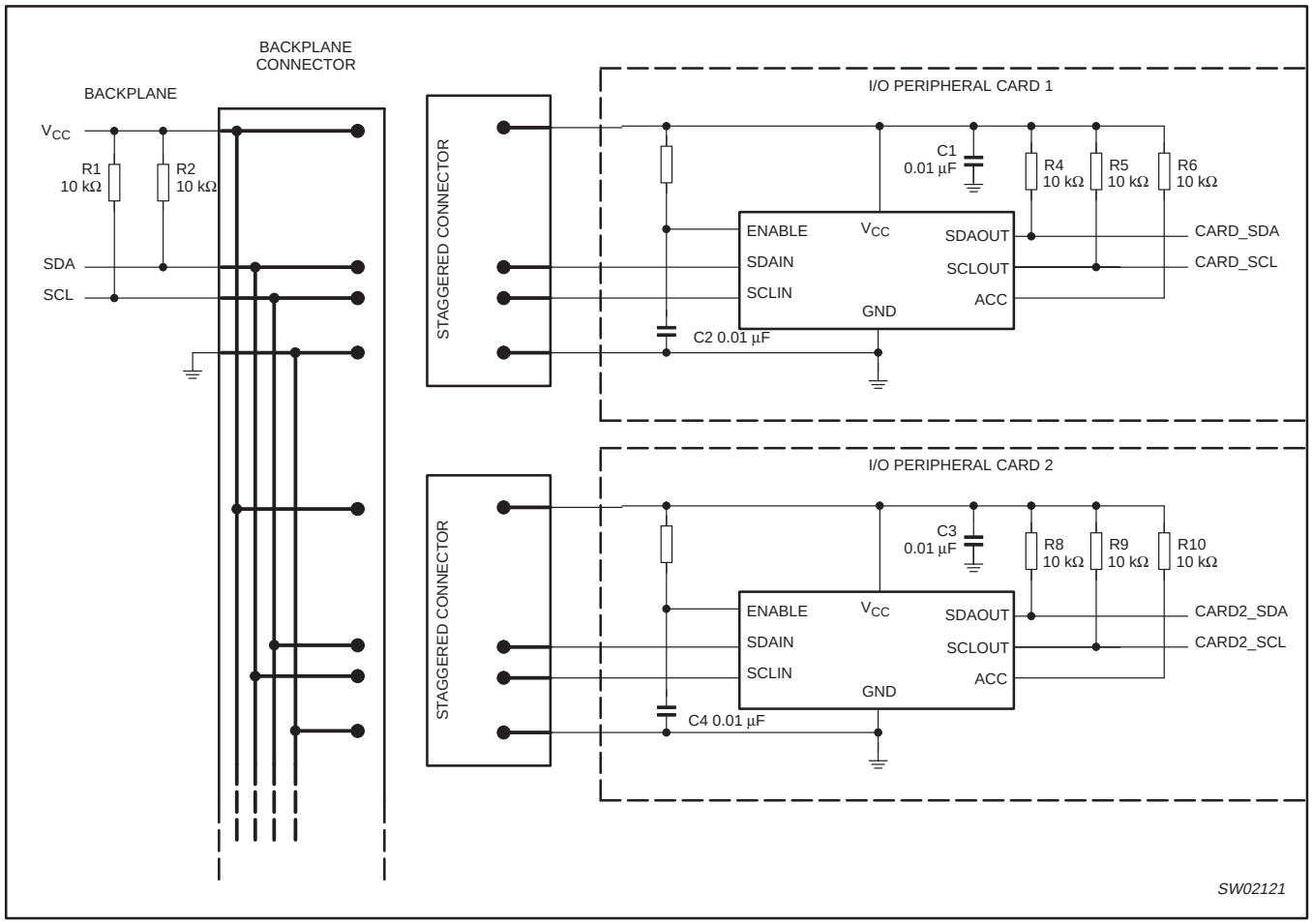


Figure 11. Hot swapping multiple I/O cards into a backplane using the PCA9514 in a PCI system

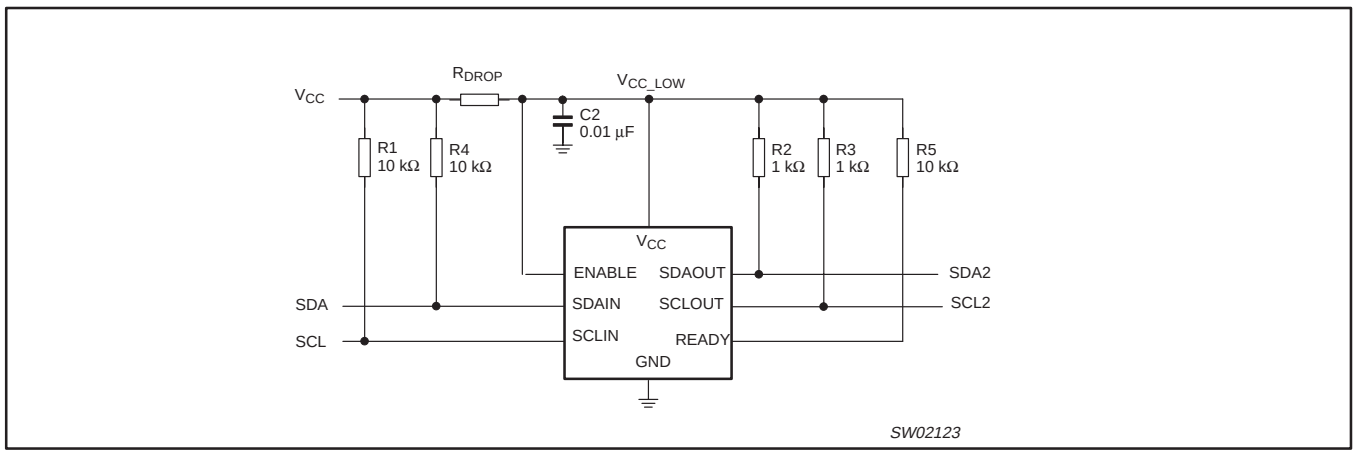


Figure 12. System with disparate V_{CC} voltages

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage range V_{CC}	–0.5	+7	V
V_n	SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE	–0.5	+7	V
I_I	Maximum current for inputs	–	±20	mA
I_{IO}	Maximum current for I/O pins	–	±50	mA
T_{opr}	Operating temperature range	–40	+85	°C
T_{stg}	Storage temperature range	–65	+125	°C
T_{sld}	Lead soldering temperature (10 sec max)	—	+300	°C
$T_{j(max)}$	Maximum junction temperature	—	+125	°C

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; T_{amb} = –40 to +85 °C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power supply						
V_{CC}	Supply voltage	Note 1	2.7	—	5.5	V
I_{CC}	Supply current	V_{CC} = 5.5 V; $V_{SDAIN} = V_{SCLIN}$ = 0 V; Note 1	—	2.8	6	mA
$I_{CC(sd)}$	Supply current in shut-down mode	V_{ENABLE} = 0 V, all other pins at V_{CC} or GND	—	200	—	µA
Start-up circuitry						
V_{EN}	Enable threshold voltage		—	$0.5 \times V_{CC}$	$0.7 \times V_{CC}$	V
V_{DIS}	Disable threshold voltage		$0.3 \times V_{CC}$	$0.5 \times V_{CC}$	—	V
I_{EN}	Enable input current	Enable from 0 V to V_{CC}	—	± 0.1	± 1	µA
t_{EN}	Enable delay or initialization time		—	130	—	µs
t_{IDLE}	Bus idle time	Note 1	50	140	250	µs
t_{DIS}	Disable time, ENABLE to Ready		—	15	—	ns
t_{STOP}	SDAIN to READY delay after STOP	Note 7	—	1.3	—	µs
t_{READY}	SCLOUT/SDAOUT to READY	Note 7	—	1.2	—	µs
I_{OFF}	Ready off state leakage current	$V_{EN} = V_{CC}$	—	± 0.3	—	µA
C_i	ENABLE capacitance	$V_I = V_{CC}$ or GND; Note 4	—	2	—	pF
C_O	Ready capacitance	$V_I = V_{CC}$ or GND; Note 4	—	2	—	pF
$V_{OL(READY)}$	LOW-level output voltage on READY pin	$I_{pull-up}$ = 3 mA; $V_{EN} = V_{CC;}$ Note 1.	—	—	0.4	V
Rise time accelerators						
$I_{PULLUPAC}$	Transient boosted pull-up current	Positive transition on SDA, SCL, V_{CC} = 2.7 V; Slew rate = 1.25 V/µs; Note 2	1	2	—	mA
Input–output connection						
V_{OS}	Input–output offset voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V; Note 1; Note 3.	0	65	150	mV
f_{SCL_SDA}	operating frequency		0	—	400	kHz
t_{PLH}	SCL to SCL and SDA to SDA	10 kΩ to V_{CC}; C_L = 100 pF each side	—	20	—	ns
t_{PHL}	SCL to SCL and SDA to SDA	10 kΩ to V_{CC}; C_L = 100 pF each side	—	380	—	ns
C_{IN}	Digital input capacitance	Note 4	—	—	10	pF
V_{OL}	LOW-level output voltage	Input = 0 V; SDA, SCL pins, I_{SINK} = 3 mA; V_{CC} = 2.7 V; Note 1	0	—	0.4	V
I_{PULLUP}	SDAIN/SCLIN pull-up current	$V_{ENABLE} = V_{CC;}$ Note 6	65	100	125	µA
I_{LI}	Input leakage current	SDA, SCL pins = V_{CC} = 5.5 V	—	—	±5	µA

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
System characteristics						
f_{I2C}	I^2C operating frequency		0	—	400	kHz
t_{BUF}	Bus free time between stop and start condition	Note 4	1.3	—	—	µs
$t_{hD,STA}$	Hold time after (repeated) start condition	Note 4	0.6	—	—	µs
$t_{su,STA}$	Repeated start condition setup time	Note 4	0.6	—	—	µs
$t_{su,STO}$	Stop condition setup time	Note 4	0.6	—	—	µs
$t_{hD,DAT}$	Data hold time	Note 4	300	—	—	ns
$t_{su,DAT}$	Data setup time	Note 4	100	—	—	ns
t_{LOW}	Clock LOW period	Note 4	1.3	—	—	µs
t_{HIGH}	Clock HIGH period	Note 4	0.6	—	—	µs
t_t	Clock, data fall time	Notes 4 and 5	$20 + 0.1 \times C_B$	—	300	ns
t_r	Clock, data rise time	Notes 4 and 5	$20 + 0.1 \times C_B$	—	300	ns

NOTES:
1. This specification applies over the full operating temperature range.
2. $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.
3. The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.
4. Guaranteed by design, not production tested.
5. C_B = total capacitance of one bus line in pF.
6. SDAIN/SCLIN = 0.1 V, SDAOUT/SCLOUT through resistor to V_{CC}.
7. Delays that can occur after ENABLE and/or idle times have passed.

TYPICAL PERFORMANCE CHARACTERISTICS

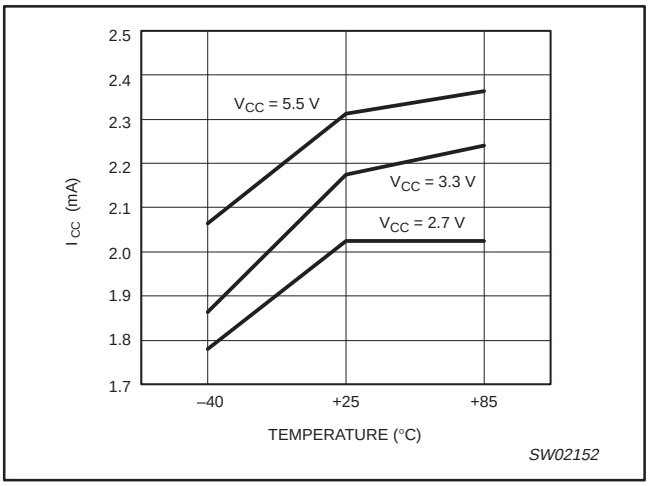


Figure 13. I_{CC} versus Temperature.

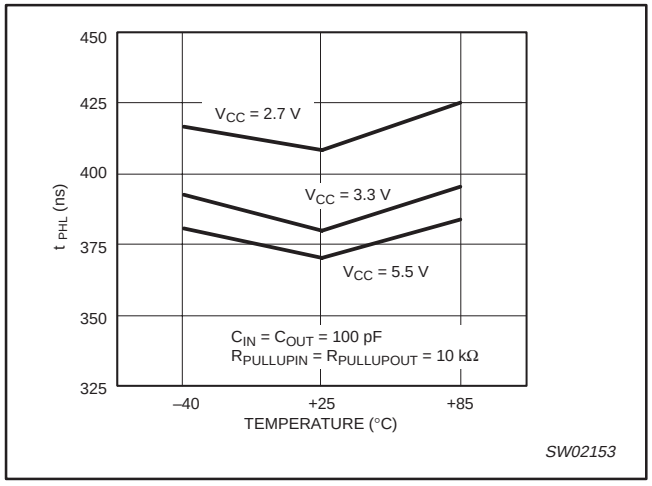


Figure 15. Input–output t_{PHL} versus Temperature.

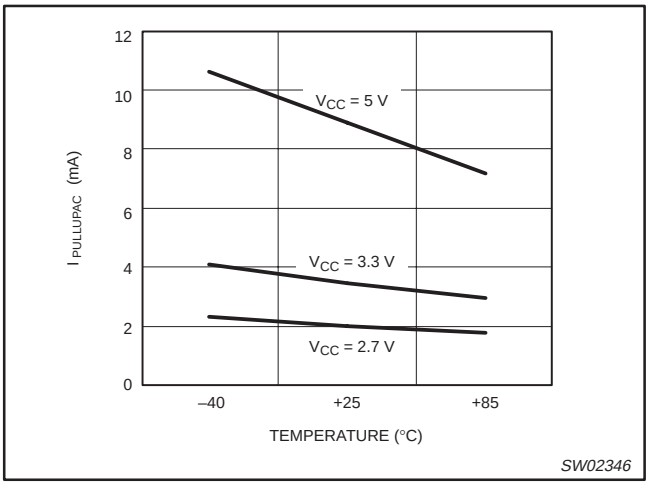


Figure 14. $I_{PULLUPAC}$ versus Temperature.

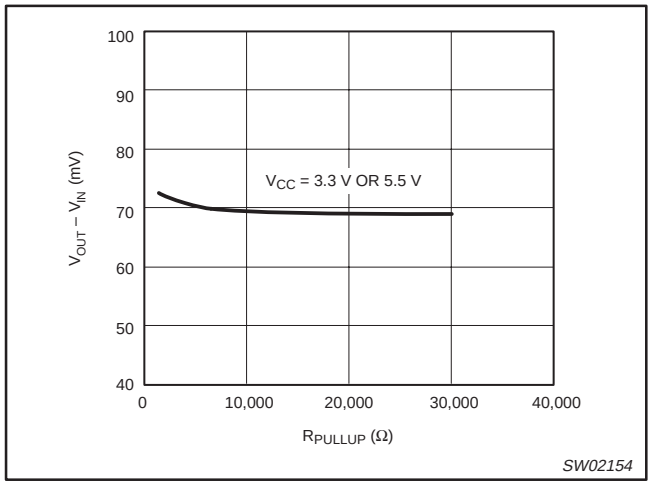


Figure 16. Connection circuitry V_{OUT} – V_{IN}.

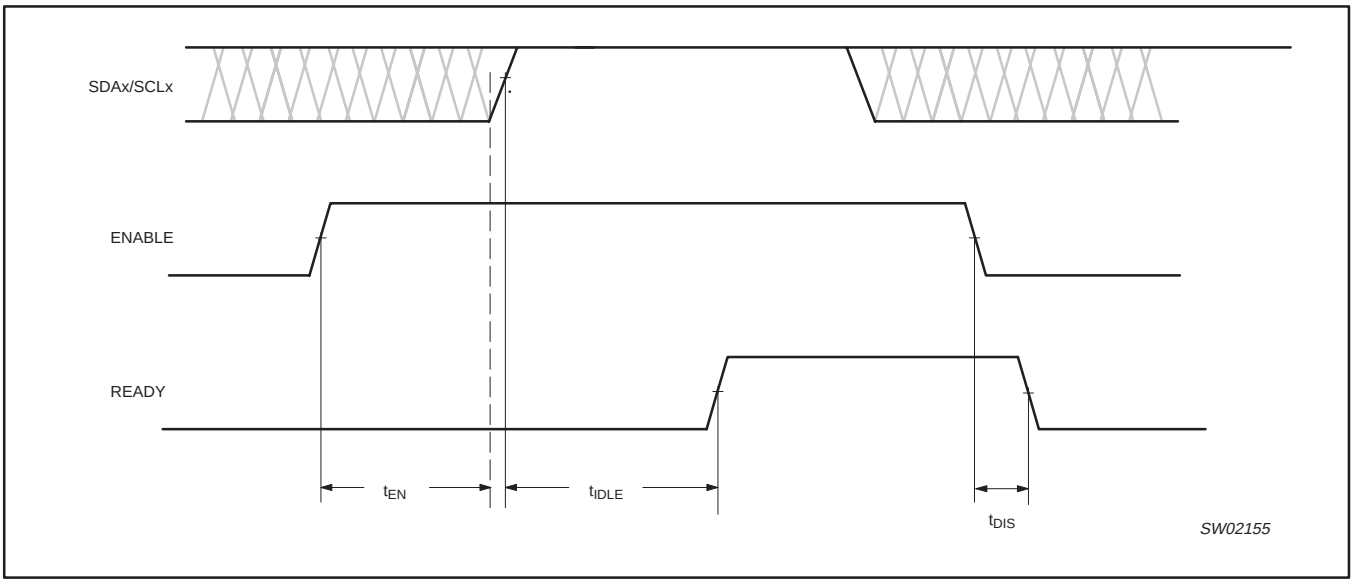


Figure 17. Timing for t_{ENABLE}, t_{IDLE}, and $t_{DISABLE}$

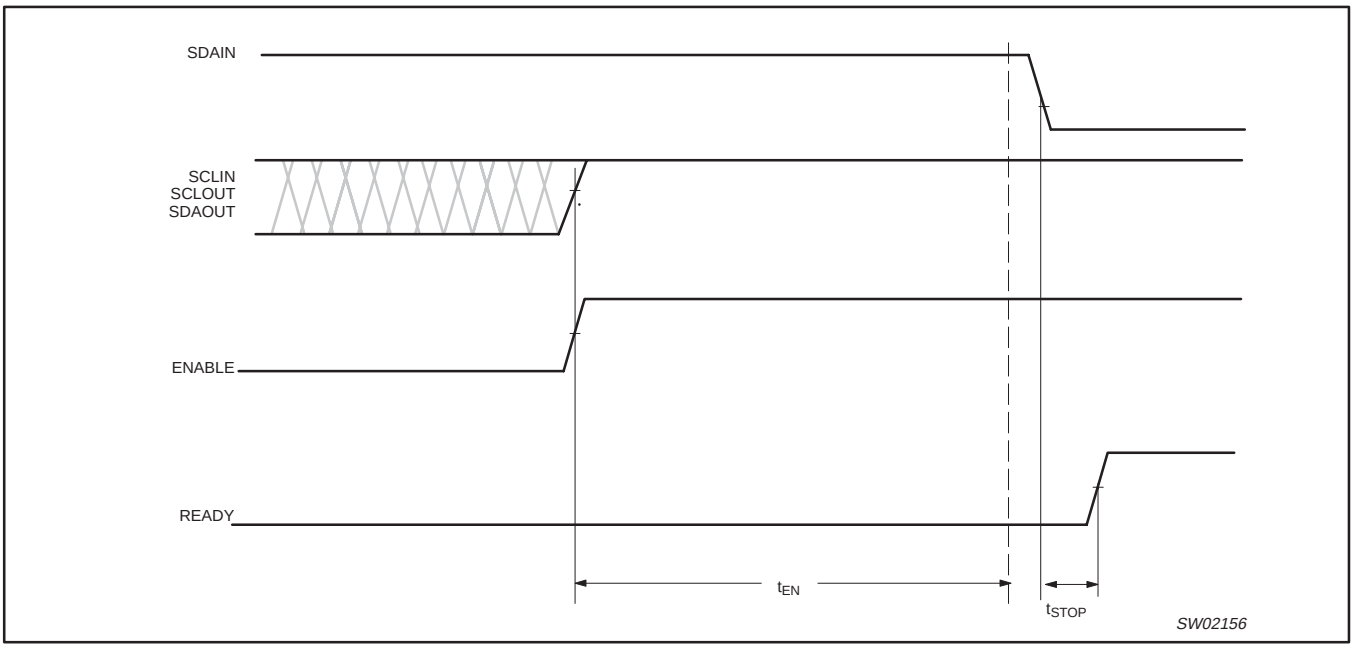


Figure 18. t_{STOP} that can occur after t_{ENALBE}

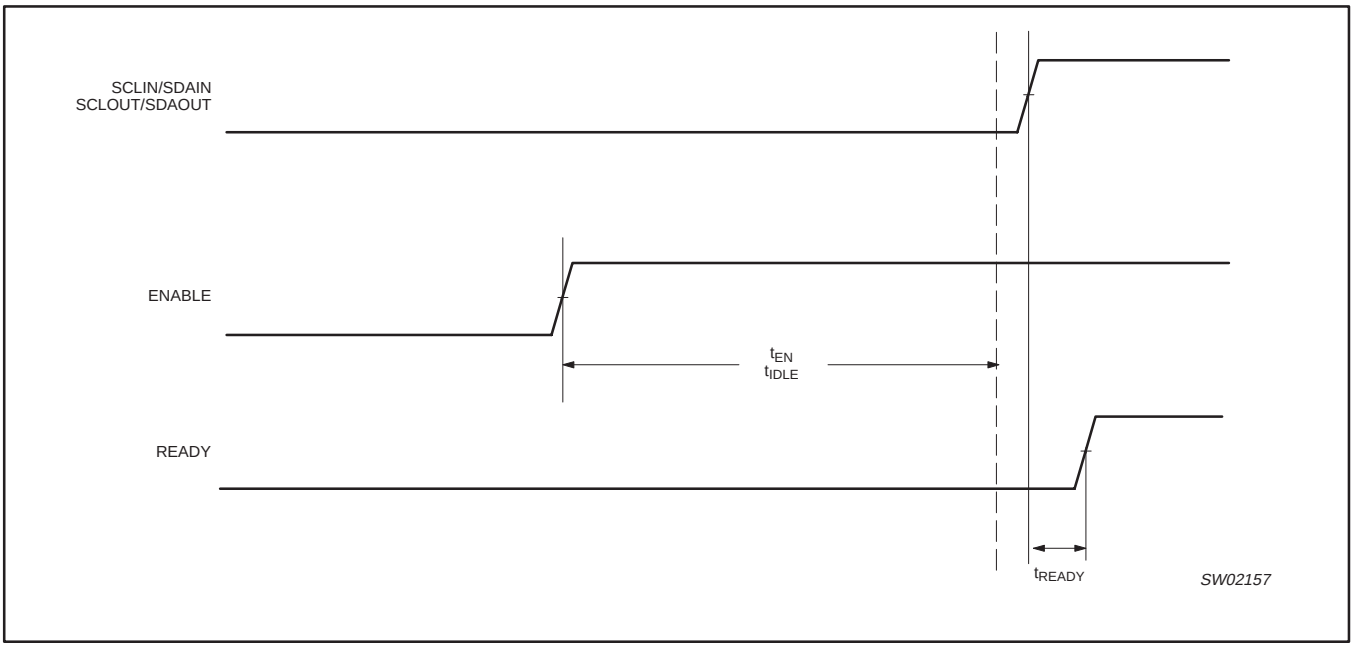
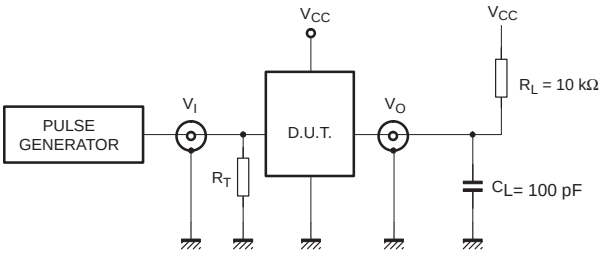


Figure 19. t_{READY} delay that can occur after t_{ENALBE} and t_{IDLE}



DEFINITIONS

R_L = Load resistor.

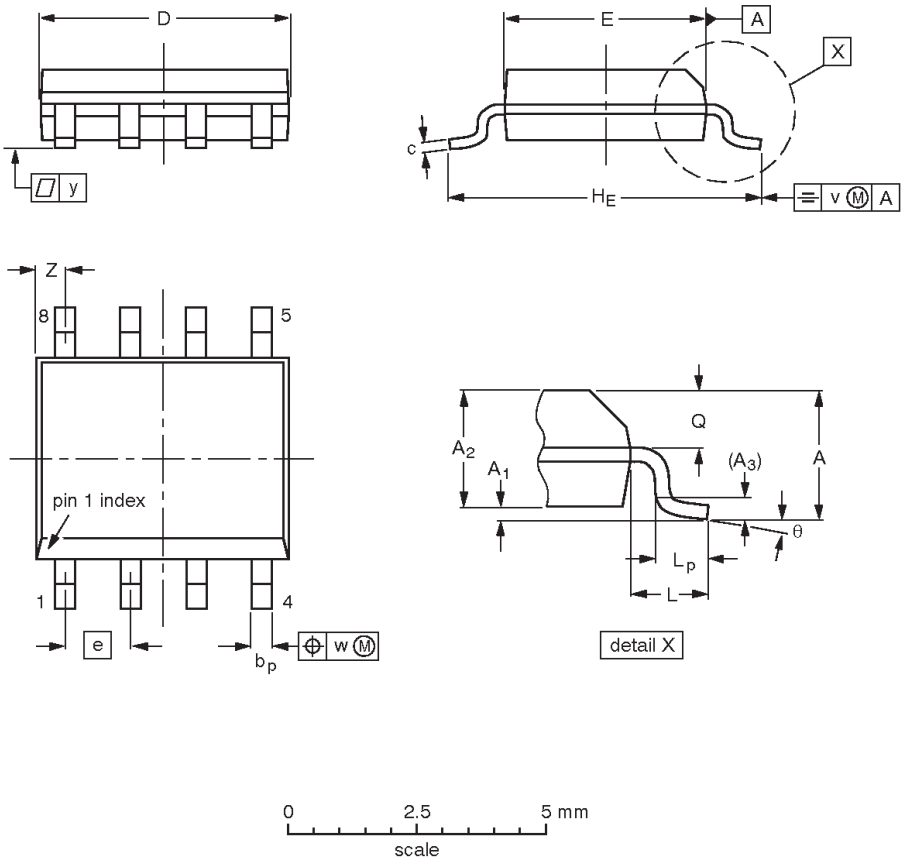
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02345

Figure 20. Test circuitry for switching times

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

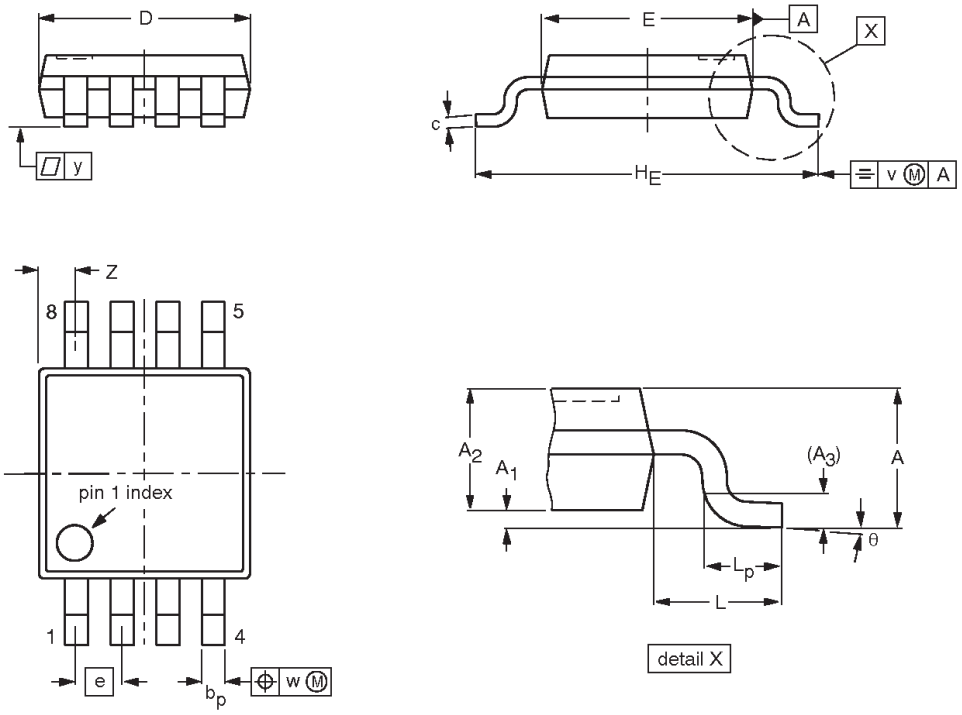
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

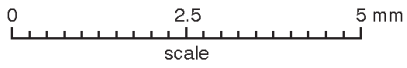
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_3	20041005	**Product data (9397 750 14001). Supersedes data of 2004 Jan 07 (9397 750 12609).** Modifications: ● 'Description' section on page 2: – Fourth paragraph: add "over the PCA9510 and PCA9511" to end of sentence. – Add fifth paragraph. ● 'Features' section on page 2: – fourth bullet: delete "(PCA9513 and PCA9514 only)" – last bullet: add "(MSOP8)" ● Add section "Maximum number of devices in series" on page 6 ● Section "Minimum SDA and SCL Capacitance Requirements" on page 7 re-written. ● Delete (old) Figure 11 "Repeater/bus extender application using the PCA9514" ● 'Absolute Maximum Ratings' table on page 12: add parameters I_I and I_{IO}. ● Electrical characteristics table, subsection "System characteristics": change Unit for $t_{hD,DAT}$ and $t_{su,DAT}$ from µs to ns. ● Figure 20 modified.
_2	20040107	**Product data (9397 750 12609); ECN 853-2441 01-A15108 dated 06 January 2004. Supersedes data of 18 Dec 2003 (9397 750 12559).**
_1	20031202	**Product data (9397 750 12559); ECN 853-2441 01-A14986 dated 15 December 2003.**

Hot swappable I²C and SMBus bus buffer PCA9513; PCA9514

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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