

**INTEGRATED CIRCUITS**

# DATA SHEET

## **TDA9829T** **Downconverter for DVB**

Product specification  
File under Integrated Circuits, IC02

1998 Nov 09

## Downconverter for DVB

## TDA9829T

## FEATURES

- 5 V supply voltage
- Gain controlled IF-amplifier
- Mixer for DVB-IF downconversion
- VCO for Quadrature Amplitude Modulation (QAM) carrier recovery
- External VCO control
- Internal and external AGC
- DVB output level adjust via AGC adjust
- High level DVB operational output amplifier
- Mute switch for DVB output
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

## GENERAL DESCRIPTION

The TDA9829T is an integrated circuit for DVB-IF processing.

## QUICK REFERENCE DATA

| SYMBOL             | PARAMETER   | CONDITIONS  | MIN. | TYP. | MAX. | UNIT        |
|--------------------|---|---|------|------|------|-------------|
| $V_P$              | supply voltage  | note 1  | 4.5  | 5.0  | 5.5  | V           |
| $I_P$              | supply current  |   | 81   | 96   | 111  | mA          |
| $V_{3-4(rms)}$     | input sensitivity (RMS value)                           | -1 dB DVB signal at output                              | -    | 100  | 150  | $\mu$ V     |
| $\Delta\phi_{SSB}$ | VCO phase noise   | $f = 100$ kHz; free-running                             | 103  | 107  | -    | dBc/Hz      |
| $\alpha_{mute}$    | mute attenuation  | note 2  | -    | 36   | -    | dB          |
| $I_{12(sink)}$     | sink current  | maximum tuner gain reduction; see Fig.3                 | 1.5  | 2    | 2.6  | mA          |
| $CR_{stps(US)}$    | control steepness $\Delta I_{14}/\Delta f_{IF}$ for USA | $f_{IF} = 43.75$ MHz; notes 3 and 4; see Fig.4          | 0.7  | 0.98 | 1.3  | $\mu$ A/kHz |
| $V_{11(p-p)}$      | output voltage (peak-to-peak value)                     | $C_L < 15$ pF; $R_L > 5$ k $\Omega$ ; with internal AGC | 1.8  | 2.1  | 2.4  | V           |
| $B_{-1dB}$         | -1 dB bandwidth   | $C_L < 15$ pF; $R_L > 5$ k $\Omega$                     | 11   | 12   | -    | MHz         |
| $\alpha_H$         | suppression of in-band harmonics                        | $V_o = 2.0$ V (p-p)                                     | 30   | 35   | -    | dB          |
| PSRR               | power supply ripple rejection at pin 11                 | see Fig.5   | 26   | 36   | -    | dB          |

## Notes

1. Performance may be decreased at  $V_P = 4.5$  V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.4. The AFC-steepness can be changed by the resistors at pin 14.
4. Depending on the ratio  $\Delta C/C_0$  of the LC resonant circuit of VCO ( $Q_0 > 50$ ;  $C_0 = C_{int} + C_{ext}$ ; see Table 2).

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ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| TDA9829T    | SO20    | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |

BLOCK DIAGRAM

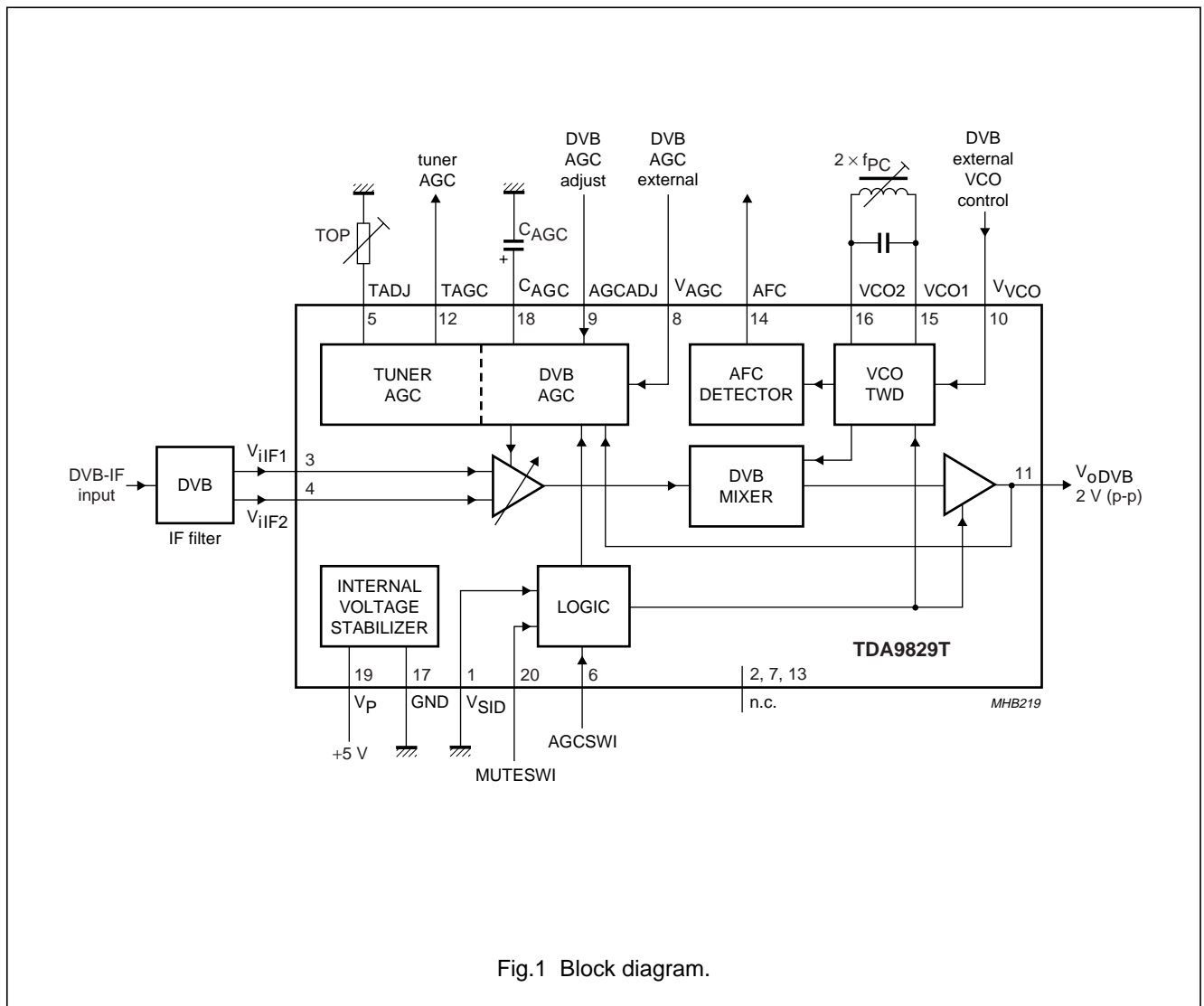


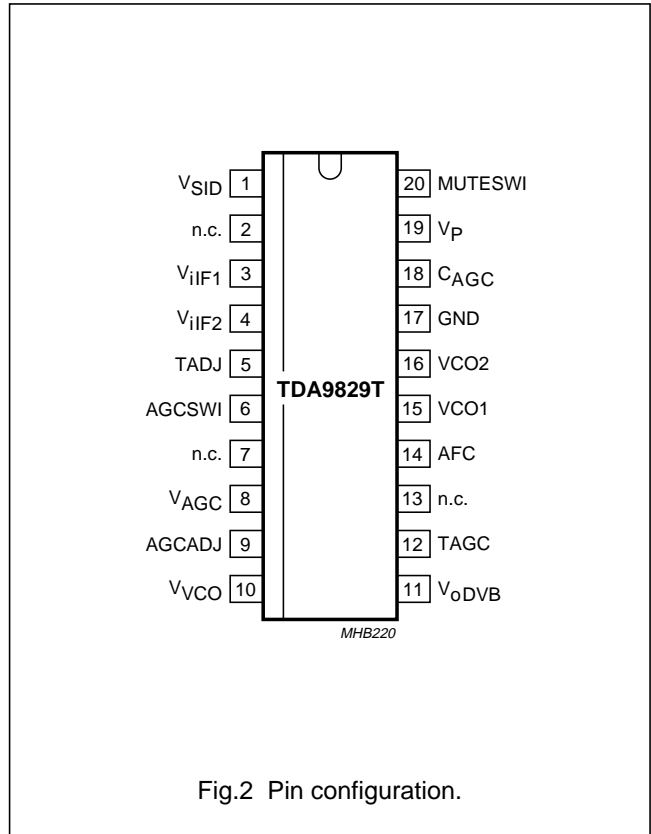
Fig.1 Block diagram.

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**PINNING**

| SYMBOL            | PIN | DESCRIPTION                            |
|-------------------|-----|--|
| V <sub>SID</sub>  | 1   | SIF down input                         |
| n.c.              | 2   | not connected                          |
| V <sub>iIF1</sub> | 3   | IF differential input signal voltage 1 |
| V <sub>iIF2</sub> | 4   | IF differential input signal voltage 2 |
| TADJ              | 5   | tuner AGC takeover adjust (TOP)        |
| AGCSWI            | 6   | AGC switch input                       |
| n.c.              | 7   | not connected                          |
| V <sub>AGC</sub>  | 8   | AGC voltage input                      |
| AGCADJ            | 9   | AGC adjust input                       |
| V <sub>VCO</sub>  | 10  | VCO control voltage                    |
| V <sub>oDVB</sub> | 11  | DVB output                             |
| TAGC              | 12  | tuner AGC output                       |
| n.c.              | 13  | not connected                          |
| AFC               | 14  | AFC output                             |
| VCO1              | 15  | VCO1 reference circuit                 |
| VCO2              | 16  | VCO2 reference circuit                 |
| GND               | 17  | ground                                 |
| C <sub>AGC</sub>  | 18  | AGC capacitor                          |
| V <sub>P</sub>    | 19  | supply voltage (+5 V)                  |
| MUTESWI           | 20  | mute switch input                      |



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**FUNCTIONAL DESCRIPTION****Vision IF amplifier**

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration to control the IF gain.

**VCO, Travelling Wave Divider (TWD) and AFC**

The VCO operates with a resonance circuit (with L and C in parallel) at double the IF frequency plus symbol frequency. The VCO is controlled by integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to its actual frequency is fed to the capacitors. This control voltage is amplified and converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates a differential output signal for downconverting the IF signal.

**DVB mixer**

The gain controlled DVB-IF signal is downconverted to the symbol frequency by use of a four quadrant multiplier. The conversion signal is provided by the VCO and TWD.

**DVB AGC and tuner AGC**

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting the IF and tuner gain in order to keep the DVB signal at a constant level.

A peak detector is used for the DVB AGC. The peak value of (digital) the QAM signal is detected and controlled to a constant value by the variable gain IF amplifier.

The detector bandwidth is adapted to the symbol frequency (3 to 11 MHz). The external AGC time constant is given by the IF AGC capacitor at pin 18.

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output).

The tuner AGC takeover point can be adjusted. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The DVB output signal ( $V_{\text{ODVB}}$ ) can be adjusted in a range of  $\pm 3$  dB by a control voltage ( $\Delta V_{\text{adj}}$ ) at pin 9. The internal AGC can be switched off at pin 6 and the IF gain can be controlled by an external voltage at pin 8. The tuner AGC is active in both instances.

**DVB output amplifier**

The output amplifier for the DVB signal has a high bandwidth and delivers a 2 V (p-p) signal. The amplifier can be switched to a mute state forced by the signal at pin 20.

**Internal voltage stabilizer**

A band gap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL               | PARAMETER                                    | CONDITIONS                         | MIN. | MAX.  | UNIT |
|----------------------|--|------------------------------------|------|-------|------|
| $V_P$                | supply voltage (pin 19)                      | maximum chip temperature of 125 °C | 0    | 5.5   | V    |
| $V_n$                | voltage at pins 1 to 10, 13, 14 and 18 to 20 |                                    | 0    | $V_P$ | V    |
| $t_{\text{sc(max)}}$ | maximum short-circuit time                   |                                    | –    | 10    | s    |
| $V_{12}$             | tuner AGC output voltage                     |                                    | 0    | 13.2  | V    |
| $T_{\text{stg}}$     | storage temperature                          |                                    | –25  | +150  | °C   |
| $T_{\text{amb}}$     | operating ambient temperature                |                                    | –20  | +70   | °C   |
| $V_{\text{es}}$      | electrostatic handling voltage               | machine model class B              | –300 | +300  | V    |

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## THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 85    | K/W  |

## CHARACTERISTICS

$V_P = 5$  V;  $T_{amb} = 25$  °C; see Table 1 for input frequencies; input level  $V_{iIF(3-4)} = 10$  mV (RMS value); measurements taken in Fig.8; unless otherwise specified.

| SYMBOL  | PARAMETER   | CONDITIONS                                    | MIN.        | TYP.         | MAX.   | UNIT           |
|---|---|---|-------------|--------------|--------|----------------|
| <b>Supply (pin 19)</b>  |   |   |             |              |        |                |
| $V_P$   | supply voltage  | note 1  | 4.5         | 5.0          | 5.5    | V              |
| $I_P$   | supply current  |   | 81          | 96           | 111    | mA             |
| <b>IF amplifier (measured at <math>f_{IF} = 43.75</math> MHz; pins 3 and 4)</b> |   |   |             |              |        |                |
| $\Delta V_{(3-4)(rms)}$   | input sensitivity (RMS value)                               | -1 dB DVB signal at output                    | -           | 100          | 150    | $\mu$ V        |
| $V_{i(3-4)(rms)}$   | maximum input signal level (RMS value)                      | 1 dB DVB signal at output                     | 140         | 200          | -      | mV             |
| $\Delta G_{IF}$   | total gain control IF amplifier                             |   | 59          | 64           | -      | dB             |
|   | tilt for $\Delta f \pm 3$ MHz                               | $f_s = 6.9$ MHz; 40 dB gain                   | -           | 0.5          | 1      | dB             |
| $R_{i(3-4)(diff)}$  | input resistance (differential)                             | note 2  | -           | 2.2          | -      | k $\Omega$     |
| $C_{i(3-4)(diff)}$  | input capacitance (differential)                            | note 2  | -           | 1.7          | -      | pF             |
| <b>DVB mixer and VCO (pins 10, 15 and 16); see notes 4 and 5 and Table 1</b>    |   |   |             |              |        |                |
| $f_{VCO(max)}$  | maximum oscillator frequency                                | $2(f_{IF} + f_s)$                             | 125         | 130          | -      | MHz            |
| $f_{VCO(US)}$   | VCO frequency for USA                                       | $2(f_{IF} + f_s)$                             | -           | 97.5         | -      | MHz            |
| $f_{VCO(EU)}$   | VCO frequency for Europe                                    | $2(f_{IF} + f_s)$                             | -           | 86.0         | -      | MHz            |
| $V_{ref(rms)}$  | oscillator voltage swing between pins 15 and 16 (RMS value) |   | -           | 60           | -      | mV             |
| $\Delta\phi_{SSB}$  | VCO phase noise   | $f = 100$ kHz; free-running                   | 103         | 107          | -      | dBc/Hz         |
| $V_{VCO}$   | VCO control range (pin 10)                                  | see Figs 6 and 7                              | 0           | -            | $V_P$  | V              |
| $R_{i(VCO)}$  | VCO control input resistance (pin 10)                       |   | 50          | 63           | 76     | k $\Omega$     |
| $CR_{stps(VCO)}$  | control steepness $\Delta f_s / \Delta V_{10}$              | see Figs 6 and 7<br>DVB (USA)<br>DVB (Europe) | -<br>-<br>- | 0.29<br>0.40 | -<br>- | MHz/V<br>MHz/V |
| <b>DVB output amplifier (pins 11 and 20)</b>                                    |   |   |             |              |        |                |
| $V_{o(DVB)(p-p)}$   | DVB output signal (QAM) (peak-to-peak value)                |   | 1.8         | 2.1          | 2.4    | V              |
| $I_{bias(int)}$   | DC internal bias current for emitter-follower (pin 11)      |   | 1.9         | 2.3          | 2.7    | mA             |
| $I_{sink(max)}$   | maximum AC and DC output sink current (pin 11)              |   | 1.5         | -            | -      | mA             |
| $I_{source(max)}$   | maximum AC and DC output source current (pin 11)            |   | 2.0         | -            | -      | mA             |

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| SYMBOL                                      | PARAMETER  | CONDITIONS  | MIN. | TYP. | MAX.  | UNIT             |
|---|--|---|------|------|-------|------------------|
| $\alpha_{\text{mute}}$                      | mute attenuation   | note 2  | –    | 36   | –     | dB               |
| $V_{i(\text{mute})}$                        | mute switch input voltage (pin 20)   | DVB mute; note 3  | 1.3  | –    | $V_P$ | V                |
|   |  | DVB no mute   | 0    | –    | 0.8   | V                |
| $I_{\text{IL}}$                             | LOW-level input current (pin 20)   | $V_{20} = 0 \text{ V}$  | 180  | 230  | 280   | $\mu\text{A}$    |
| <b>DVB AGC detector (pins 8, 9 and 18)</b>  |  |   |      |      |       |                  |
| $t_{\text{resp}}$                           | response to an increasing amplitude step in the IF input signal                  | note 6  | –    | 0.25 | –     | ms/dB            |
|   | response to a decreasing amplitude step in the IF input signal                   | note 6  | –    | 0.25 | –     | ms/dB            |
| $I_{\text{ch}}$                             | charging current (pin 18)  |   | –    | 200  | –     | $\mu\text{A}$    |
| $I_{\text{dch}}$                            | discharging current (pin 18)   |   | –    | 200  | –     | $\mu\text{A}$    |
| $\Delta V_{i(\text{AGC})}$                  | AGC adjust input voltage range (pin 9)   |   | 1    | 2.5  | 4.5   | V                |
| $\Delta R_{i(\text{AGC})}$                  | AGC adjust input resistance (pin 9)  |   | 8    | 10   | 12    | $\text{k}\Omega$ |
| $\Delta \text{AGC}_{\text{steps}}$          | AGC adjust steepness   | $2 \text{ V} < V_9 < 3 \text{ V}$   | –    | –5   | –     | dB/V             |
| $V_{\text{AGC}(\text{ext})}$                | external AGC voltage for DVB (pin 8)   | see Fig.3   | 1    | –    | 4.5   | V                |
| $R_{i(\text{AGC})}(\text{ext})$             | external AGC input resistance (pin 8)  |   | 40   | –    | –     | $\text{k}\Omega$ |
| <b>Tuner AGC (pin 12)</b>                   |  |   |      |      |       |                  |
| $V_{i(\text{min})}(\text{rms})$             | IF input signal voltage for minimum starting point of tuner takeover (RMS value) | input at pins 3 and 4;<br>$R_{\text{TOP}} = 22 \text{ k}\Omega$ ;<br>$I_{\text{TAGC}} = 0.4 \text{ mA}$ | –    | 2    | 5     | mV               |
| $V_{i(\text{max})}(\text{rms})$             | IF input signal voltage for maximum starting point of tuner takeover (RMS value) | input at pins 3 and 4;<br>$R_{\text{TOP}} = 0 \Omega$ ; $I_{\text{TAGC}} = 0.4 \text{ mA}$              | 50   | 100  | –     | mV               |
| $V_o$                                       | permissible output voltage   | from external source; note 2  | –    | –    | 13.2  | V                |
| $V_{\text{sat}}$                            | saturation voltage   | $I_{\text{TAGC}} = 1.5 \text{ mA}$  | –    | –    | 0.2   | V                |
| $\frac{\Delta V_{\text{TOP},12}}{\Delta T}$ | variation of takeover point by temperature                                       | $I_{\text{TAGC}} = 0.4 \text{ mA}$  | –    | 0.03 | 0.07  | dB/K             |
| $I_{\text{sink}}$                           | sink current   | see Fig.3<br>no tuner gain reduction;<br>$V_{\text{TAGC}} = 13.2 \text{ V}$                             | –    | –    | 5     | $\mu\text{A}$    |
|   |  | maximum tuner gain reduction  | 1.5  | 2    | 2.6   | mA               |

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| SYMBOL   | PARAMETER  | CONDITIONS  | MIN. | TYP. | MAX. | UNIT        |
|--|--|---|------|------|------|-------------|
| $\Delta G_{IF}$  | IF slip by automatic gain control                          | tuner gain current from 20 to 80%                       | –    | 6    | 8    | dB          |
| <b>AFC circuit (pin 14); see notes 7 and 8 and Fig.4</b> |  |   |      |      |      |             |
| $CR_{stps(US)}$  | control steepness $\Delta I_{14}/\Delta f_{IF}$ for USA    | $f_{IF} = 43.75$ MHz                                    | 0.7  | 0.98 | 1.3  | $\mu A/kHz$ |
| $CR_{stps(EU)}$  | control steepness $\Delta I_{14}/\Delta f_{IF}$ for Europe | $f_{IF} = 36.15$ MHz                                    | 0.45 | 0.70 | 0.95 | $\mu A/kHz$ |
| <b>DVB output signal (IF input to DVB output)</b>        |  |   |      |      |      |             |
| $V_{o(p-p)}$   | output voltage (pin 11) (peak-to-peak value)               | $C_L < 15$ pF; $R_L > 5$ k $\Omega$ ; with internal AGC | 1.8  | 2.1  | 2.4  | V           |
| $V_{O(DC)}$  | DC output voltage  |   | –    | 2.5  | –    | V           |
| $B_{-1dB}$   | –1 dB bandwidth  | $C_L < 15$ pF; $R_L > 5$ k $\Omega$                     | 11   | 12   | –    | MHz         |
| $B_{-3dB}$   | –3 dB bandwidth  |   | –    | 17   | –    | MHz         |
| $\alpha_{C(DVB)}$  | fundamental input signal and IF harmonics                  |   | 35   | 40   | –    | dB          |
| $\alpha_H$   | suppression of in-band harmonics                           | $V_o = 2.0$ V (p-p)                                     | 30   | 35   | –    | dB          |
| PSRR   | power supply ripple rejection at pin 11                    | see Fig.5   | 26   | 36   | –    | dB          |

**Notes**

- Performance may be decreased at  $V_P = 4.5$  V.
- This parameter is not tested during production and is only given as application information for designing the television receiver.
- Mute state also can be achieved by leaving pin 20 open-circuit.
- Resonance circuit of VCO:  $Q_0 > 50$ ;  $C_{ext}$ ,  $C_{int}$  and L see Table 2.
- Temperature coefficient of external LC-circuit is equal to zero.
- Response speed valid for an IF input level range of 200  $\mu V$  up to 70 mV.
- To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.4. The AFC steepness can be changed by the resistors at pin 14.
- Depending on the ratio  $\Delta C/C_0$  of the LC resonant circuit of VCO ( $Q_0 > 50$ ;  $C_0 = C_{int} + C_{ext}$ ; see Table 2).

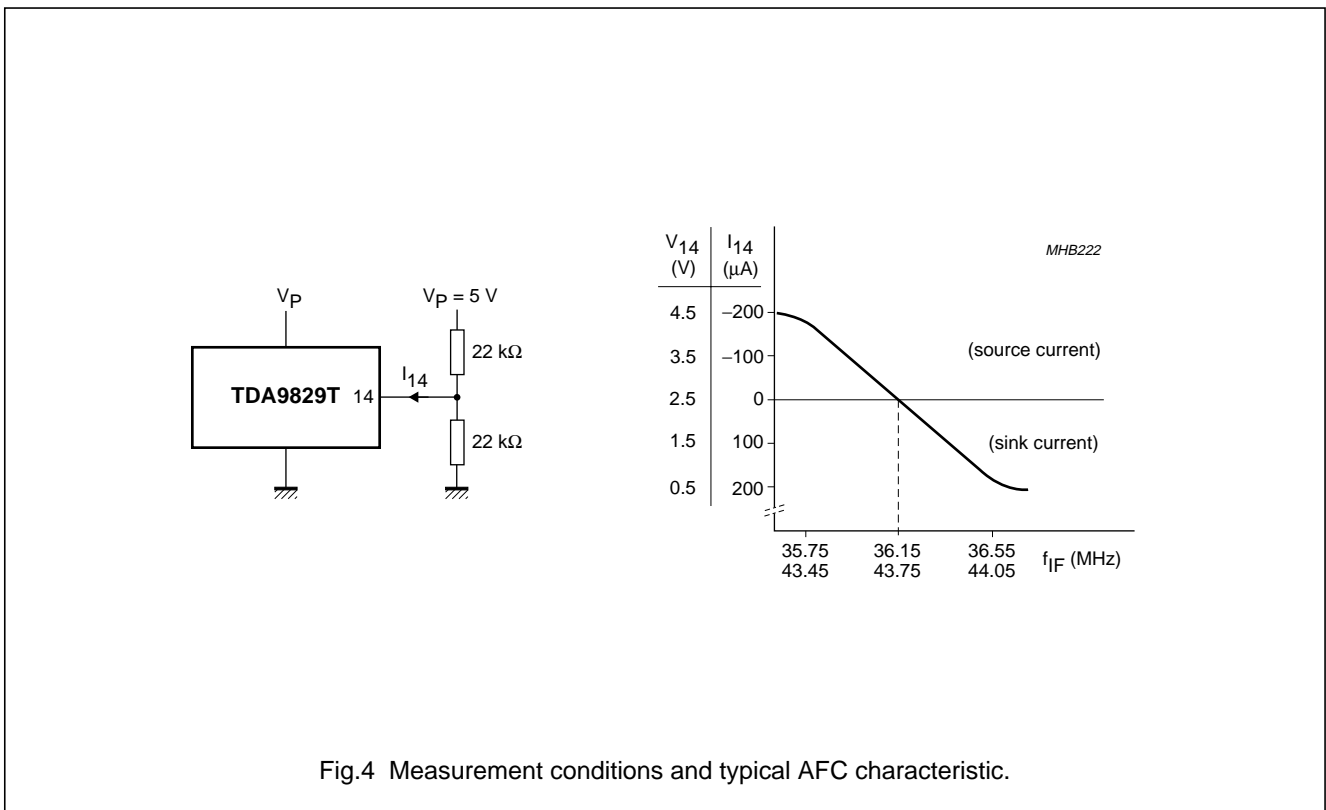
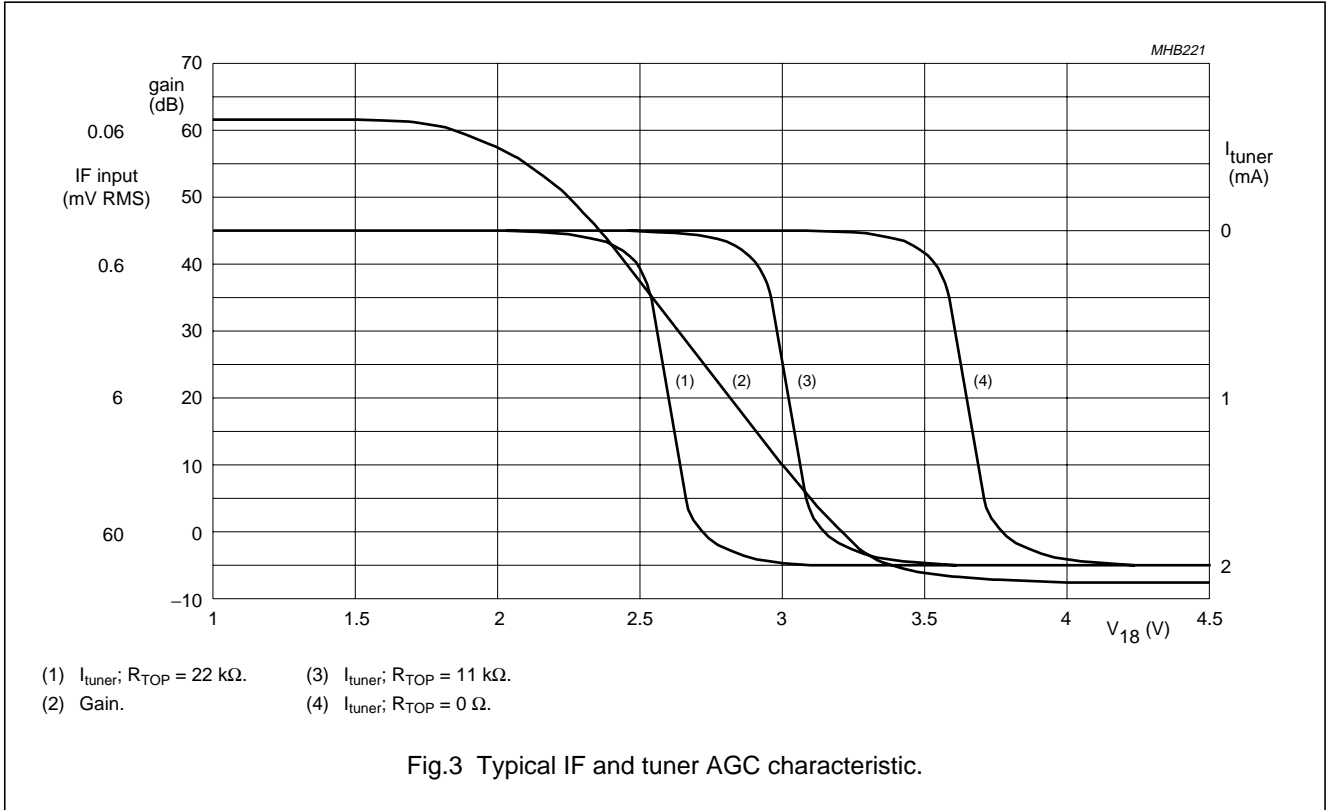
**Table 1** Input frequencies, symbol frequencies and VCO frequencies

| SYMBOL    | DESCRIPTION      | DVB (Europe) | DVB (USA) | UNIT |
|-----------|------------------|--------------|-----------|------|
| $f_s$     | Symbol frequency | 6.9          | 5.0       | MHz  |
| $f_{IF}$  | IF frequency     | 36.15        | 43.75     | MHz  |
| $f_{VCO}$ | VCO frequency    | 86.0         | 97.5      | MHz  |



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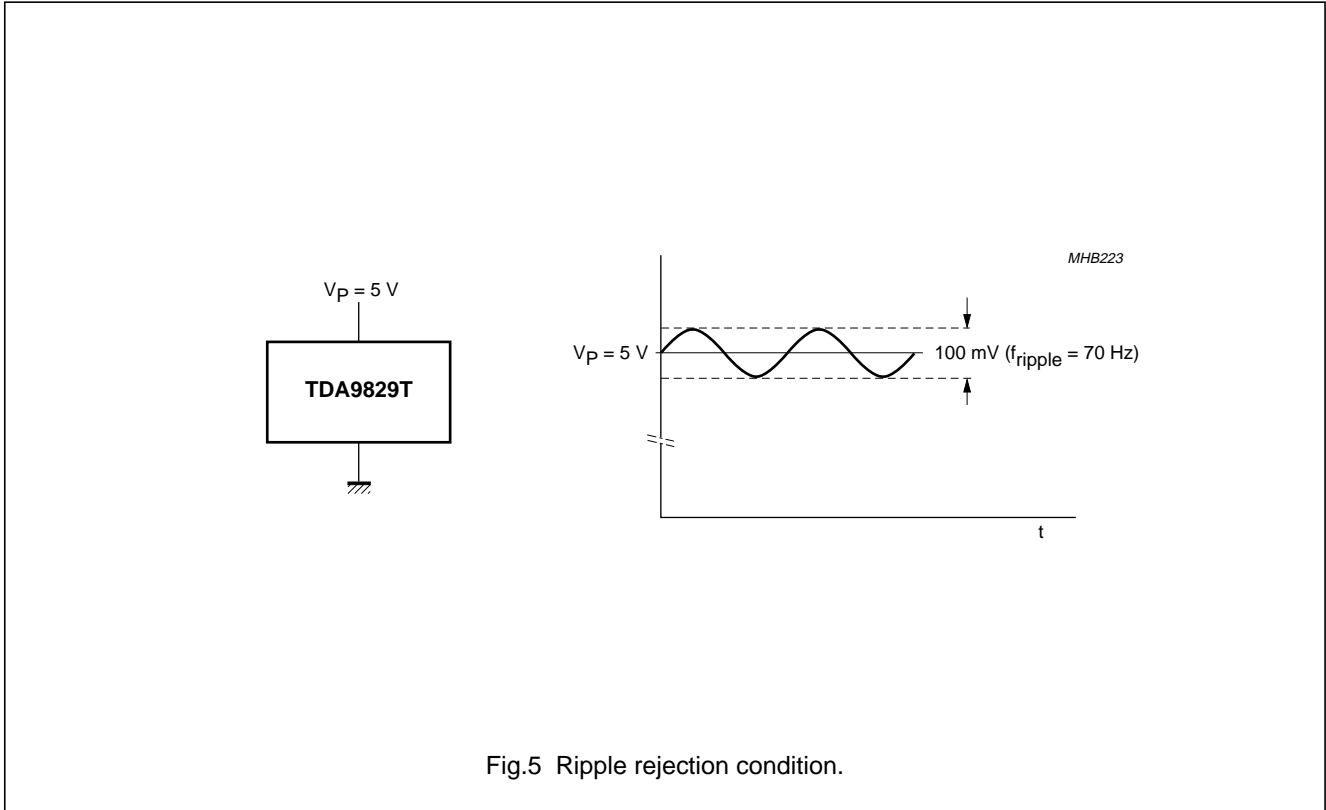
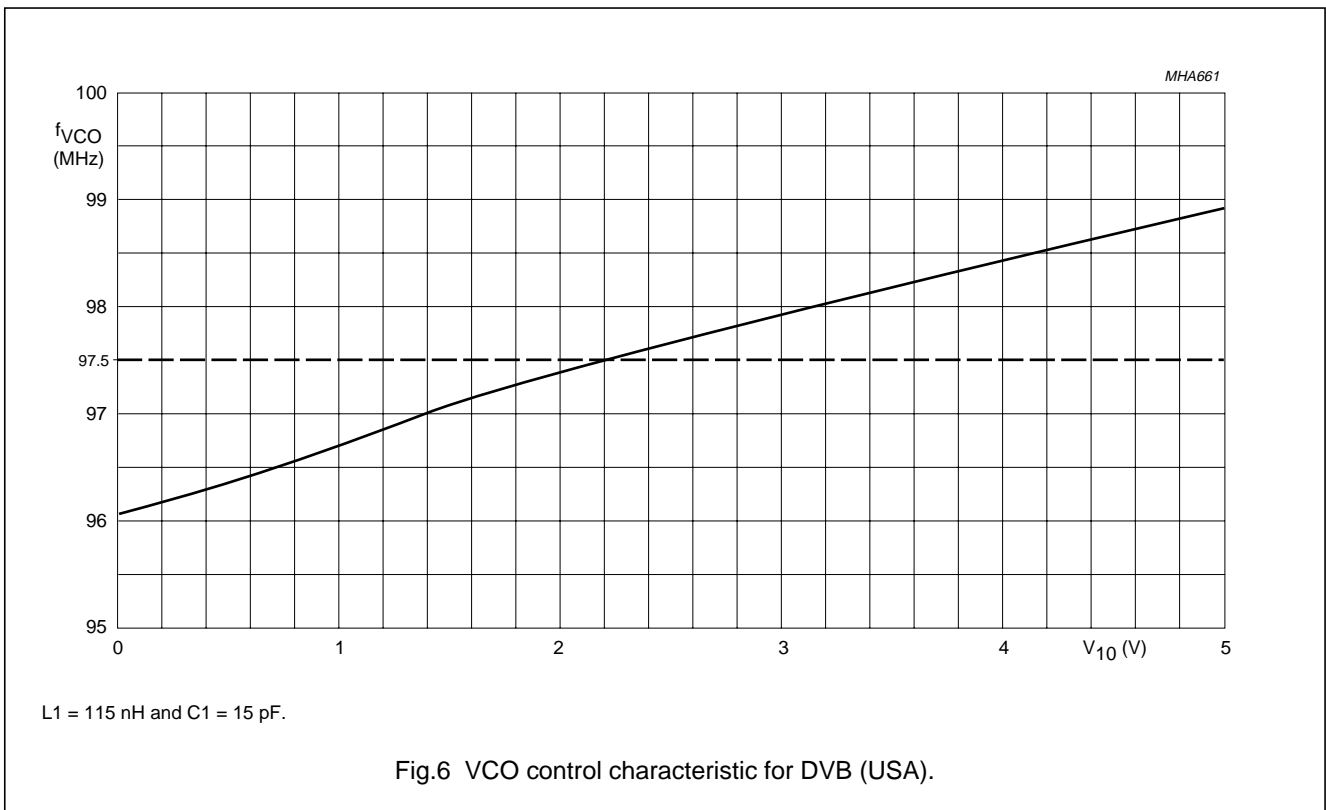


Fig.5 Ripple rejection condition.

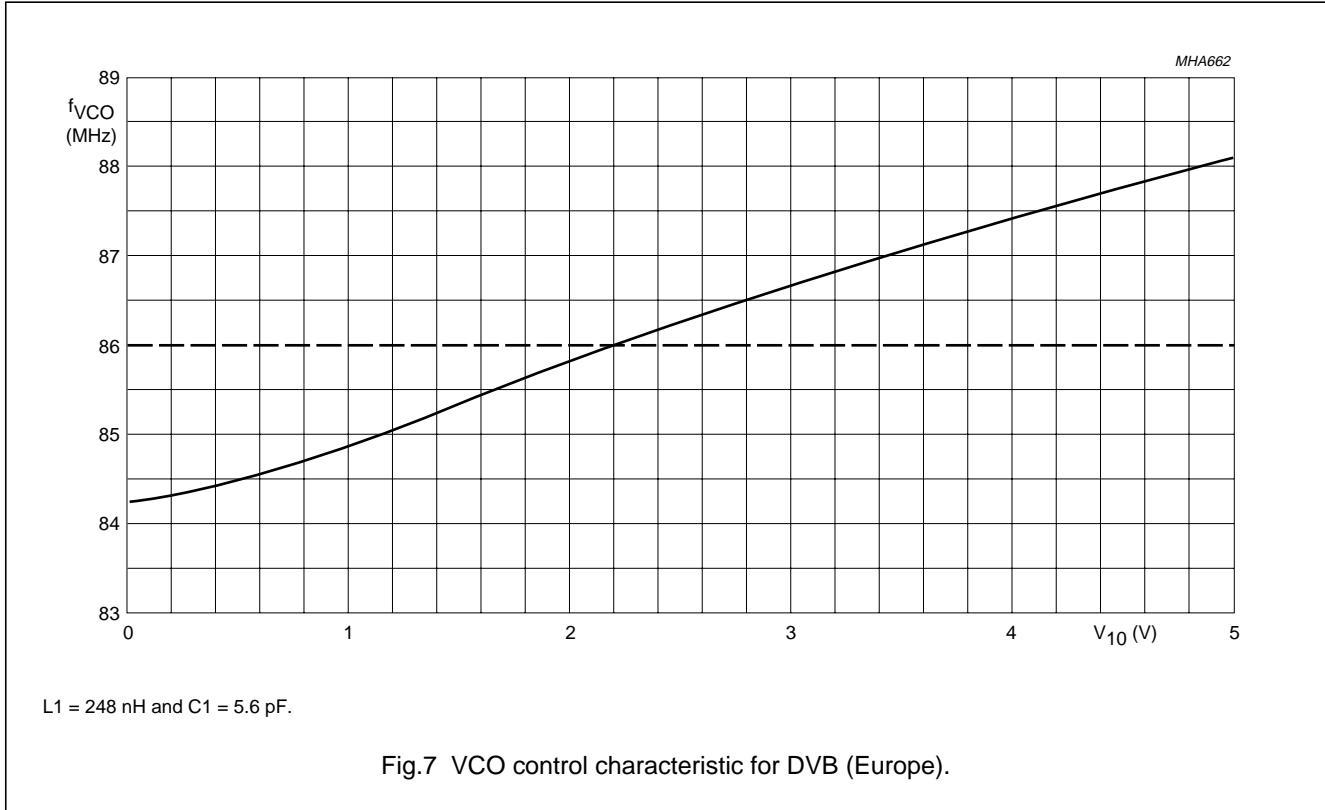


L1 = 115 nH and C1 = 15 pF.

Fig.6 VCO control characteristic for DVB (USA).

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TEST CIRCUIT

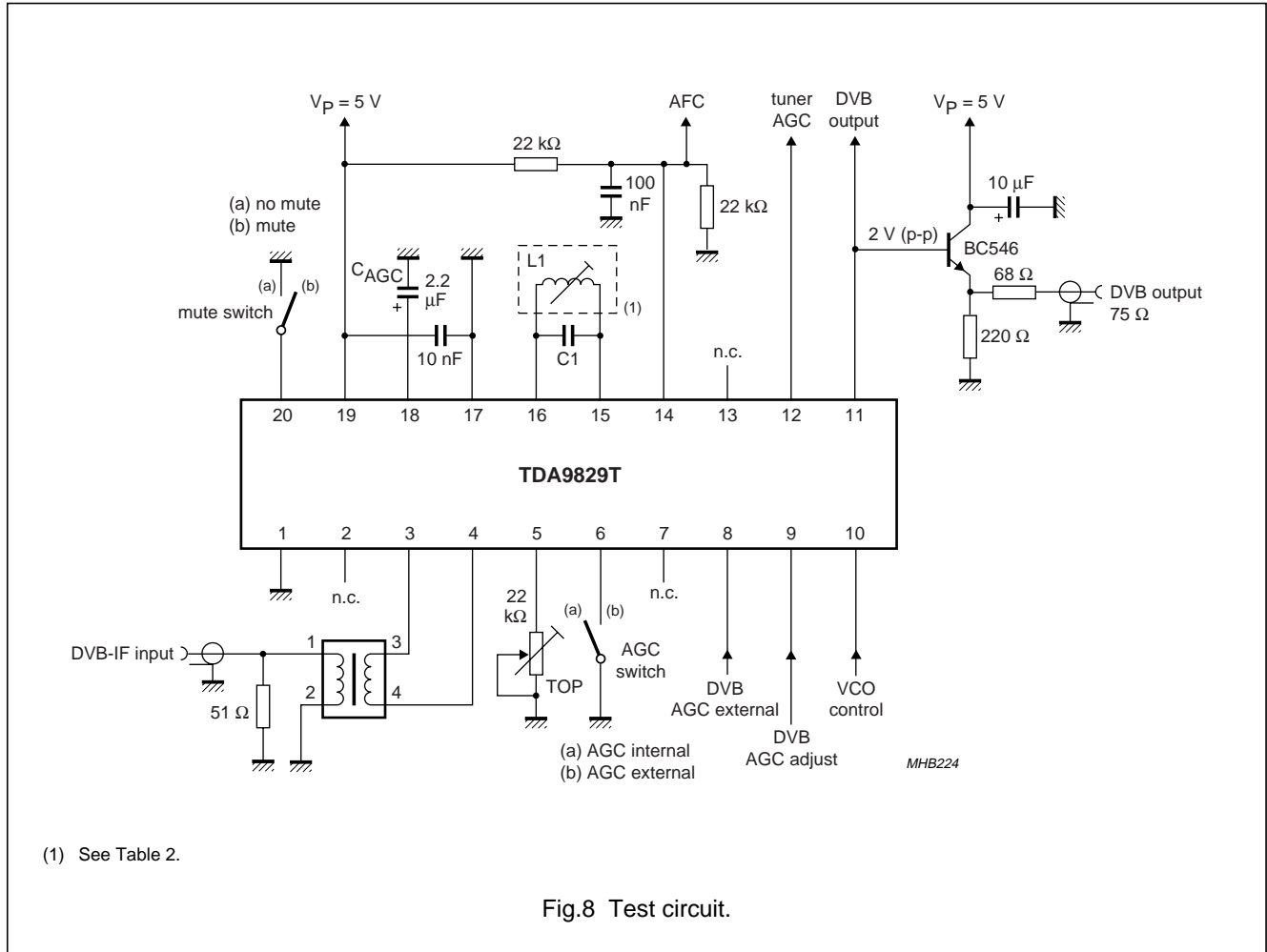


Table 2 Test circuit values

| PARAMETER                 | Europe  | USA  |
|---------------------------|---|--|
| IF frequency              | 36.15 MHz   | 43.75 MHz  |
| VCO frequency             | 86.0 MHz  | 97.5 MHz   |
| Oscillator circuit        | <p>(1) C(VCO) = 8.2 pF.<br/>                 (2) C1 = 5.6 pF.<br/>                 (3) L1 = 248 nH.</p> | <p>(1) C(VCO) = 8.2 pF.<br/>                 (2) C1 = 15 pF.<br/>                 (3) L1 = 115 nH.</p> |
| Toko coil                 | 5KM 369SNS - 2010Z  | 5KM 369SNS - 1647Z   |
| Philips ceramic capacitor | 2222 632 39478  | 2222 632 33129   |

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INTERNAL PIN CONFIGURATIONS

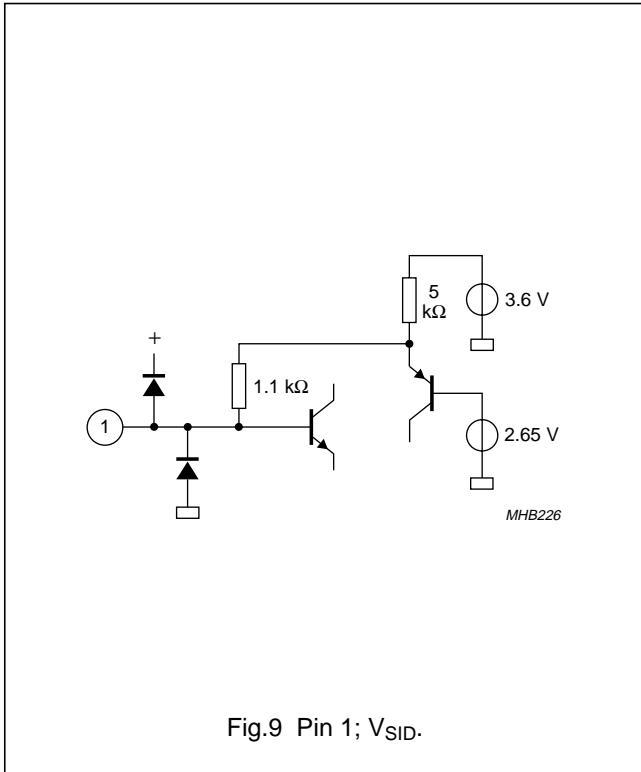


Fig.9 Pin 1; V<sub>SID</sub>.

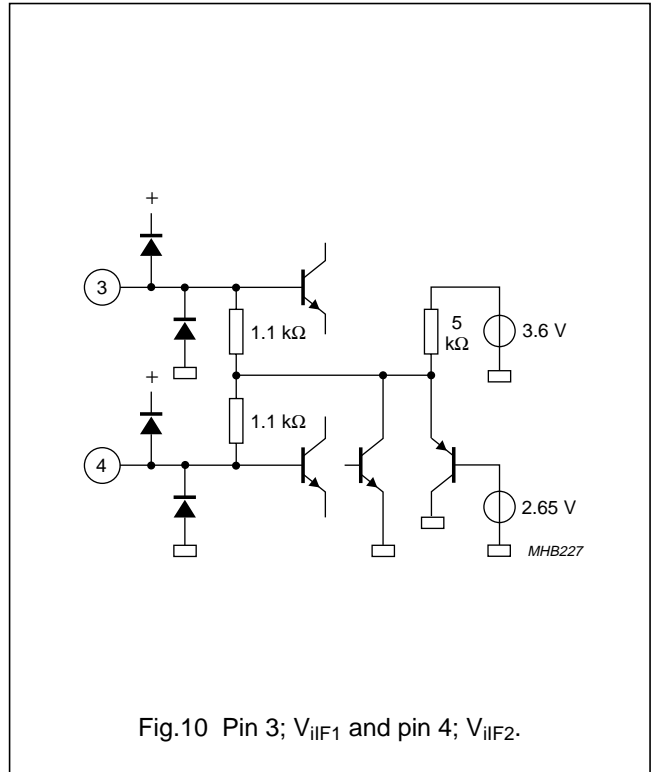


Fig.10 Pin 3; V<sub>II F1</sub> and pin 4; V<sub>II F2</sub>.

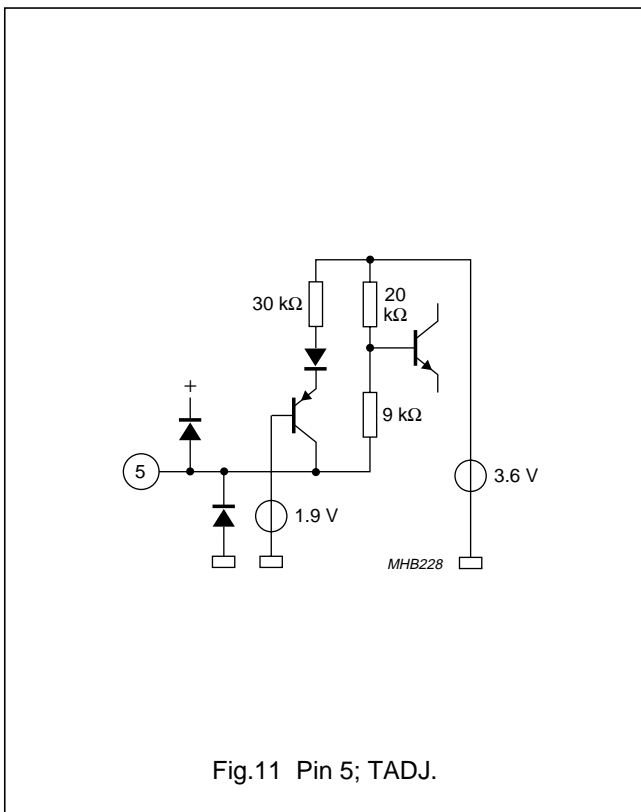


Fig.11 Pin 5; TADJ.

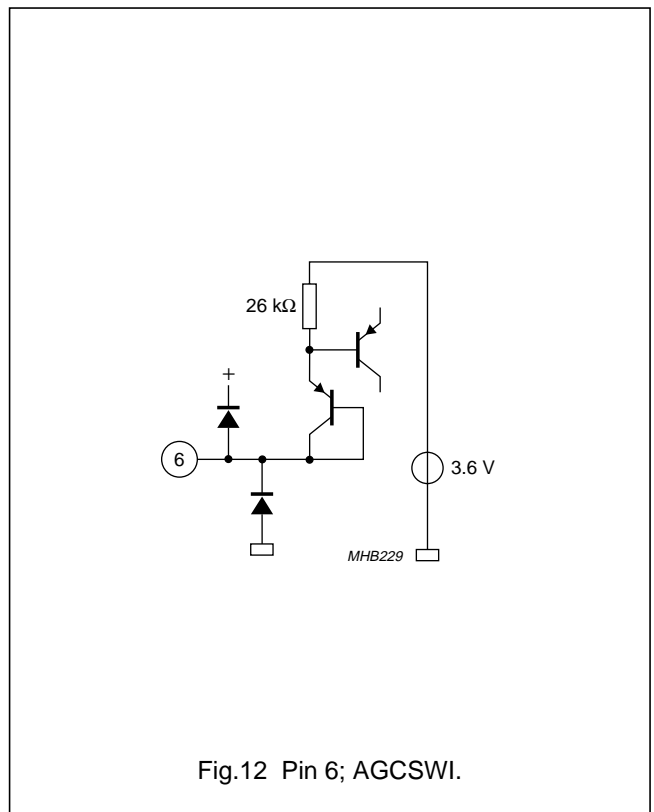


Fig.12 Pin 6; AGCSWI.

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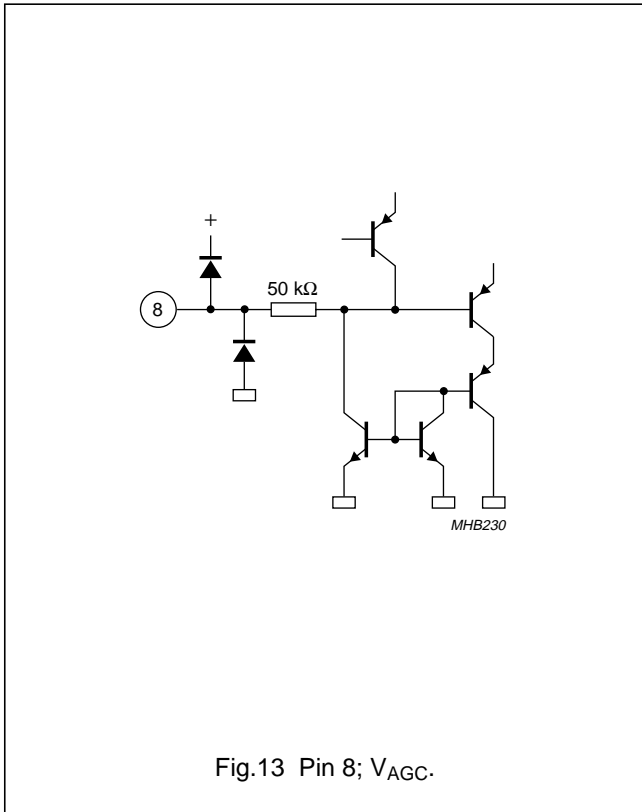


Fig.13 Pin 8;  $V_{AGC}$ .

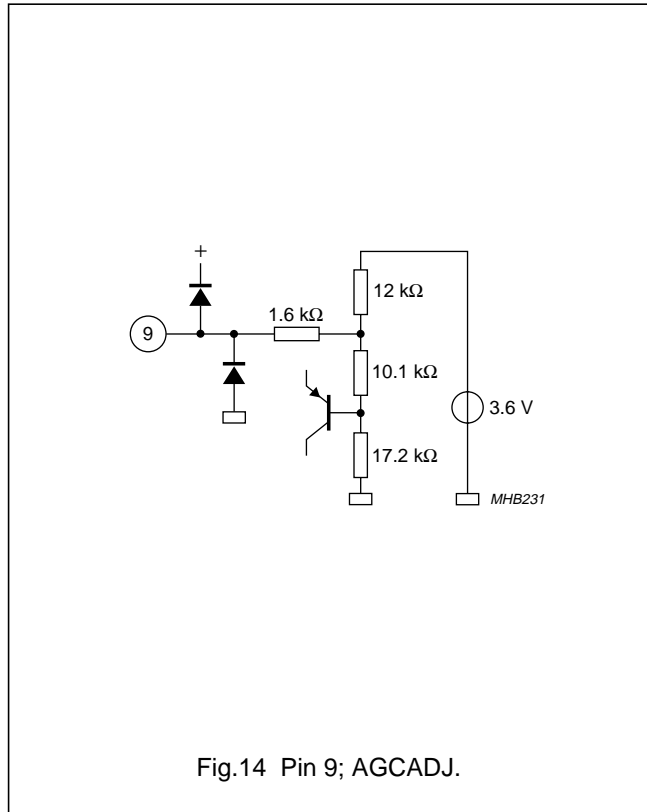


Fig.14 Pin 9; AGCADJ.

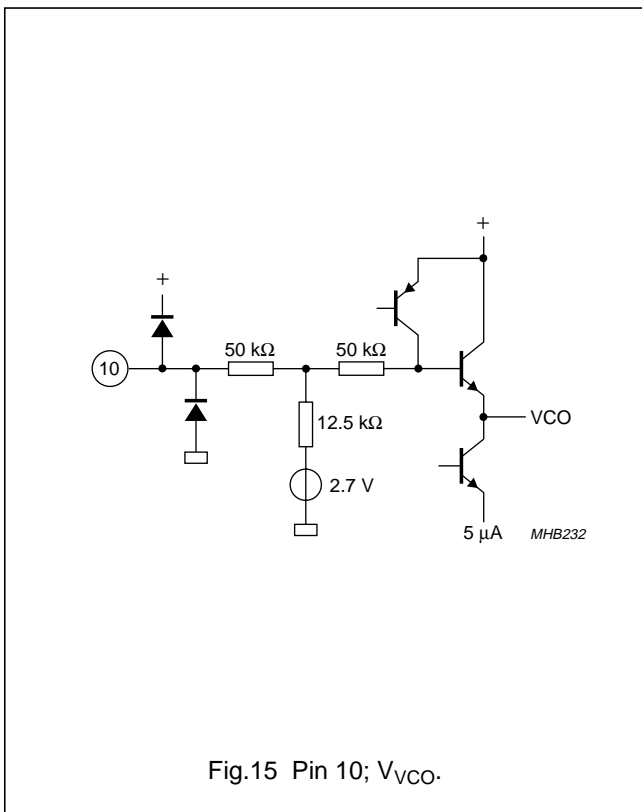


Fig.15 Pin 10;  $V_{VCO}$ .

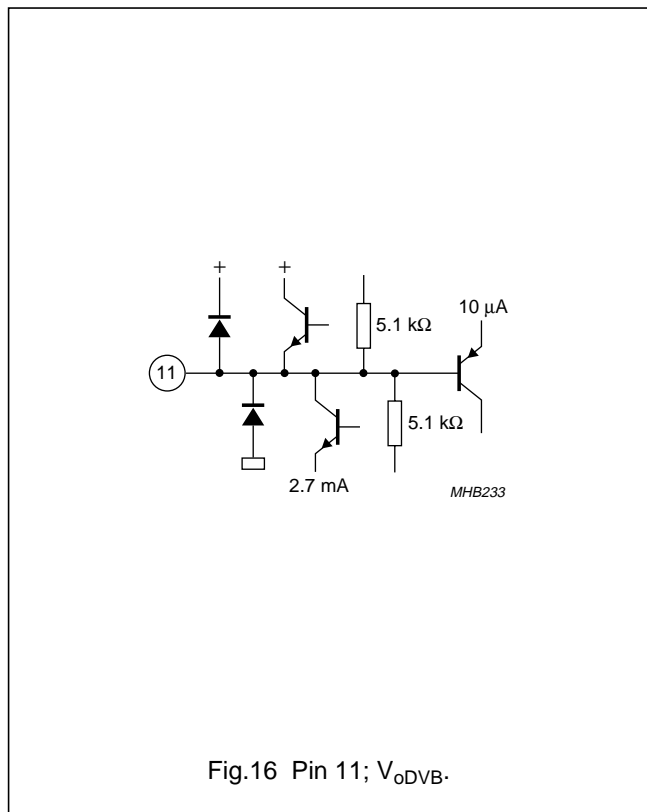


Fig.16 Pin 11;  $V_{ODVB}$ .

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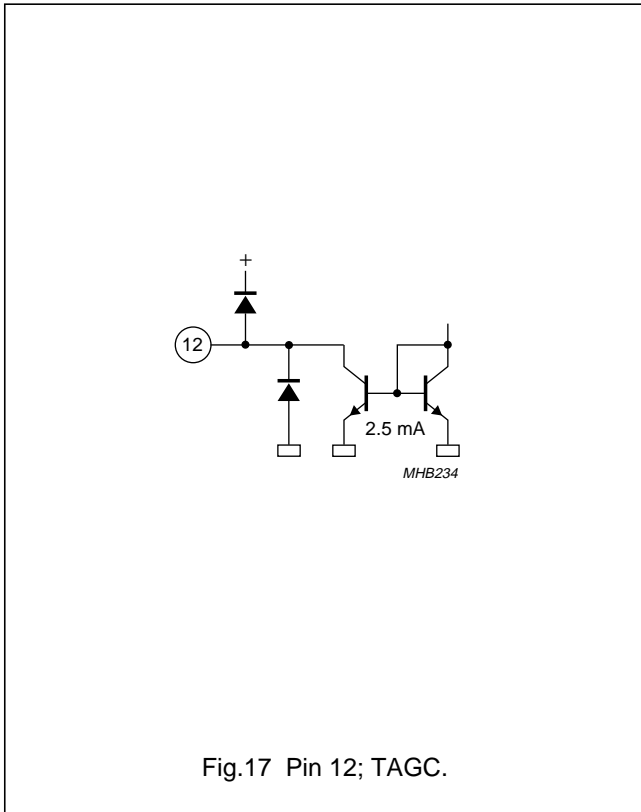


Fig.17 Pin 12; TAGC.

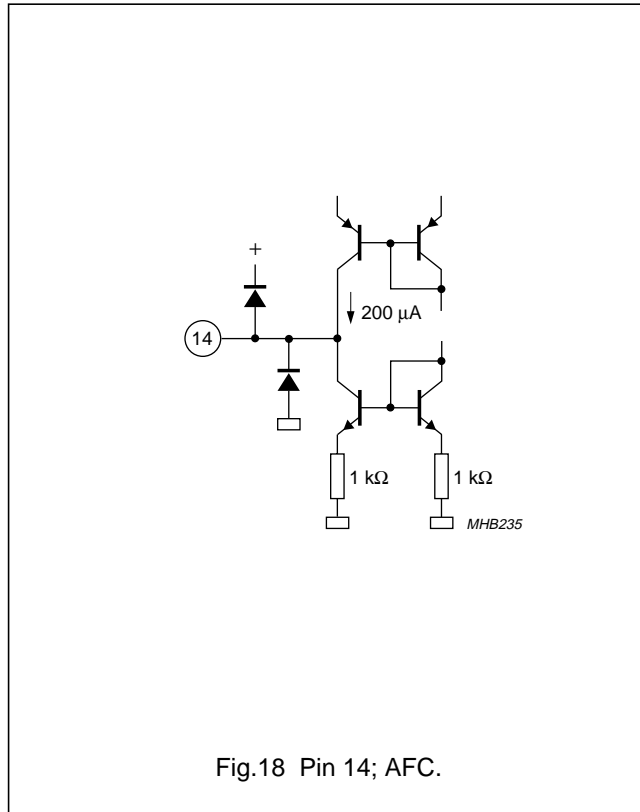


Fig.18 Pin 14; AFC.

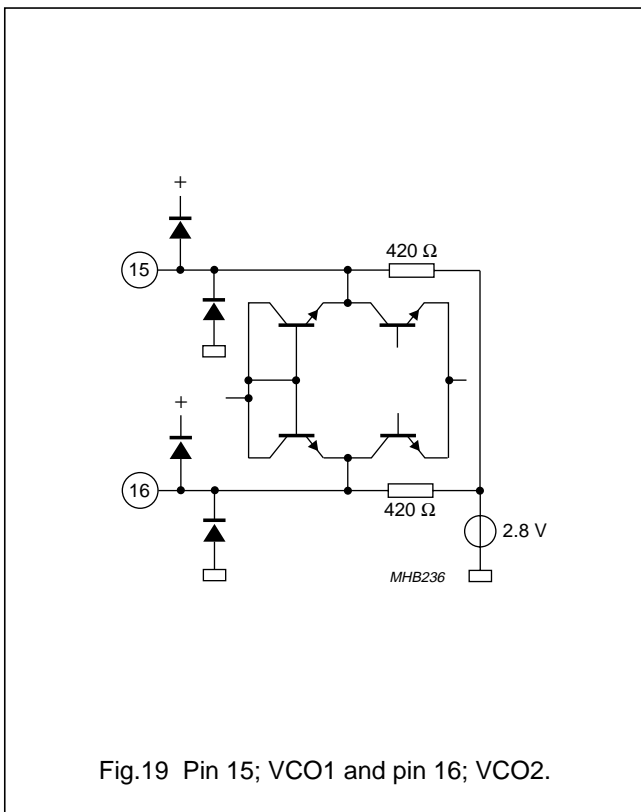


Fig.19 Pin 15; VCO1 and pin 16; VCO2.

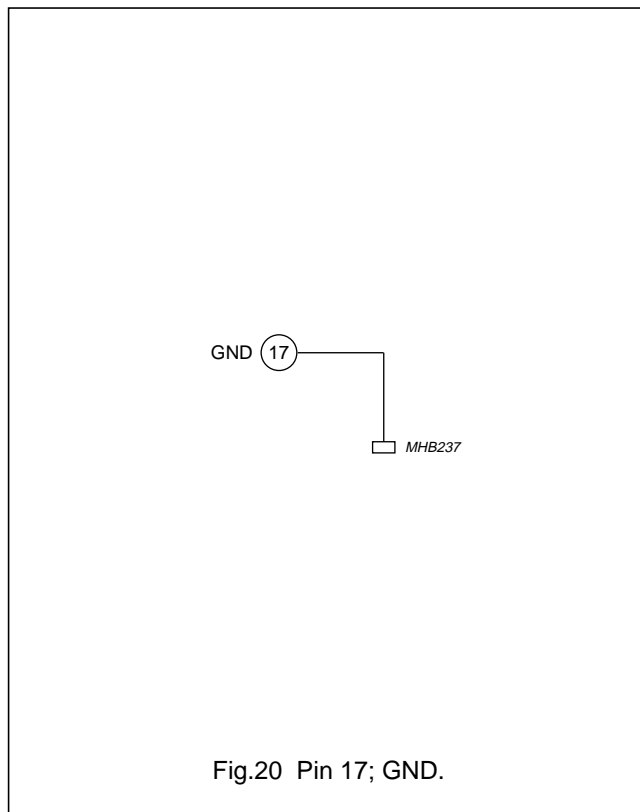


Fig.20 Pin 17; GND.

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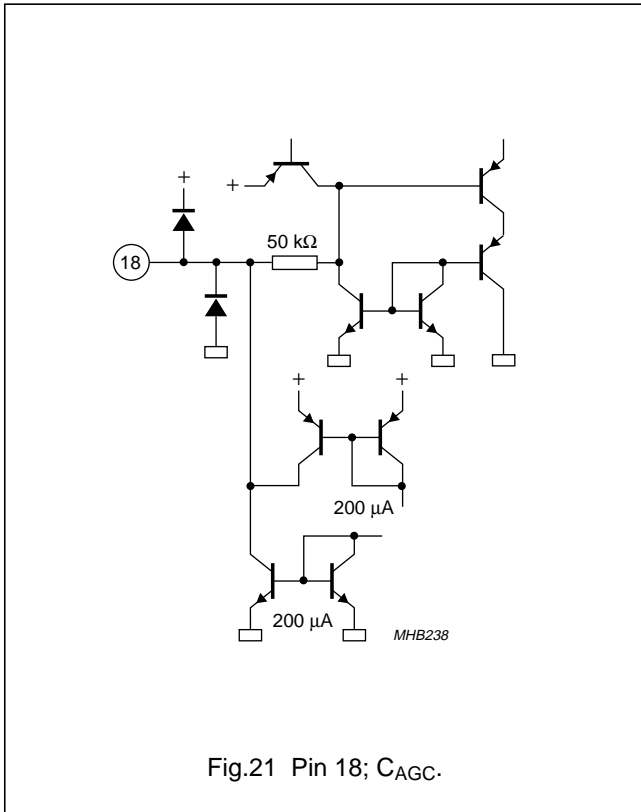


Fig.21 Pin 18; C<sub>AGC</sub>.

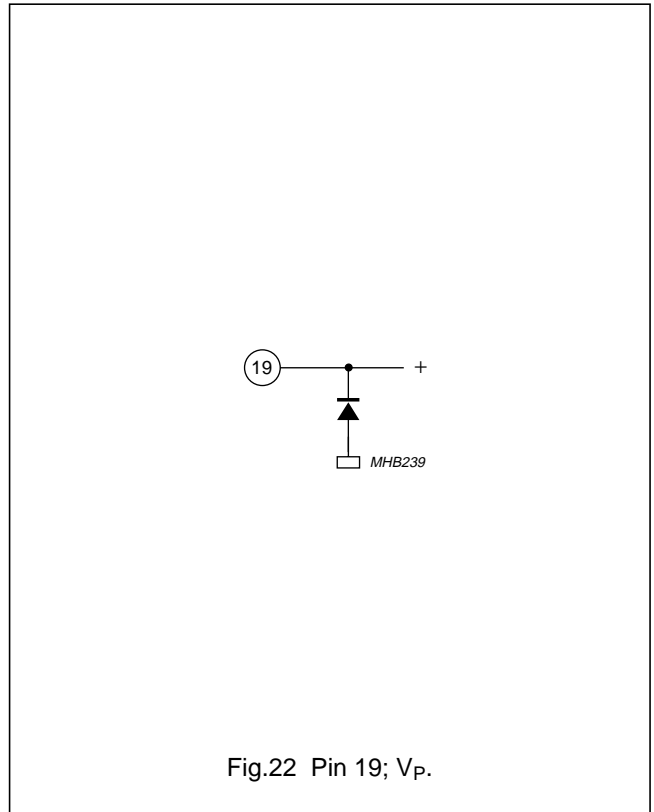


Fig.22 Pin 19; V<sub>P</sub>.

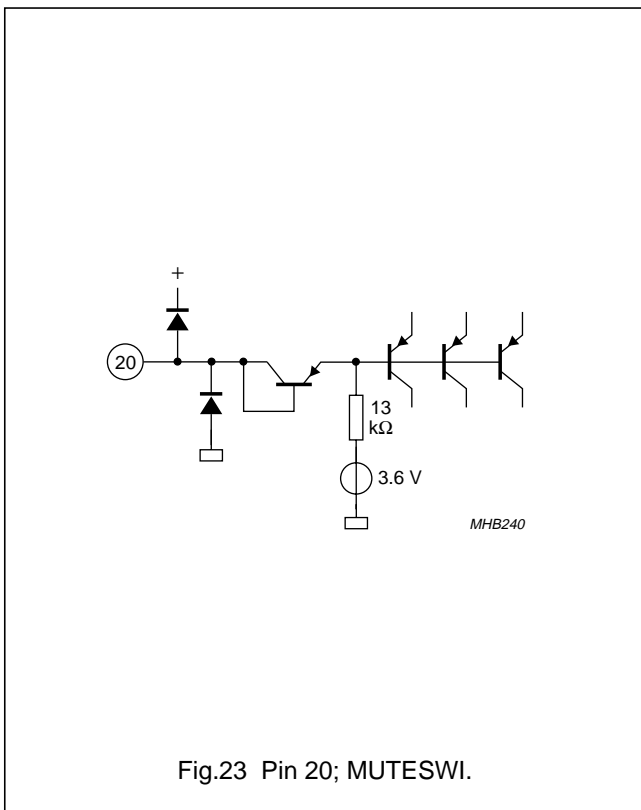


Fig.23 Pin 20; MUTESWI.



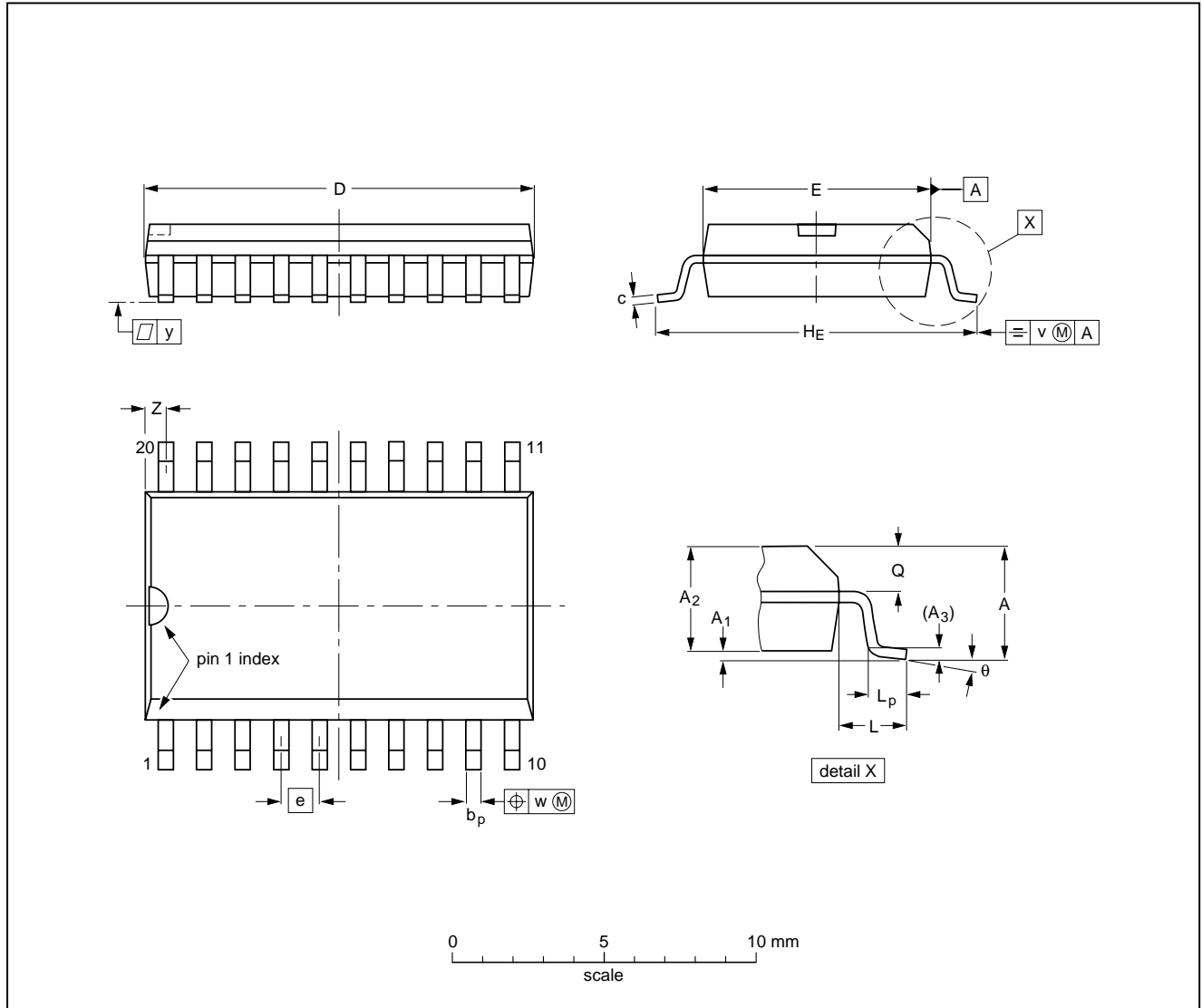
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PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 13.0<br>12.6     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49     | 0.30<br>0.29     | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |                     |                      |
| SOT163-1        | 075E04     | MS-013AC |      |                     | 95-01-24<br>97-05-22 |

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## Downconverter for DVB

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**DEFINITIONS**

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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