

INTEGRATED CIRCUITS

DATA SHEET



TDA9885; TDA9886

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

Product specification
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I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

CONTENTS	10	LIMITING VALUES
1	FEATURES	11
2	GENERAL DESCRIPTION	12
3	APPLICATIONS	13
4	ORDERING INFORMATION	14
5	QUICK REFERENCE DATA	15
6	BLOCK DIAGRAM	15.1
7	PINNING	15.2
8	FUNCTIONAL DESCRIPTION	15.3
8.1	VIF amplifier	15.4
8.2	Tuner AGC and VIF-AGC	15.5
8.3	VIF-AGC detector	
8.4	FPLL detector	16
8.5	VCO and divider	17
8.6	AFC and digital acquisition help	18
8.7	Video demodulator and amplifier	19
8.8	Sound carrier trap	
8.9	SIF amplifier	
8.10	SIF-AGC detector	
8.11	Single reference QSS mixer	
8.12	AM demodulator	
8.13	FM demodulator and acquisition help	
8.14	Audio amplifier and mute time constant	
8.15	Internal voltage stabilizer	
8.16	I ² C-bus transceiver and module address	
9	I ² C-BUS CONTROL	
9.1	Read format	
9.1.1	Slave address	
9.1.2	Data byte	
9.2	Write format	
9.2.1	Subaddress	
9.2.2	Data byte for switching mode	
9.2.3	Data byte for adjust mode	
9.2.4	Data byte for data mode	
		THERMAL CHARACTERISTICS
		CHARACTERISTICS
		TEST AND APPLICATION INFORMATION
		PACKAGE OUTLINES
		SOLDERING
		15.1 Introduction to soldering surface mount packages
		15.2 Reflow soldering
		15.3 Wave soldering
		15.4 Manual soldering
		15.5 Suitability of surface mount IC packages for wave and reflow soldering methods
		DATA SHEET STATUS
		DEFINITIONS
		DISCLAIMERS
		PURCHASE OF PHILIPS I ² C COMPONENTS

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

1 FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C-bus
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module Address (MAD).



2 GENERAL DESCRIPTION

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

3 APPLICATIONS

- TV, VTR, PC, and STB applications.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V3	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
TDA9886T/V4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886HN/V4	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _P	supply voltage	notes 1 and 2	4.5	5.0	5.5	V
I _P	supply current		52	63	70	mA
Video part						
V _{i(VIF)(rms)}	VIF input voltage sensitivity (RMS value)	-1 dB video at output	-	60	100	μV
G _{VIF(cr)}	VIF gain control range	see Fig.7	60	66	-	dB
f _{VIF}	vision carrier operating frequencies	see Table 14	-	33.4	-	MHz
			-	33.9	-	MHz
			-	38.0	-	MHz
			-	38.9	-	MHz
			-	45.75	-	MHz
			-	58.75	-	MHz
Δf _{VIF}	VIF frequency window of digital acquisition help	related to f _{VIF} ; see Fig.10	-	±2.3	-	MHz
V _{o(v)(p-p)}	video signal output voltage (peak-to-peak value)	see Fig.5				
		normal mode	1.7	2.0	2.3	V
		trap bypass mode	0.95	1.10	1.25	V
G _{dif}	differential gain	"CCIR 330"; note 3				
		B/G standard	-	-	5	%
		L standard	-	-	7	%
φ _{dif}	differential phase	"CCIR 330"	-	2	4	deg
B _{v(-1dB)}	-1 dB video bandwidth	trap bypass mode; AC load; C _L < 20 pF; R _L > 1 kΩ	5	6	-	MHz
B _{v(-3dB)(trap)}	-3 dB video bandwidth including sound carrier trap	note 4				
		f _{trap} = 4.5 MHz	3.95	4.05	-	MHz
		f _{trap} = 5.5 MHz	4.90	5.00	-	MHz
		f _{trap} = 6.0 MHz	5.40	5.50	-	MHz
		f _{trap} = 6.5 MHz	5.50	5.95	-	MHz
α _{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	-	dB
		B/G standard	30	36	-	dB
S/N _W	weighted signal-to-noise ratio	weighted in accordance with "CCIR 567"; see Fig.11; note 5	56	59	-	dB
PSRR _{CVBS}	power supply ripple rejection at pin CVBS	f _{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Fig.6	20	25	-	dB
AFC _{stps}	AFC control steepness	definition: ΔI _{AFC} /Δf _{VIF}	0.85	1.05	1.25	μA/kHz

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio part						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 μ s de-emphasis	430	540	650	mV
THD	total harmonic distortion of audio signal	FM: 27 kHz FM deviation; 50 μ s de-emphasis	–	0.15	0.50	%
		AM: m = 54 %	–	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; dependent on FM-PLL filter	80	100	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM: 27 kHz FM deviation; 50 μ s de-emphasis; vision carrier unmodulated	52	56	–	dB
		AM: m = 54 %	45	50	–	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	50 μ s de-emphasis; AM: f = 1 kHz and m = 54 %; referenced to 27 kHz FM deviation	40	46	–	dB
$PSRR_{AUD}$	power supply ripple rejection on pin AUD	$f_{ripple} = 70$ Hz; see Fig.6 for AM	20	26	–	dB
		for FM	14	20	–	dB
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC ₁ ; SC ₂ off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; PC/SC ₁ = 20 dB; SC ₂ off; note 6	–	75	–	mV
Reference frequency						
f_{ref}	reference signal frequency	note 7	–	4	–	MHz
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal	80	–	400	mV

Notes

1. Values of video and sound parameters can be decreased at $V_P = 4.5$ V.
2. For applications without I²C-bus, the time constant ($R \times C$) at the supply must be >1.2 μ s (e.g. 1 Ω and 2.2 μ F).
3. Condition: luminance range (5 steps) from 0 % to 100 %.
4. AC load: $C_L < 20$ pF and $R_L > 1$ k Ω . The sound carrier frequencies (depending on the TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; $|H(s)|$ is the absolute value of transfer function).
5. S/N_W is the ratio of the black-to-white amplitude to the black level noise voltage (RMS value measured on pin CVBS). B = 5 MHz weighted in accordance with "CCIR 567".

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

6. The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^r \text{ V}$$

$$\text{and } r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}} (\text{dB}) + 6 \text{ dB} \pm 3 \text{ dB} \right)$$

where:

$\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}} (\text{dB})$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and $\pm 3 \text{ dB}$ is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

7. Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

6 BLOCK DIAGRAM

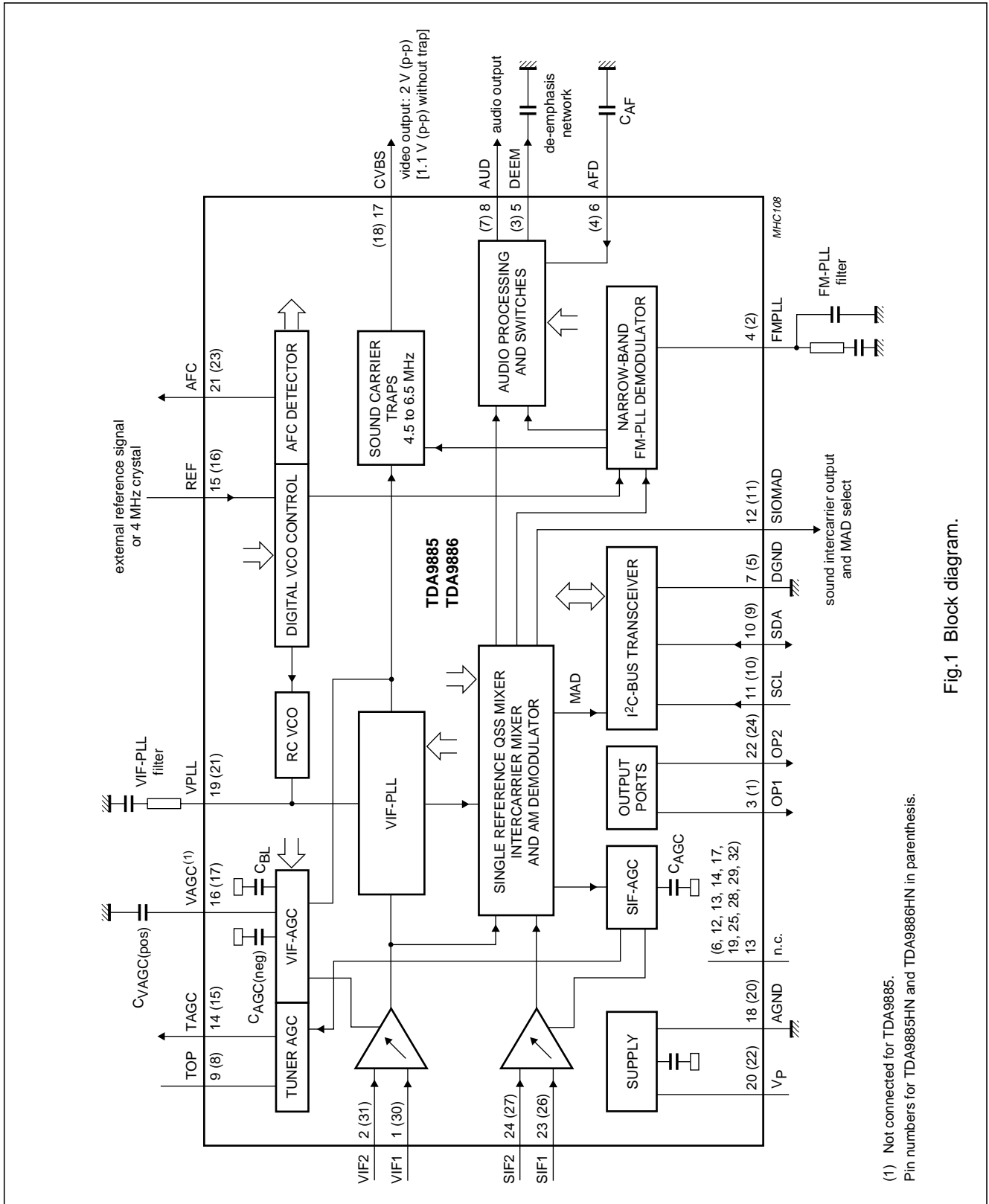


Fig.1 Block diagram.

(1) Not connected for TDA9885.
Pin numbers for TDA9885HN and TDA9886HN in parenthesis.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

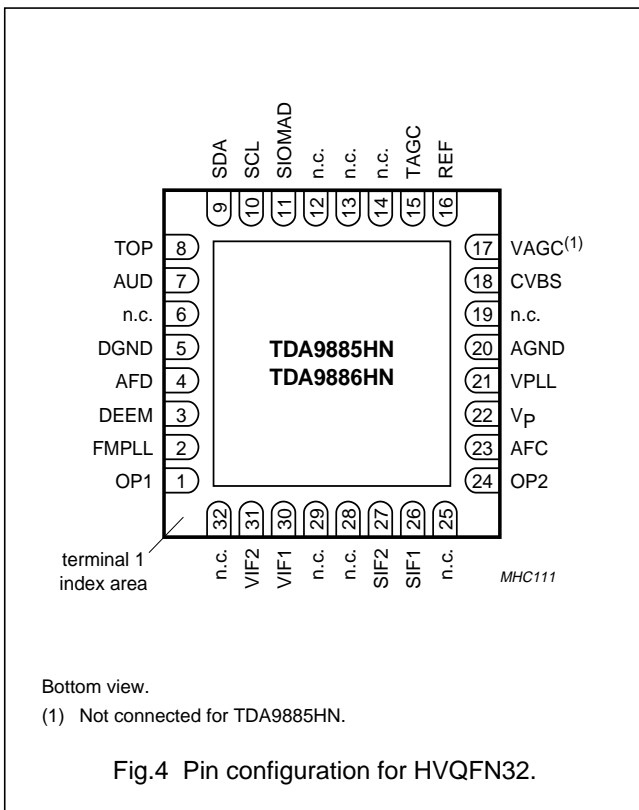
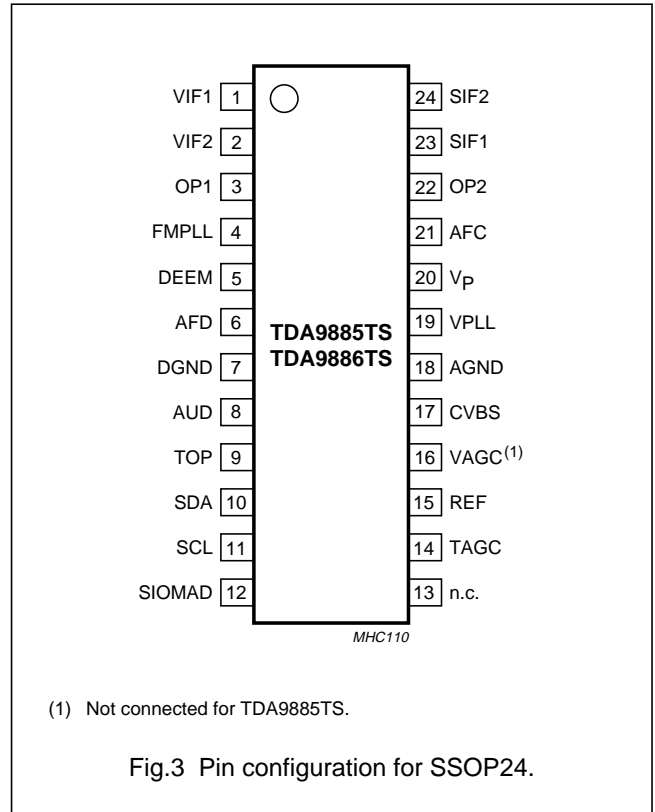
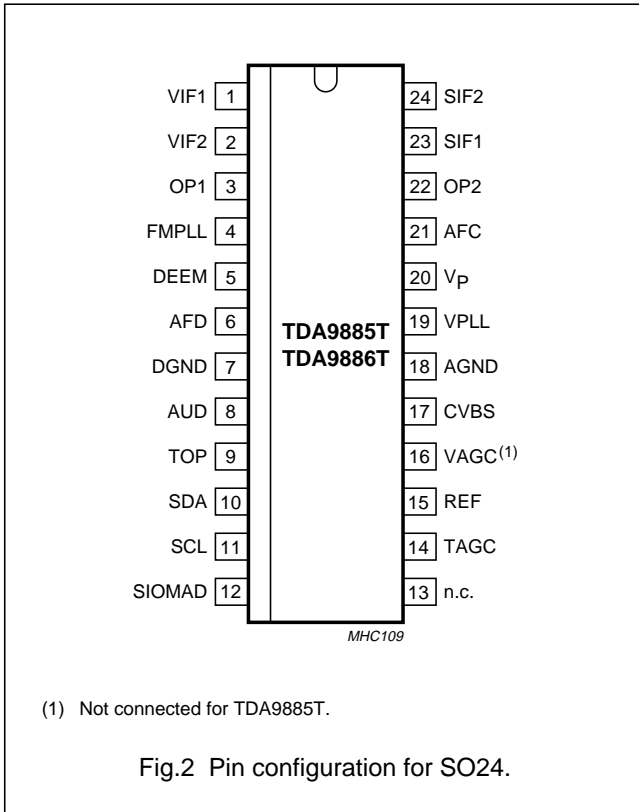
TDA9885; TDA9886

7 PINNING

SYMBOL	PIN				DESCRIPTION
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	–	–	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM-PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF decoupling input for capacitor
DGND	7	7	5	5	digital ground
n.c.	–	–	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	9	I ² C-bus data input and output
SCL	11	11	10	10	I ² C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	–	–	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	–	–	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	–	16	–	17	VIF-AGC for capacitor
n.c.	16	–	17	–	not connected
CVBS	17	17	18	18	composite video output
n.c.	–	–	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF-PLL for loop filter
V _P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	–	–	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	28	not connected
n.c.	–	–	29	29	not connected

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886



I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

8 FUNCTIONAL DESCRIPTION

Figure 1 shows the simplified block diagram of the device which comprises the following functional blocks:

- VIF amplifier
- Tuner AGC and VIF-AGC
- VIF-AGC detector
- Frequency Phase-Locked Loop (FPLL) detector
- VCO and divider
- AFC and digital acquisition help
- Video demodulator and amplifier
- Sound carrier trap
- SIF amplifier
- SIF-AGC detector
- Single reference QSS mixer
- AM demodulator
- FM demodulator and acquisition help
- Audio amplifier and mute time constant
- Internal voltage stabilizer
- I²C-bus transceiver and MAD (module address).

8.1 VIF amplifier

The VIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typically 66 dB. The differential input impedance is typically 2 k Ω in parallel with 3 pF.

8.2 Tuner AGC and VIF-AGC

This block adapts the voltages, generated at the VIF-AGC and SIF-AGC detectors, to the internal signal processing at the VIF and SIF amplifiers and performs the tuner AGC control current generation. The onset of the tuner AGC control current generation can be set either via the I²C-bus (see Table 13) or optionally by a potentiometer at pin TOP (in case that the I²C-bus information cannot be stored, related to the device). The presence of a potentiometer is automatically detected and the I²C-bus setting is disabled.

Furthermore, derived from the AGC detector voltage, a comparator is used to test if the corresponding VIF input voltage is higher than 200 μ V. This information can be read out via the I²C-bus (bit VIFLEV = 1).

8.3 VIF-AGC detector

Gain control is performed by sync level detection (negative modulation) or peak white detection (positive modulation).

For negative modulation, the sync level voltage is stored at an integrated capacitor by means of a fast peak detector. This voltage is compared with a reference voltage (nominal sync level) by a comparator which charges or discharges the integrated AGC capacitor for the generation of the required VIF gain. The time constants for decreasing or increasing the gain are nearly equal and the total AGC reaction time is fast to cope with 'aeroplane fluttering'.

For positive modulation, the white peak level voltage is compared with a reference voltage (nominal white level) by a comparator which charges (fast) or discharges (slow) the external AGC capacitor directly for the generation of the required VIF gain. The need of a very long time constant for VIF gain increase is because the peak white level may appear only once in a field. In order to reduce this time constant, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step controlled by the detected actual black level voltage. The threshold level for fast mode AGC is typically -6 dB video amplitude. The fast mode state is also transferred to the SIF-AGC detector for speed-up. In case of missing peak white pulses, the VIF gain increase is limited to typically +3 dB by comparing the detected actual black level voltage with a corresponding reference voltage.

8.4 FPLL detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier for removing the video AM.

During acquisition the frequency detector produces a current proportional to the frequency difference between the VIF and the VCO signals. After frequency lock-in the phase detector produces a current proportional to the phase difference between the VIF and the VCO signals. The currents from the frequency and phase detectors are charged into the loop filter which controls the VIF VCO and locks it to the frequency and phase of the VIF carrier.

For a positive modulated VIF signal, the charging currents are gated by the composite sync in order to avoid signal distortion in case of overmodulation. The gating depth is switchable via the I²C-bus.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

8.5 VCO and divider

The VCO of the VIF-FPLL operates as an integrated low radiation relaxation oscillator at double the picture carrier frequency. The control voltage, required to tune the VCO to double the picture carrier frequency, is generated at the loop filter by the frequency phase detector. The possible frequency range is 50 to 140 MHz (typical value).

The oscillator frequency is divided-by-two to provide two differential square wave signals with exactly 90 degrees phase difference, independent of the frequency, for use in the FPLL detectors, the video demodulator and the intercarrier mixer.

8.6 AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL.

The in-window and out-window control at the FM-PLL is additionally used to mute the audio stage (if auto mute is selected via the I²C-bus).

The working principle of the digital acquisition help is as follows. The PLL VCO output is connected to a down counter which has a predefined start value (standard dependent). The VCO frequency clocks the down counter for a fixed gate time. Thereafter, the down counter stop value is analysed. In case the stop value is higher (lower) than the expected value range, the VCO frequency is lower (higher) than the wanted lock-in window frequency range. A positive (negative) control current is injected into the PLL loop filter and consequently the VCO frequency is increased (decreased) and a new counting cycle starts.

The gate time as well as the control logic of the acquisition help circuit is dependent on the precision of the reference signal at pin REF. Operation as a crystal oscillator is possible as well as connecting this input via a serial capacitor to an external reference frequency, e.g. the tuning system oscillator.

The AFC signal is derived from the corresponding down counter stop value after a counting cycle. The last four bits are latched and can be read out via the I²C-bus (see Table 7). Also the digital-to-analog converted value is given as current at pin AFC.

8.7 Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The VIF signal is multiplied with the 'in phase' signal of the VIF-PLL VCO.

The demodulator output signal is fed into the video preamplifier via a level shift stage with integrated low-pass filter to achieve carrier harmonics attenuation.

The output signal of the preamplifier is fed to the VIF-AGC detector (see Section 8.3) and in the sound trap mode also fed internally to the integrated sound carrier trap (see Section 8.8). The differential trap output signal is converted and amplified by the following postamplifier. The video output level at pin CVBS is 2 V (p-p).

In the bypass mode the output signal of the preamplifier is fed directly through the postamplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10 % overall loss.

Noise clipping is provided in both cases.

8.8 Sound carrier trap

The sound carrier trap consists of a reference filter, a phase detector and the sound trap itself.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces a DC voltage by charging or discharging an integrated capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage controls the frequency position of the reference filter and the sound trap. So the accurate frequency position for the different standards is set by the sound carrier reference signal.

The sound trap itself is constructed of three separate traps to realize sufficient suppression of the first and second sound carriers.

8.9 SIF amplifier

The SIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typically 66 dB. The differential input impedance is typically 2 k Ω in parallel with 3 pF.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

8.10 SIF-AGC detector

SIF gain control is performed by the detection of the DC component of the AM demodulator output signal. This DC signal corresponds directly to the SIF voltage at the output of the SIF amplifier so that a constant SIF signal is supplied to the AM demodulator and to the single reference QSS mixer.

By switching the gain of the input amplifier of the SIF-AGC detector via the I²C-bus, the internal SIF level for FM sound is 5.5 dB lower than for AM sound. This is to adapt the SIF-AGC characteristic to the VIF-AGC characteristic. The adaptation is ideal for a picture-to-sound FM carrier ratio of 13 dB.

Via a comparator, the integrated AGC capacitor is charged or discharged for the generation of the required SIF gain. Due to AM sound, the AGC reaction time is slow ($f_c < 20$ Hz for the closed AGC loop). For reducing this AM sound time constant in the event of a decreasing IF amplitude step, the load current of the AGC capacitor is increased (fast mode) when the VIF-AGC detector (at positive modulation mode) operates in the fast mode too. An additional circuit (threshold approximately 7 dB) ensures a very fast gain reduction for a large increasing IF amplitude step.

8.11 Single reference QSS mixer

With the present system a high performance Hi-Fi stereo sound processing can be achieved. For a simplified application without a SIF SAW filter, the single reference QSS mixer can be switched to the intercarrier mode via the I²C-bus.

The single reference QSS mixer generates the 2nd FM TV sound intercarrier signal. It is realized by a linear multiplier which multiplies the SIF amplifier output signal and the VIF-PLL VCO signal (90 degrees output) which is locked to the picture carrier. In this way the QSS mixer operates as a quadrature mixer in the intercarrier mode and provides suppression of the low frequency video signals.

The QSS mixer output signal is fed internally via a high-pass and low-pass combination to the FM demodulator as well as via an operational amplifier to the intercarrier output pin SIOMAD.

8.12 AM demodulator

The amplitude modulated SIF amplifier output signal is fed both to a two-stage limiting amplifier that removes the AM and to a linear multiplier. The result of the multiplication of the SIF signal with the limiter output signal is AM demodulation (passive synchronous demodulator). The demodulator output signal is fed via a low-pass filter that attenuates the carrier harmonics and via the input amplifier of the SIF-AGC detector to the audio amplifier.

8.13 FM demodulator and acquisition help

The narrow-band FM-PLL detector consists of:

- Gain controlled FM amplifier and AGC detector
- Narrow-band PLL.

The intercarrier signal from the intercarrier mixer is fed to the input of an AC-coupled gain controlled amplifier with two stages. The gain controlled output signal is fed to the phase detector of the narrow-band FM-PLL (FM demodulator). For good selectivity and robustness against disturbance caused by the video signal, a high linearity of the gain controlled FM amplifier and of the phase detector as well as a constant signal level are required. The gain control is done by means of an 'in phase' demodulator for the FM carrier (from the output of the FM amplifier). The demodulation output is fed into a comparator for charging or discharging the integrated AGC capacitor. This leads to a mean value AGC loop to control the gain of the FM amplifier.

The FM demodulator is realized as a narrow-band PLL with an external loop filter, which provides the necessary selectivity (bandwidth approximately 100 kHz). To achieve good selectivity, a linear phase detector and a constant input level are required. The gain controlled intercarrier signal from the FM amplifier is fed to the phase detector. The phase detector controls via the loop filter the integrated low radiation relaxation oscillator. The designed frequency range is from 4 to 7 MHz.

The VCO within the FM-PLL is phase-locked to the incoming 2nd SIF signal, which is frequency modulated. As well as this, the VCO control voltage is superimposed by the AF voltage. Therefore, the VCO tracks with the FM of the 2nd SIF signal. So, the AF voltage is present at the loop filter and is typically 5 mV (RMS) for 27 kHz FM deviation. This AF signal is fed via a buffer to the audio amplifier.

The correct locking of the PLL is supported by the digital acquisition help circuit (see Section 8.6).

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

8.14 Audio amplifier and mute time constant

The audio amplifier consists of two parts:

- AF preamplifier
- AF output amplifier.

The AF preamplifier used for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator is 5 mV (RMS) for a frequency deviation of 27 kHz and is amplified by 30 dB. By the use of a DC operating point control circuit (with external capacitor C_{AF}), the AF preamplifier is decoupled from the PLL DC voltage. The low-pass characteristic of the amplifier reduces the harmonics of the sound intercarrier signal at the AF output terminal.

For FM sound a switchable de-emphasis network (with external capacitor) is implemented between the preamplifier and the output amplifier.

The AF output amplifier provides the required AF output level by a rail-to-rail output stage. A preceding stage makes use of an input selector for switching between FM sound, AM sound and mute state. The gain can be switched between 10 dB (normal) and 4 dB (reduced).

Switching to the mute state is controlled automatically, dependent on the digital acquisition help in case the VCO of the FM-PLL is not in the required frequency window. This is done by a time constant: fast for switching to the mute state and slow (typically 40 ms) for switching to the no-mute state.

All switching functions are controlled via the I²C-bus:

- AM sound, FM sound and forced mute
- Auto mute enable or disable
- De-emphasis off or on with 50 or 75 μ s
- Audio gain normal or reduced.

8.15 Internal voltage stabilizer

The band gap circuit internally generates a voltage of approximately 2.4 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

8.16 I²C-bus transceiver and module address

The device can be controlled via the 2-wire I²C-bus by a microcontroller. Two wires carry serial data (SDA) and serial clock (SCL) information between the devices connected to the I²C-bus.

The device has an I²C-bus slave transceiver with auto-increment. The circuit operates up to clock frequencies of 400 kHz.

A slave address is sent from the master to the slave receiver. To avoid conflicts in a real application with other devices providing similar or complementing functions, there are four possible slave addresses available. These Module Addresses (MADs) can be selected by connecting resistors on pin SIOMAD and/or pins SIF1 and SIF2 (see Fig.23). Pin SIOMAD relates with bit A0 and pins SIF1 and SIF2 relate with bit A3. The slave addresses of this device are given in Table 1.

The power-on preset value is dependent on the use of pin SIOMAD and can be chosen for 45.75 MHz NTSC as default (pin SIOMAD left open-circuit) or 58.75 MHz NTSC (resistor on pin SIOMAD). In this way the device can be used without the I²C-bus as an NTSC only device.

Remark: In case of using the device without the I²C-bus, then the rise time of the supply voltage after switching on power must be longer than 1.2 μ s.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

Table 1 Slave address detection

SLAVE ADDRESS	SELECTABLE ADDRESS BIT		RESISTOR ON PIN	
	A3	A0	SIF1 AND SIF2	SIOMAD
MAD1	0	1	no	no
MAD2	0	0	no	yes
MAD3	1	1	yes	no
MAD4	1	0	yes	yes

9 I²C-BUS CONTROL

9.1 Read format

Table 2 I²C-bus read format (slave transmits data)

S	BYTE 1								A	BYTE 2								AN	P
	A6	A5	A4	A3	A2	A1	A0	R/ \bar{W}		D7	D6	D5	D4	D3	D2	D1	D0		
	slave address							1		data									

Table 3 Explanation of Table 2

SYMBOL	FUNCTION
S	START condition, generated by the master
Slave address	see Table 4
R/ \bar{W} = 1	read command, generated by the master
A	acknowledge bit, generated by the slave
Data	8-bit data word, transmitted by the slave (see Table 5)
AN	acknowledge-not bit, generated by the master
P	STOP condition, generated by the master

The master generates an acknowledge when it has received the dataword READ. The master next generates an acknowledge, then slave begins transmitting the dataword READ, and so on until the master generates an acknowledge-not bit and transmits a STOP condition.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

9.1.1 SLAVE ADDRESS

The first module address MAD1 is the standard address (see Table 1).

Table 4 Slave addresses; notes 1 and 2

SLAVE ADDRESS		BIT						
NAME	VALUE (HEX)	A6	A5	A4	A3	A2	A1	A0
MAD1	43	1	0	0	0	0	1	1
MAD2	42	1	0	0	0	0	1	0
MAD3	4B	1	0	0	1	0	1	1
MAD4	4A	1	0	0	1	0	1	0

Notes

1. For MAD activation via external resistor: see Table 1 and Fig.23.
2. For applications without I²C-bus: see Tables 17 and 18.

9.1.2 DATA BYTE

Table 5 Data read register (status register)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
AFCWIN	VIFLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 6 Description of status register bits

BIT	VALUE	DESCRIPTION
AFCWIN	1	AFC window VCO in ± 1.6 MHz AFC window; note 1
	0	VCO out of ± 1.6 MHz AFC window
VIFLEV	1	VIF input level high level; VIF input voltage ≥ 200 μ V (typically)
	0	low level
CARRDET	1	FM carrier detection detection
	0	no detection
AFC[4:1]		Automatic frequency control see Table 7
PONR	1	Power-on reset after Power-on reset or after supply breakdown
	0	after a successful reading of the status register

Note

1. If no IF input is applied, then bit AFCWIN = 1 due to the fact that the VCO is forced to the AFC window border for fast lock-in behaviour.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

Table 7 Automatic frequency control bits; note 1

BIT				f_{VIF}
AFC4	AFC3	AFC2	AFC1	
0	1	1	1	$\leq (f_0 - 187.5 \text{ kHz})$
0	1	1	0	$f_0 - 162.5 \text{ kHz}$
0	1	0	1	$f_0 - 137.5 \text{ kHz}$
0	1	0	0	$f_0 - 112.5 \text{ kHz}$
0	0	1	1	$f_0 - 87.5 \text{ kHz}$
0	0	1	0	$f_0 - 62.5 \text{ kHz}$
0	0	0	1	$f_0 - 37.5 \text{ kHz}$
0	0	0	0	$f_0 - 12.5 \text{ kHz}$
1	1	1	1	$f_0 + 12.5 \text{ kHz}$
1	1	1	0	$f_0 + 37.5 \text{ kHz}$
1	1	0	1	$f_0 + 62.5 \text{ kHz}$
1	1	0	0	$f_0 + 87.5 \text{ kHz}$
1	0	1	1	$f_0 + 112.5 \text{ kHz}$
1	0	1	0	$f_0 + 137.5 \text{ kHz}$
1	0	0	1	$f_0 + 162.5 \text{ kHz}$
1	0	0	0	$\geq (f_0 + 187.5 \text{ kHz})$

Note

1. f_0 is the nominal frequency of f_{VIF} .

9.2 Write format**Table 8** I²C-bus write format (slave receives data); note 1

S	BYTE 1		A	BYTE 2		A	BYTE 3		A	BYTE n		A	P
	A6 to A0	R/ \bar{W}		A7 to A0			bits 7 to 0			bits 7 to 0			
	slave address	0		subaddress			data 1			data n			

Note

1. The auto-increment of the subaddress stops if the subaddress is 3.

Table 9 Explanation of Table 8

SYMBOL	FUNCTION
S	START condition, generated by the master
Slave address	see Table 4
$R/\bar{W} = 0$	write command, generated by the master
A	acknowledge bit, generated by the slave
Subaddress (SAD)	see Table 10
Data 1, data n	8-bit data words, transmitted by the master (see Tables 11, 12 and 14)
P	STOP condition

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

9.2.1 SUBADDRESS

If more than one data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 10.

Table 10 Definition of the subaddress (second byte after slave address); note 1

REGISTER	MSB							LSB	
	A7 ⁽²⁾	A6 ⁽³⁾	A5 ⁽³⁾	A4 ⁽³⁾	A3 ⁽³⁾	A2 ⁽³⁾	A1	A0	
SAD for switching mode	0	X	X	X	X	X	0	0	
SAD for adjust mode	0	X	X	X	X	X	0	1	
SAD for data mode	0	X	X	X	X	X	1	0	

Notes

1. X = don't care.
2. Bit A7 = 1 is not allowed.
3. Bits A6 to A2 will be ignored by the internal hardware.

9.2.2 DATA BYTE FOR SWITCHING MODE

Table 11 Bit description of SAD register for switching mode (SAD = 00)

BIT	VALUE	DESCRIPTION
B7	1	Output port 2 for SAW switching or monitoring high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
B6	1	Output port 1 for SAW switching or external input high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
B5	1	Forced audio mute on
	0	off
B4 and B3	00	TV standard modulation positive AM TV; note 1
	01	not used
	10	negative FM TV
	11	not used
B2	1	Carrier mode QSS mode
	0	intercarrier mode
B1	1	Auto mute of FM AF output active
	0	inactive

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

BIT	VALUE	DESCRIPTION
B0	1	Video mode (sound trap) sound trap bypass
	0	sound trap active

Note

- For positive AM TV choose 6.5 MHz for the second SIF.

9.2.3 DATA BYTE FOR ADJUST MODE

Table 12 Bit description of SAD register for adjust mode (SAD = 01)

BIT	VALUE	DESCRIPTION
C7	1	Audio gain –6 dB
	0	0 dB
C6	1	De-emphasis time constant 50 μ s
	0	75 μ s
C5	1	De-emphasis on
	0	off
C4 to C0		Tuner takeover point adjustment see Table 13

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

Table 13 Tuner takeover point adjustment bits

BIT					TOP ADJUSTMENT (dB)
C4	C3	C2	C1	C0	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0 ⁽¹⁾
0	1	1	1	1	-1
0	1	1	1	0	-2
0	1	1	0	1	-3
0	1	1	0	0	-4
0	1	0	1	1	-5
0	1	0	1	0	-6
0	1	0	0	1	-7
0	1	0	0	0	-8
0	0	1	1	1	-9
0	0	1	1	0	-10
0	0	1	0	1	-11
0	0	1	0	0	-12
0	0	0	1	1	-13
0	0	0	1	0	-14
0	0	0	0	1	-15
0	0	0	0	0	-16

Note

1. 0 dB is equal to 17 mV (RMS).

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

9.2.4 DATA BYTE FOR DATA MODE

Table 14 Bit description of SAD register for data mode (SAD = 10)

BIT	VALUE	DESCRIPTION
E7		VIF-AGC and port features dependent on bit E5; see Table 15
E6	1 0	L standard PLL gating gating in case of 36 % positive modulation gating in case of 0 % positive modulation
E5		VIF, SIF and tuner minimum gain dependent on bit E7; see Table 15
E4 to E2		Vision intermediate frequency selection see Table 16
E1 and E0	00 01 10 11	Sound intercarrier frequency selection (sound 2nd IF) $f_{FM} = 4.5$ MHz $f_{FM} = 5.5$ MHz $f_{FM} = 6.0$ MHz $f_{FM} = 6.5$ MHz; note 1

Note

- For positive modulation choose 6.5 MHz.

Table 15 Options in extended TV mode; bit B3 = 0 of SAD 00 register

FUNCTION	BIT E7 = 0		BIT E7 = 1	
	BIT E5 = 0	BIT E5 = 1	BIT E5 = 0	BIT E5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input ⁽¹⁾
Pin OP2	port function	port function	VIF-AGC output ⁽¹⁾	port function
Gain	normal gain	minimum gain	normal gain	external gain

Note

- The corresponding port function has to be disabled (set to 'high-impedance'); see Table 11 and Chapter 12, Table of Characteristics, note 12.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

Table 16 TV standard selection for VIF

VIDEO IF SELECT BITS			f_{VIF} (MHz)
E4	E3	E2	
0	0	0	58.75 ⁽¹⁾
0	0	1	45.75 ⁽¹⁾
0	1	0	38.9
0	1	1	38.0
1	0	0	33.9
1	0	1	33.4
1	1	0	not applicable
1	1	1	not applicable

Note

1. Pin SIOMAD can be used for the selection of the different NTSC standards without I²C-bus. With a resistor on pin SIOMAD, $f_{VIF} = 58.75$ MHz; without a resistor on pin SIOMAD, $f_{VIF} = 45.75$ MHz (NTSC-M).

Table 17 Data setting after power-on reset (default setting with a resistor on pin SIOMAD)

REGISTER	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	0	0	0

Table 18 Data setting after power-on reset (default setting without a resistor on pin SIOMAD)

REGISTER	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	1	0	0

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage		–	5.5	V
V _n	voltage on pins VIF1, VIF2, SIF1, SIF2, OP1, OP2, V _P , and FMPLL pin TAGC		0 0	V _P 8.8	V V
t _{sc}	short-circuit time to ground or V _P		–	10	s
T _{stg}	storage temperature		–25	+150	°C
T _{amb}	ambient temperature TDA9885T (SO24), TDA9885TS (SSOP24), TDA9886T (SO24) and TDA9886TS (SSOP24) TDA9885HN (HVQFN32) and TDA9886HN (HVQFN32)		–20 –20	+70 +85	°C °C
V _{es}	electrostatic discharge voltage on all pins	note 1	–400	+400	V
		note 2	–4000	+3500	V

Notes

- Machine model in accordance with SNW-FQ-302B: class C, discharging a 200 pF capacitor via a 0.75 µH series inductance.
- Human body model in accordance with SNW-FQ-302A: class 2, discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	TDA9885T (SO24)		76	K/W
	TDA9885TS (SSOP24)		118	K/W
	TDA9885HN (HVQFN32)		40	K/W
	TDA9886T (SO24)		76	K/W
	TDA9886TS (SSOP24)		118	K/W
	TDA9886HN (HVQFN32)		40	K/W

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

12 CHARACTERISTICS

$V_P = 5\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; see Table 20 for input frequencies; B/G standard is used for the specification ($f_{\text{PC}} = 38.9\text{ MHz}$; $f_{\text{SC}} = 33.4\text{ MHz}$; $\text{PC/SC} = 13\text{ dB}$; $f_{\text{mod}} = 400\text{ Hz}$); input level $V_{i(\text{VIF})} = 10\text{ mV (RMS)}$ (sync level for B/G; peak white level for L); IF input from $50\text{ }\Omega$ via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "CCIR line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Fig.23; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V_P)						
V _P	supply voltage	note 1	4.5	5.0	5.5	V
I _P	supply current		52	63	70	mA
P _{tot}	total power dissipation		–	305	385	mW
POWER-ON RESET						
V _{P(start)}	supply voltage for start of reset	decreasing supply voltage	2.5	3.0	3.5	V
V _{P(stop)}	supply voltage for end of reset	increasing supply voltage; I ² C-bus transmission enable	–	–	4.4	V
τ_P	time constant (R × C) for network at pin V _P	for applications without I ² C-bus	1.2	–	–	μs
VIF amplifier (pins VIF1 and VIF2)						
V _{i(VIF)(rms)}	VIF input voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	μV
V _{i(max)(rms)}	maximum input voltage (RMS value)	+1 dB video at output	150	190	–	mV
V _{i(ovl)(rms)}	overload input voltage (RMS value)	note 2	–	–	440	mV
$\Delta V_{\text{IF(int)}}$	internal IF amplitude difference between picture and sound carrier	within AGC range; $\Delta f = 5.5\text{ MHz}$	–	0.7	–	dB
G _{VIF(cr)}	VIF gain control range	see Fig.7	60	66	–	dB
B _{VIF(–3dB)(ll)}	lower limit –3 dB VIF bandwidth		–	15	–	MHz
B _{VIF(–3dB)(ul)}	upper limit –3 dB VIF bandwidth		–	80	–	MHz
R _{i(dif)}	differential input resistance	note 3	–	2	–	k Ω
C _{i(dif)}	differential input capacitance	note 3	–	3	–	pF
V _I	DC input voltage		–	1.93	–	V
FPLL and true synchronous video demodulator; note 4						
f _{VCO(max)}	maximum oscillator frequency for carrier regeneration	$f = 2f_{\text{PC}}$	120	140	–	MHz
f _{VIF}	vision carrier operating frequencies	see Table 14	–	33.4	–	MHz
			–	33.9	–	MHz
			–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF} ; see Fig.10	–	± 2.3	–	MHz
t_{acq}	acquisition time	BL = 70 kHz; note 5	–	–	30	ms
$V_{i(lock)(rms)}$	input voltage sensitivity for PLL to be locked (RMS value)	measured on pins VIF1 and VIF2; maximum IF gain	–	30	70	μV
$T_{cy(DAH)}$	cycle time of digital acquisition help		–	64	–	μs
$K_{O(VIF)}$	VIF VCO steepness	definition: $\Delta f_{VIF}/\Delta V_{VPLL}$	–	20	–	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	definition: $\Delta I_{VPLL}/\Delta \phi_{VIF}$	–	23	–	$\mu A/rad$
Video output 2 V (pin CVBS)						
NORMAL MODE (SOUND CARRIER TRAP ACTIVE) AND SOUND CARRIER ON						
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Fig.5	1.7	2.0	2.3	V
ΔV_o	video output voltage difference	difference between L and B/G standard	–12	–	+12	%
V/S	ratio between video (black-to-white) and sync level		1.90	2.33	3.00	
V_{sync}	sync voltage level		1.0	1.2	1.4	V
$V_{clip(u)}$	upper video clipping voltage level		$V_P - 1.1$	$V_P - 1$	–	V
$V_{clip(l)}$	lower video clipping voltage level		–	0.7	0.9	V
R_o	output resistance	note 3	–	–	30	Ω
$I_{bias(int)}$	internal DC bias current for emitter-follower		1.5	2.0	–	mA
$I_{o(sink)(max)}$	maximum AC and DC output sink current		1	–	–	mA
$I_{o(source)(max)}$	maximum AC and DC output source current		3.9	–	–	mA
$\Delta V_{o(CVBS)}$	deviation of CVBS output voltage	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(bl)}$	black level tilt	negative modulation	–	–	1	%
$\Delta V_{o(bl)(v)}$	vertical black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only	–	–	3	%
G_{dif}	differential gain	"CCIR 330"; note 6 B/G standard	–	–	5	%
		L standard	–	–	7	%
ϕ_{dif}	differential phase	"CCIR 330"	–	2	4	deg
S/N _W	weighted signal-to-noise ratio	weighted in accordance with "CCIR 567"; see Fig.11; note 7	56	59	–	dB

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_{UW}	unweighted signal-to-noise ratio	note 7	47	51	–	dB
$\alpha_{IM(\text{blue})}$	intermodulation attenuation at 'blue'	see Fig.12; note 8 f = 1.1 MHz f = 3.3 MHz	58 58	64 64	– –	dB dB
$\alpha_{IM(\text{yellow})}$	intermodulation attenuation at 'yellow'	see Fig.12; note 8 f = 1.1 MHz f = 3.3 MHz	60 59	66 65	– –	dB dB
$\Delta V_{r(PC)(\text{rms})}$	residual picture carrier (RMS value)	fundamental wave and harmonics	–	2	5	mV
$\Delta f_{\text{unw}(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	3 % residual carrier; 50 % serration pulses; L standard; note 3	–	–	12	kHz
$\Delta\phi$	robustness for modulator imbalance	0 % residual carrier; 50 % serration pulses; L standard; L-gating = 0 %; note 3	–	–	3	%
α_H	suppression of video signal harmonics	$C_L < 20 \text{ pF}$; $R_L > 1 \text{ k}\Omega$; AC load; note 9a	35	40	–	dB
α_{spur}	suppression of spurious elements	note 9b	40	–	–	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	$f_{\text{ripple}} = 70 \text{ Hz}$; video signal; grey level; positive and negative modulation; see Fig.6	20	25	–	dB
M/N STANDARD INCLUDING KOREA; see Fig 13						
$B_{V(-3\text{dB})(\text{trap})}$	–3 dB video bandwidth including sound carrier trap	$f_{\text{trap}} = 4.5 \text{ MHz}$; note 10	3.95	4.05	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz	30	36	–	dB
$\alpha_{SC1(60\text{kHz})}$	attenuation at first sound carrier $f_{SC1} \pm 60 \text{ kHz}$	f = 4.5 MHz	21	27	–	dB
α_{SC2}	attenuation at second sound carrier	f = 4.724 MHz	21	27	–	dB
$\alpha_{SC2(60\text{kHz})}$	attenuation at second sound carrier $f_{SC2} \pm 60 \text{ kHz}$	f = 4.724 MHz	15	21	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	f = 3.58 MHz; see Fig.14	110	180	250	ns
B/G STANDARD; see Fig.15						
$B_{V(-3\text{dB})(\text{trap})}$	–3 dB video bandwidth including sound carrier trap	$f_{\text{trap}} = 5.5 \text{ MHz}$; note 10	4.90	5.00	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 5.5 MHz	30	36	–	dB
$\alpha_{SC1(60\text{kHz})}$	attenuation at first sound carrier $f_{SC1} \pm 60 \text{ kHz}$	f = 5.5 MHz	24	30	–	dB
α_{SC2}	attenuation at second sound carrier	f = 5.742 MHz	21	27	–	dB

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	$f = 5.742$ MHz	15	21	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	$f = 4.43$ MHz; see Fig.16	110	180	250	ns
I STANDARD; see Fig.17						
$B_{V(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	$f_{trap} = 6.0$ MHz; note 10	5.40	5.50	–	MHz
α_{SC1}	attenuation at first sound carrier	$f = 6.0$ MHz	26	32	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	$f = 6.0$ MHz	20	26	–	dB
α_{SC2}	attenuation at second sound carrier	$f = 6.55$ MHz	12	18	–	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	$f = 6.55$ MHz	10	15	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	$f = 4.43$ MHz	–	90	160	ns
D/K STANDARD; see Fig.18						
$B_{V(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	$f_{trap} = 6.5$ MHz; note 10	5.50	5.95	–	MHz
α_{SC1}	attenuation at first sound carrier	$f = 6.5$ MHz	26	32	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	$f = 6.5$ MHz	20	26	–	dB
α_{SC2}	attenuation at second sound carrier	$f = 6.742$ MHz	18	24	–	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	$f = 6.742$ MHz	13	18	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	$f = 4.28$ MHz	–	60	130	ns
Video output 1.1 V (pin CVBS)						
TRAP BYPASS MODE AND SOUND CARRIER OFF; note 11						
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Fig.5	0.95	1.10	1.25	V
V_{sync}	sync voltage level		1.35	1.5	1.6	V
$V_{clip(u)}$	upper video clipping voltage level		3.5	3.6	–	V
$V_{clip(l)}$	lower video clipping voltage level		–	0.9	1.0	V
$B_{V(-1dB)}$	–1 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ k Ω ; AC load	5	6	–	MHz
$B_{V(-3dB)}$	–3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ k Ω ; AC load	7	8	–	MHz

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_W	weighted signal-to-noise ratio	weighted in accordance with "CCIR 567"; see Fig.11; note 7	56	59	–	dB
S/N_{UW}	unweighted signal-to-noise ratio	note 7	48	52	–	dB
VIF-AGC; note 12						
$t_{\text{resp(inc)}}$	AGC response time to an increasing VIF step	negative modulation; 20 dB; note 13	–	4	–	ms
		positive modulation; 20 dB; note 13	–	2.6	–	ms
$t_{\text{resp(dec)}}$	AGC response time to a decreasing VIF step	negative modulation; 20 dB; note 13	–	3	–	ms
		positive modulation; 20 dB; note 13	–	890	–	ms
		L standard; fast mode	–	2.6	–	ms/dB
		L standard; normal mode; note 13	–	143	–	ms/dB
$\Delta V_{i(\text{VIF})}$	VIF amplitude step for activating AGC fast mode	L standard	–2	–6	–10	dB
V_{VAGC}	gain control voltage range	see Fig.7	0.8	–	3.5	V
CR_{stps}	control steepness	definition: $\Delta G_{\text{VIF}}/\Delta V_{\text{VAGC}}$; $V_{\text{VAGC}} = 2$ to 3 V	–	–80	–	dB/V
$V_{\text{th(VIF)}}$	threshold voltage for high level VIF input	see Tables 5 and 6	120	200	320	μ V
PIN VAGC						
$I_{\text{ch(max)}}$	maximum charge current	L standard	–	100	–	μ A
$I_{\text{ch(add)}}$	additional charge current	L standard: in the event of missing VITS pulses and no white video content	–	100	–	nA
I_{dch}	discharge current	L standard; normal mode	–	35	–	nA
		L standard; fast mode	–	1.8	–	μ A
Tuner AGC (pin TAGC); see Figs 7 to 9						
$V_{i(\text{VIF})(\text{start1})(\text{rms})}$	VIF input signal voltage for minimum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	$I_{\text{TAGC}} = 120 \mu\text{A}$; $R_{\text{TOP}} = 22 \text{ k}\Omega$ or no R_{TOP} and -15 dB via I ² C-bus (see Table 13)	–	2	5	mV
$V_{i(\text{VIF})(\text{start2})(\text{rms})}$	VIF input signal voltage for maximum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	$I_{\text{TAGC}} = 120 \mu\text{A}$; $R_{\text{TOP}} = 0 \Omega$ or no R_{TOP} and $+15$ dB via I ² C-bus (see Table 13)	45	90	–	mV

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
QV _{TOP}	tuner takeover point accuracy	I _{TAGC} = 120 μA; R _{TOP} = 10 kΩ or no R _{TOP} and 0 dB via I ² C-bus (see Table 13)	7	17	43	mV
ΔQV _{TOP} /ΔT	takeover point variation with temperature	I _{TAGC} = 120 μA	–	0.03	0.07	dB/K
V _o	permissible output voltage	from external source	–	–	8.8	V
V _{sat}	saturation voltage	I _{TAGC} = 450 μA	–	–	0.5	V
I _{sink}	sink current	no tuner gain reduction; V _{TAGC} = 8.8 V	–	–	0.75	μA
		maximum tuner gain reduction; V _{TAGC} = 1 V	450	600	750	μA
ΔG _{IF}	IF slip by automatic gain control	tuner gain current from 20 % to 80 %	3	5	8	dB
AFC circuit (pin AFC); see Fig.10; notes 14 and 15						
V _{sat(ul)}	upper limit saturation voltage		V _P – 0.6	V _P – 0.3	–	V
V _{sat(ll)}	lower limit saturation voltage		–	0.3	0.6	V
I _{o(source)}	output source current		160	200	240	μA
I _{o(sink)}	output sink current		160	200	240	μA
AFC _{stps}	AFC control steepness	definition: ΔI _{AFC} /Δf _{VIF}	0.85	1.05	1.25	μA/kHz
Qf _{VIF(a)}	analog accuracy of AFC circuit	I _{AFC} = 0; f _{REF} = 4 MHz	–20	–	+20	kHz
Qf _{VIF(d)}	digital accuracy of AFC circuit via I ² C-bus	I _{AFC} = 0; f _{REF} = 4 MHz; 1 digit = 25 kHz	–20 – 1 digit	–	+20 + 1 digit	kHz
SIF amplifier (pins SIF1 and SIF2)						
V _{i(SIF)(rms)}	SIF input voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin SIOMAD	–	30	70	μV
		AM mode; –3 dB at AF output pin AUD	–	70	100	μV
V _{i(max)(rms)}	maximum input voltage (RMS value)	FM mode; +1 dB at intercarrier output pin SIOMAD	50	70	–	mV
		AM mode; +1 dB at AF output pin AUD	80	140	–	mV
V _{i(ovl)(rms)}	overload input voltage (RMS value)	note 2	–	–	320	mV
G _{SIF(cr)}	SIF gain control range	FM and AM mode; see Fig.9	60	66	–	dB
B _{SIF(–3dB)(ll)}	lower limit –3 dB SIF bandwidth		–	15	–	MHz
B _{SIF(–3dB)(ul)}	upper limit –3 dB SIF bandwidth		–	80	–	MHz
R _{i(dif)}	differential input resistance	note 3	–	2	–	kΩ
C _{i(dif)}	differential input capacitance	note 3	–	3	–	pF
V _I	DC input voltage		–	1.93	–	V

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIF-AGC detector						
t_{resp}	AGC response time to an increasing or decreasing SIF step of 20 dB	FM or AM fast step				
		increasing	–	8	–	ms
		decreasing	–	25	–	ms
		AM slow step				
		increasing	–	80	–	ms
		decreasing	–	250	–	ms
Single reference QSS intercarrier mixer (pin SIOMAD)						
$V_{o(\text{intc})}(\text{rms})$	IF intercarrier output level (RMS value)	QSS mode; SC ₁ ; SC ₂ off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; PC/SC ₁ = 20 dB; SC ₂ off; note 16	–	75	–	mV
$B_{\text{intc}(-3\text{dB})(\text{ul})}$	upper limit –3 dB intercarrier bandwidth		12	15	–	MHz
$\Delta V_{r(\text{SC})}(\text{rms})$	residual sound carrier (RMS value)	fundamental wave and harmonics				
		QSS mode	–	2	5	mV
		intercarrier mode	–	2	5	mV
$\Delta V_{r(\text{PC})}(\text{rms})$	residual picture carrier (RMS value)	fundamental wave and harmonics				
		QSS mode	–	2	5	mV
		intercarrier mode	–	5	20	mV
α_{H}	suppression of video signal harmonics	intercarrier mode; $f_{\text{video}} = 5 \text{ MHz}$	35	40	–	dB
R_{O}	output resistance	note 3	–	–	30	Ω
V_{O}	DC output voltage		–	2	–	V
$I_{\text{bias}(\text{int})}$	internal DC bias current for emitter follower		0.90	1.15	–	mA
$I_{\text{o}(\text{sink})(\text{max})}$	maximum AC output sink current		0.6	0.8	–	mA
$I_{\text{o}(\text{source})(\text{max})}$	maximum AC output source current		0.6	0.8	–	mA
$I_{\text{o}(\text{source})}$	DC output source current	MAD2 activated; note 17	0.75	0.93	1.20	mA

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM-PLL demodulator ; notes 15 and 18 to 22						
SOUND INTERCARRIER OUTPUT (PIN SIOMAD)						
$V_{FM(rms)}$	IF intercarrier level for gain controlled operation of FM-PLL (RMS value)	corresponding PC/SC ratio at input pins VIF1 and VIF2 is 7 to 47 dB	3.2	–	320	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)		–	–	2	mV
$V_{FM(det)(rms)}$	IF intercarrier level for FM carrier detect (RMS value)	see Table 6	–	–	2.3	mV
f_{FM}	sound intercarrier operating FM frequencies	see Table 14	–	4.5	–	MHz
			–	5.5	–	MHz
			–	6.0	–	MHz
			–	6.5	–	MHz
AUDIO OUTPUT (PIN AUD)						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	25 kHz FM deviation; 75 μ s de-emphasis	400	500	600	mV
		27 kHz FM deviation; 50 μ s de-emphasis	430	540	650	mV
$V_{o(AF)(cl)(rms)}$	AF output clipping level (RMS value)	THD < 1.5 %	1.3	1.4	–	V
$\Delta V_{o(AF)}/\Delta T$	AF output voltage variation with temperature		–	3×10^{-3}	7×10^{-3}	dB/K
THD	total harmonic distortion		–	0.15	0.50	%
Δf_{AF}	frequency deviation	THD < 1.5 %; note 19	–	–	± 55	kHz
		–6 dB AF output via I ² C-bus; note 19	–	–	± 110	kHz
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter of Fig.23	80	100	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM-PLL only; 27 kHz FM deviation; 50 μ s de-emphasis	52	56	–	dB
		black picture; see Fig.19	50	56	–	dB
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics; without de-emphasis	–	–	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 μ s de-emphasis; AM: f = 1 kHz; m = 54 %	40	46	–	dB
$PSRR_{FM}$	power supply ripple rejection	$f_{ripple} = 70$ Hz; see Fig.6	14	20	–	dB

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM-PLL FILTER (PIN FMPLL)						
V _{loop}	DC loop voltage		1.5	–	3.3	V
I _{o(source)(PD)(max)}	maximum phase detector output source current		–	60	–	μA
I _{o(sink)(PD)(max)}	maximum phase detector output sink current		–	60	–	μA
I _{o(source)(DAH)}	output source current of digital acquisition help		–	55	–	μA
I _{o(sink)(DAH)}	output sink current of digital acquisition help		–	55	–	μA
t _{W(DAH)}	pulse width of digital acquisition help current		–	16	–	μs
T _{cy(DAH)}	cycle time of digital acquisition help		–	64	–	μs
K _{O(FM)}	VCO steepness	definition: $\Delta f_{FM}/\Delta V_{FMPLL}$	–	3.3	–	MHz/V
K _{D(FM)}	phase detector steepness	definition: $\Delta I_{FMPLL}/\Delta \phi_{FM}$	–	4	–	μA/rad
Audio amplifier						
DE-EMPHASIS NETWORK (PIN DEEM)						
R _o	output resistance	50 μs de-emphasis; see Table 12	4.4	5.0	5.6	kΩ
		75 μs de-emphasis; see Table 12	6.6	7.5	8.4	kΩ
V _{AF(rms)}	audio signal (RMS value)	f _{AF} = 400 Hz; V _{AUD} = 500 mV	–	170	–	mV
V _O	DC output voltage		–	2.37	–	V
AF DECOUPLING (PIN AFD)						
V _{dec}	DC decoupling voltage	dependent on f _{FM} intercarrier frequency	1.5	–	3.3	V
I _L	leakage current	ΔV _{O(AUD)} < ±50 mV	–	–	±25	nA
I _{ch(max)}	maximum charge current		1.15	1.50	1.85	μA
I _{dch(max)}	maximum discharge current		1.15	1.50	1.85	μA
AUDIO OUTPUT (PIN AUD)						
R _o	output resistance	note 3	–	–	300	Ω
V _{O(AUD)}	DC output voltage		–	2.37	–	V
R _L	load resistance	AC-coupled	10	–	–	kΩ
R _{L(DC)}	DC load resistance		100	–	–	kΩ
C _L	load capacitance		–	–	1.5	nF
B _{AF(-3dB)(ul)}	upper limit –3 dB AF bandwidth of audio amplifier		150	–	–	kHz
B _{AF(-3dB)(ll)}	lower limit –3 dB AF bandwidth of audio amplifier	note 20	–	–	20	Hz
α _{mute}	mute attenuation of AF signal	via I ² C-bus	70	75	–	dB

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{jump}	DC jump voltage for switching AF output to mute state or vice versa	activated by digital acquisition help or via I ² C-bus mute	–	±50	±150	mV
FM operation; notes 21 and 23						
INTERCARRIER AF PERFORMANCE; note 24						
S/N_W	weighted signal-to-noise ratio	PC/SC ratio is 21 to 27 dB at pins VIF1 and VIF2				
		black picture	50	56	–	dB
		white picture	45	51	–	dB
		6 kHz sine wave (black-to-white modulation)	40	46	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	35	40	–	dB
SINGLE REFERENCE QSS AF PERFORMANCE; notes 25 and 26						
$S/N_{W(SC1)}$	weighted signal-to-noise ratio for SC ₁	PC/SC ₁ ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); "CCIR 468"	40	–	–	dB
		black picture	53	58	–	dB
		white picture	50	53	–	dB
		6 kHz sine wave (black-to-white modulation)	44	48	–	dB
		250 kHz square wave (black-to-white modulation)	40	45	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	45	51	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	46	52	–	dB

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N _{W(SC2)}	weighted signal-to-noise ratio for SC ₂	PC/SC ₂ ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); "CCIR 468"	40	–	–	dB
		black picture	48	55	–	dB
		white picture	46	51	–	dB
		6 kHz sine wave (black-to-white modulation)	42	46	–	dB
		250 kHz square wave (black-to-white modulation)	29	34	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	44	50	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	45	51	–	dB
AM operation						
L STANDARD (PIN AUD); see Figs 20 and 21; note 27						
V _{O(AF)(rms)}	AF output voltage (RMS value)	54 % modulation	400	500	600	mV
THD	total harmonic distortion	54 % modulation	–	0.5	1.0	%
B _{AF(-3dB)}	–3 dB AF bandwidth		100	125	–	kHz
S/N _{W(AF)}	weighted signal-to-noise ratio of audio signal	in accordance with "CCIR 468"	45	50	–	dB
V _{O(AUD)}	DC potential voltage		–	2.37	–	V
PSRR _{AM}	power supply ripple rejection	see Fig.6	20	26	–	dB
Reference frequency input (pin REF)						
V _I	DC input voltage		2.3	2.6	2.9	V
R _i	input resistance	note 3	–	5	–	kΩ
R _{xtal}	resonance resistance of crystal	operation as crystal oscillator	–	–	200	Ω
C _x	pull-up/down capacitance	note 28	–	–	–	pF
f _{ref}	reference signal frequency	note 29	–	4	–	MHz
Δf _{ref}	tolerance of reference signal frequency	note 15	–	–	±0.1	%
V _{ref(rms)}	reference signal voltage (RMS value)	operation as input terminal	80	–	400	mV
R _{O(ref)}	output resistance of reference signal source		–	–	4.7	kΩ
C _K	decoupling capacitance to external reference signal source	operation as input terminal	22	100	–	pF

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus transceiver (pins SDA and SCL); notes 30 and 31						
f _{SCL}	SCL clock frequency		0	–	400	kHz
V _{IH}	HIGH-level input voltage		3	–	V _{CC}	V
V _{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I _{IH}	HIGH-level input current		–10	–	+10	μA
I _{IL}	LOW-level input current		–10	–	+10	μA
V _{OL}	LOW-level output voltage	I _{OL} = 3 mA	–	–	0.4	V
I _{o(sink)}	output sink current	V _P = 0 V	–	–	10	μA
I _{o(source)}	output source current	V _P = 0 V	–	–	10	μA
Output ports (pins OP1 and OP2); note 32						
V _{OL}	LOW-level output voltage	I _{OL} = 2 mA (sink current)	–	–	0.4	V
V _{OH}	HIGH-level output voltage		–	–	6	V
I _{o(sink)}	output sink current		–	–	2	mA
I _{o(sink/source)(max)}	maximum output sink or source current	pin OP2 functions as VIF-AGC output	–	–	10	μA

Notes

- Values of video and sound parameters can be decreased at V_P = 4.5 V.
- Level headroom for input level jumps during gain control setting.
- This parameter is not tested during the production and is only given as application information for designing the receiver circuit.
- Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formula:

$$BL_{-3dB} = \frac{1}{2\pi} K_O K_D R, \text{ valid for } d \geq 1.2$$

$$d = \frac{1}{2} R \sqrt{K_O K_D C},$$

where:

K_O is the VCO steepness $\left(\frac{\text{rad}}{\text{V}}\right)$ or $\left(2\pi\frac{\text{Hz}}{\text{V}}\right)$; K_D is the phase detector steepness $\left(\frac{\mu\text{A}}{\text{rad}}\right)$;

R is the loop resistor; C is the loop capacitor; BL_{-3dB} is the loop bandwidth for –3 dB; d is the damping factor.

- V_{i(VIF)} = 10 mV (RMS); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
- Condition: luminance range (5 steps) from 0 % to 100 %.
- S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value on pin CVBS). B = 5 MHz (B/G, I and D/K standard). Noise analyzer setting: 200 kHz high-pass and SC-trap switched on.
- The intermodulation figures are defined for:
 - f = 1.1 MHz (referenced to black and white signal) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 1.1 \text{ MHz}}\right) + 3.6 \text{ dB}$
 - f = 3.3 MHz (referenced to colour carrier) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 3.3 \text{ MHz}}\right)$

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

9. Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz.
 - a) Modulation Vestigial Side-Band (VSB); sound carrier off; $f_{\text{video}} > 0.5$ MHz.
 - b) Sound carrier on; $f_{\text{video}} = 10$ kHz to 10 MHz.
10. AC load; $C_L < 20$ pF and $R_L > 1$ k Ω . The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; $|H(s)|$ is the absolute value of transfer function).
11. The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).
12. If selected by the I²C-bus, the VIF-AGC voltage can be monitored at pin OP2, and pin OP1 can be used as input. In this case, both pins cannot be used for the normal port function.
13. The response time is valid for a VIF input level range from 200 μ V to 70 mV.
14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.10. The AFC slope (voltage per frequency) can be changed by resistors R1 and R2.
15. The tolerance of the reference frequency determines the accuracy of the VIF-AFC, FM demodulator centre frequency and maximum FM deviation.
16. The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(\text{intc})(\text{rms})} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^r \text{ V}$$

$$\text{and } r = \frac{1}{20} \times \left(\frac{V_{i(\text{SC})}}{V_{i(\text{PC})}} (\text{dB}) + 6 \text{ dB} \pm 3 \text{ dB} \right)$$

where:

$\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(\text{SC})}}{V_{i(\text{PC})}} (\text{dB})$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2

in dB, 6 dB is the correction term of internal circuitry and ± 3 dB is the tolerance of video output and intercarrier output $V_{o(\text{intc})(\text{rms})}$.

17. For normal operation (with the I²C-bus) no DC load at pin SIOMAD is allowed. The second module address (MAD2) will be activated by the application of a 2.2 k Ω resistor between pin SIOMAD and ground. If this MAD2 is activated, also the power-on set-up state activates a VIF frequency of 58.75 MHz.
18. SIF input level is 10 mV (RMS); VIF input level is 10 mV (RMS) unmodulated.
19. Measured with an FM deviation of 25 kHz and the typical AF output voltage of 500 mV (RMS). The AF output signal can be attenuated by 6 dB to 250 mV (RMS) via the I²C-bus. For handling a frequency deviation of more than 55 kHz, the AF output signal has to be reduced in order to avoid clipping (THD < 1.5 %).
20. The lower limit of the audio bandwidth depends on the value of the capacitor at pin AFD. A value of $C_{\text{AF}} = 470$ nF leads to $f_{\text{AF}(-3\text{dB})} \approx 20$ Hz and $C_{\text{AF}} = 220$ nF leads to $f_{\text{AF}(-3\text{dB})} \approx 40$ Hz.
21. For all S/N measurements the VIF modulator in use has to meet the following specifications:
 - a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.
 - b) QSS AF performance, measured with the television demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (at deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.
 - c) Picture-to-sound carrier ratio $\text{PC}/\text{SC}_1 = 13$ dB (transmitter).

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

22. Calculation of the loop filter parameters can be done approximately using the following formulae:

$$f_o = \frac{1}{2\pi} \sqrt{\frac{K_O K_D}{C_P}}$$

$$\vartheta = \frac{1}{2R \sqrt{K_O K_D C_P}}$$

$$BL_{-3dB} = f_o (1.55 - \vartheta^2)$$

The formulae are only valid under the following conditions:

$$\vartheta \leq 1 \text{ and } C_S > 5C_P$$

where:

K_O is the VCO steepness $\left(\frac{\text{rad}}{\text{V}}\right)$ or $\left(2\pi \frac{\text{Hz}}{\text{V}}\right)$;

K_D is the phase detector steepness $\left(\frac{\mu\text{A}}{\text{rad}}\right)$;

R is the loop resistor;

C_S is the series capacitor;

C_P is the parallel capacitor;

f_o is the natural frequency of PLL;

BL_{-3dB} is the loop bandwidth for -3 dB;

ϑ is the damping factor. For examples, see Table 19.

23. The PC/SC ratio is calculated as the addition of TV transmitter PC/SC₁ ratio and SAW filter PC/SC₁ ratio. This PC/SC ratio is necessary to achieve the S/N_W values as noted. A different PC/SC ratio will change these values.
24. Measurements taken with SAW filter G1984 (Siemens) for vision and sound IF (sound shelf: 14 dB). Picture-to-sound carrier ratio of transmitter PC/SC = 13 dB. Input level on pins VIF1 and VIF2 of $V_{i(\text{SIF})} = 10$ mV (RMS) sync level, 27 kHz FM deviation for sound carrier, $f_{AF} = 400$ Hz. Measurements in accordance with "CCIR 468". De-emphasis is 50 μs.
25. The QSS signal output on pin SIOMAD is analysed by a test demodulator TDA9820. The S/N ratio of this device is more than 60 dB, related to a deviation of ±27 kHz, in accordance with "CCIR 468".
26. Measurements taken with SAW filter K3953 for vision IF (suppressed sound carrier) and K9453 for sound IF (suppressed picture carrier). Input level $V_{i(\text{SIF})} = 10$ mV (RMS), 27 kHz (54 % FM deviation).
27. Measurements taken with SAW filter K9453 (Siemens) for AM sound IF (suppressed picture carrier).
28. The value of C_x determines the accuracy of the resonance frequency of the crystal. It depends on the type of crystal used.
29. Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.
30. The SDA and SCL lines will not be pulled down if V_{CC} is switched off.
31. The AC characteristics are in accordance with the I²C-bus specification for fast mode (maximum clock frequency is 400 kHz). Information about the I²C-bus can be found in the brochure "The I²C-bus and how to use it" (order number 9398 393 40011).
32. Port P1 and port P2 are open-collector outputs.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

Table 19 Examples to note 22 (FM-PLL filter)

BL _{-3dB} (kHz)	C _S (nF)	C _P (pF)	R (kΩ)	ϑ
100	10	390	5.6	0.5
160	10	150	9.1	0.5

Table 20 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	M/N STANDARD	L STANDARD	L ACCENT STANDARD	UNIT
VIF carrier	f _{PC}	38.9	45.75 or 58.75	38.9	33.9	MHz
SIF carrier	f _{SC1}	33.4	41.25 or 54.25	32.4	40.4	MHz
	f _{SC2}	33.158	–	–	–	MHz
Picture-to-sound carrier ratio	SC ₁	13	7	10	10	dB
	SC ₂	20	–	–	–	dB

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TDA9885; TDA9886

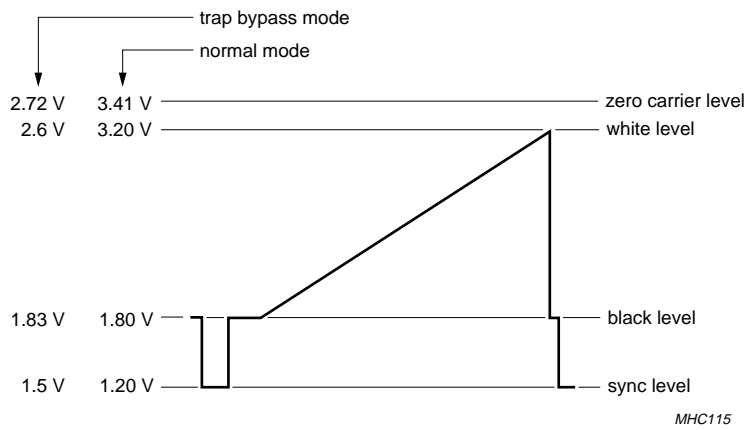


Fig.5 Typical video signal levels on output pin CVBS (sound carrier off).

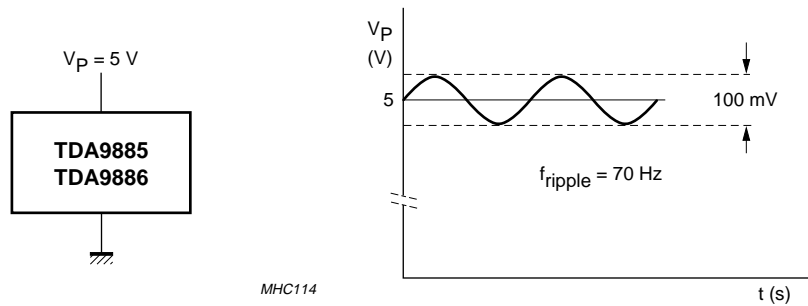
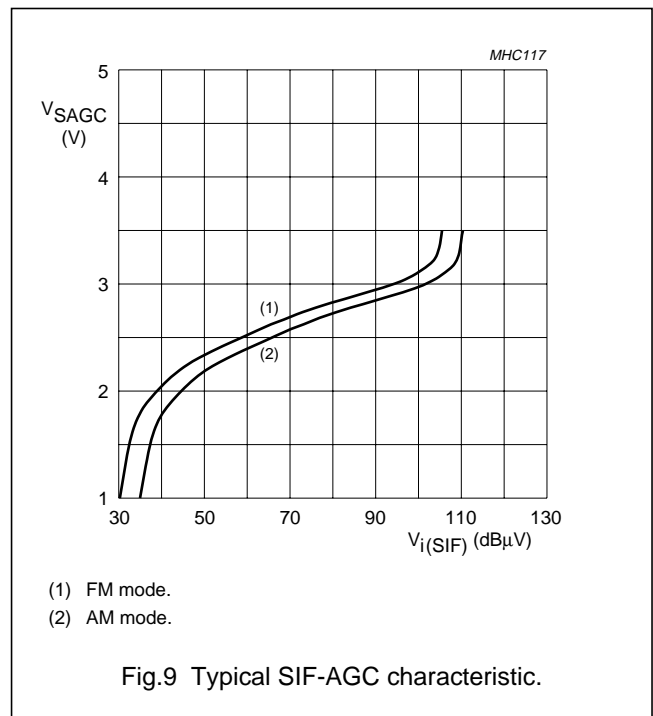
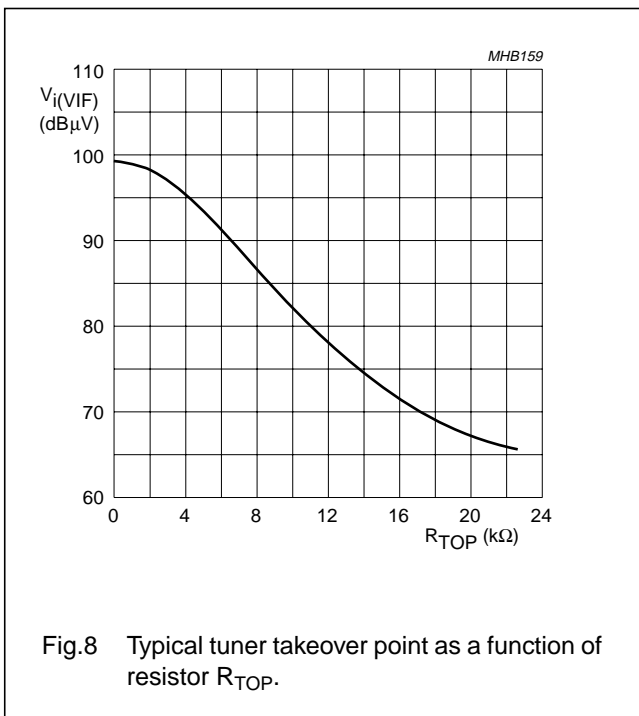
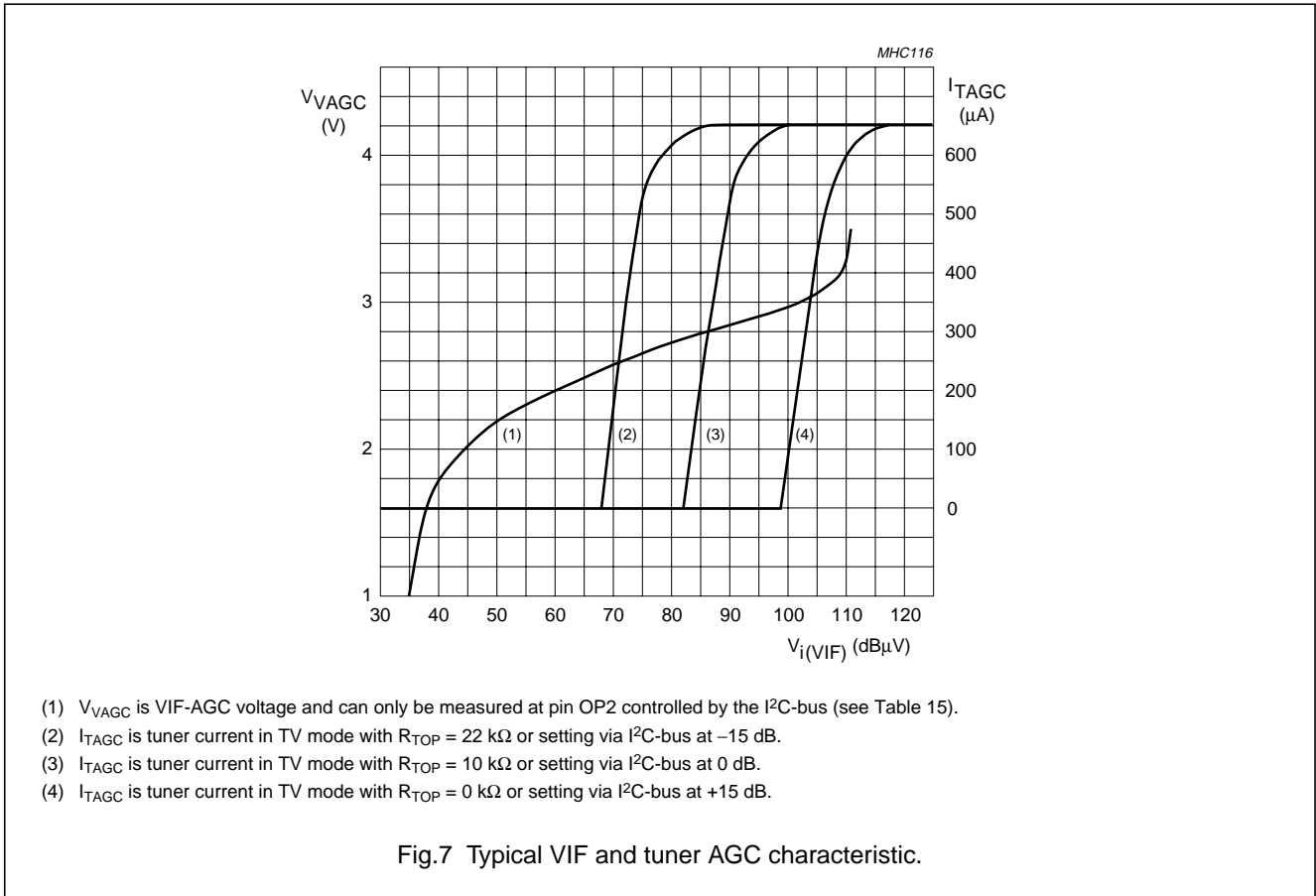


Fig.6 Ripple rejection condition.

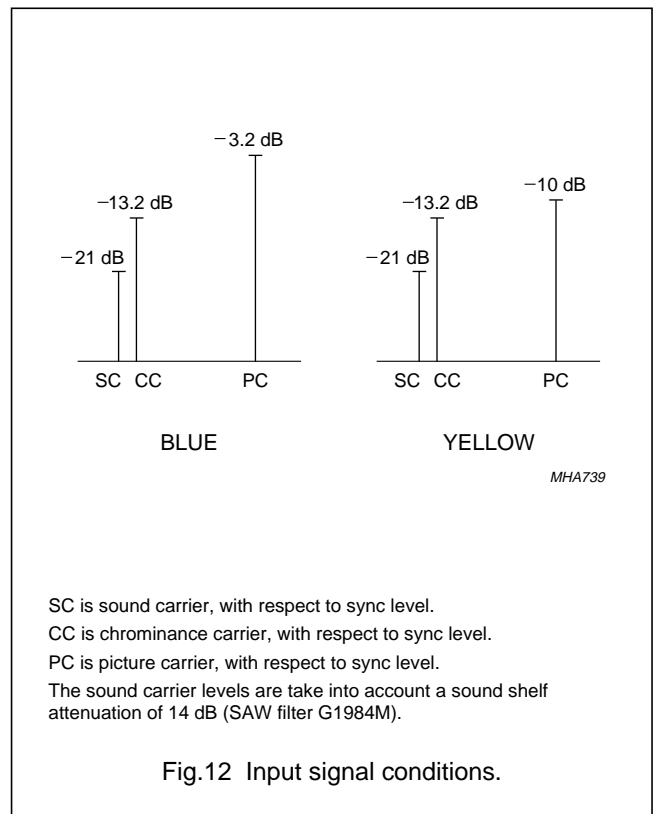
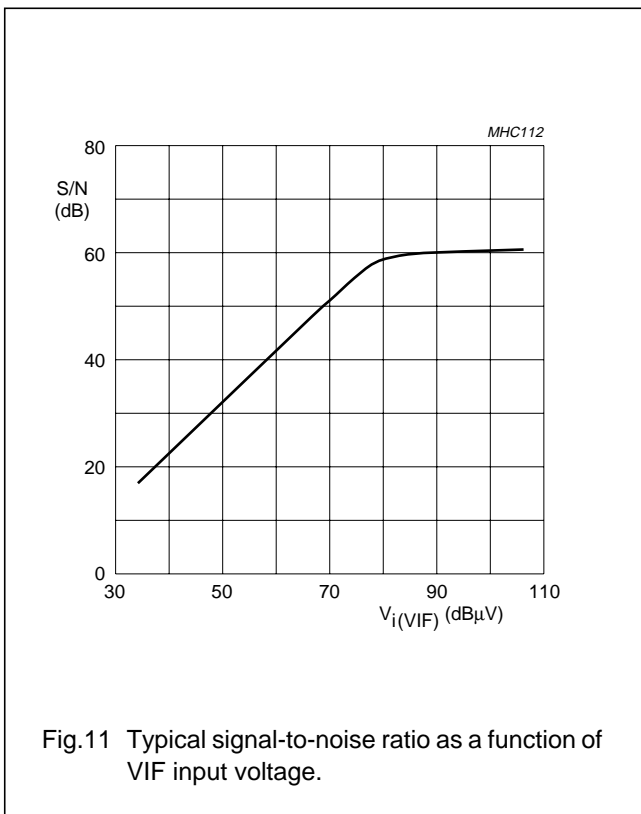
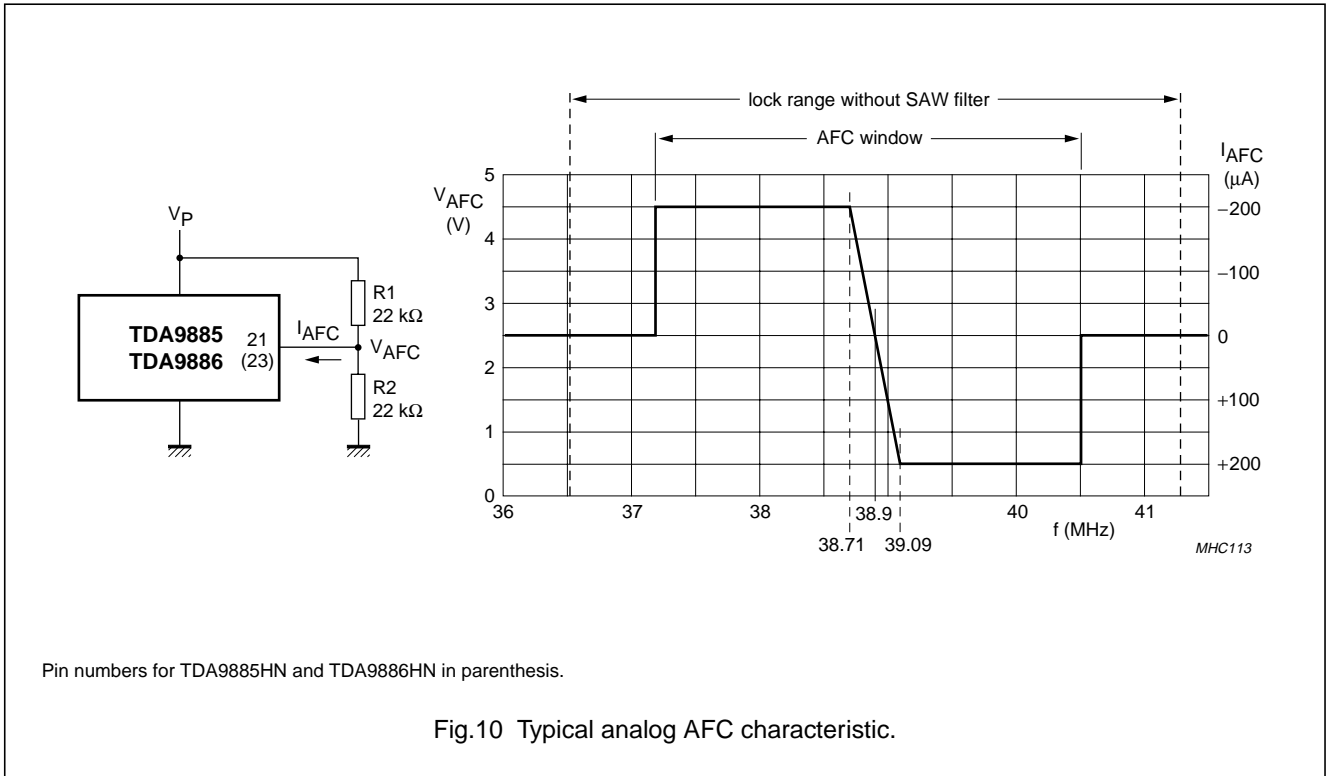
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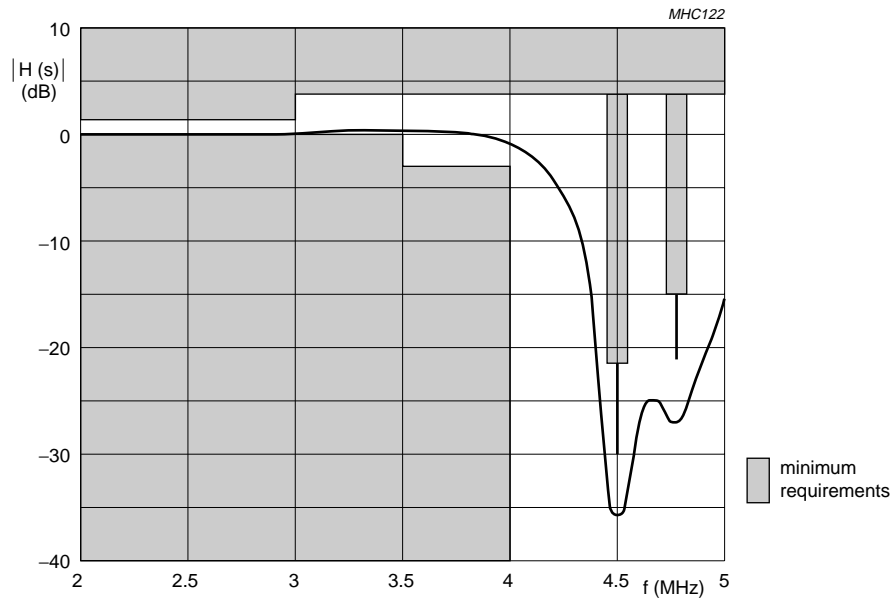
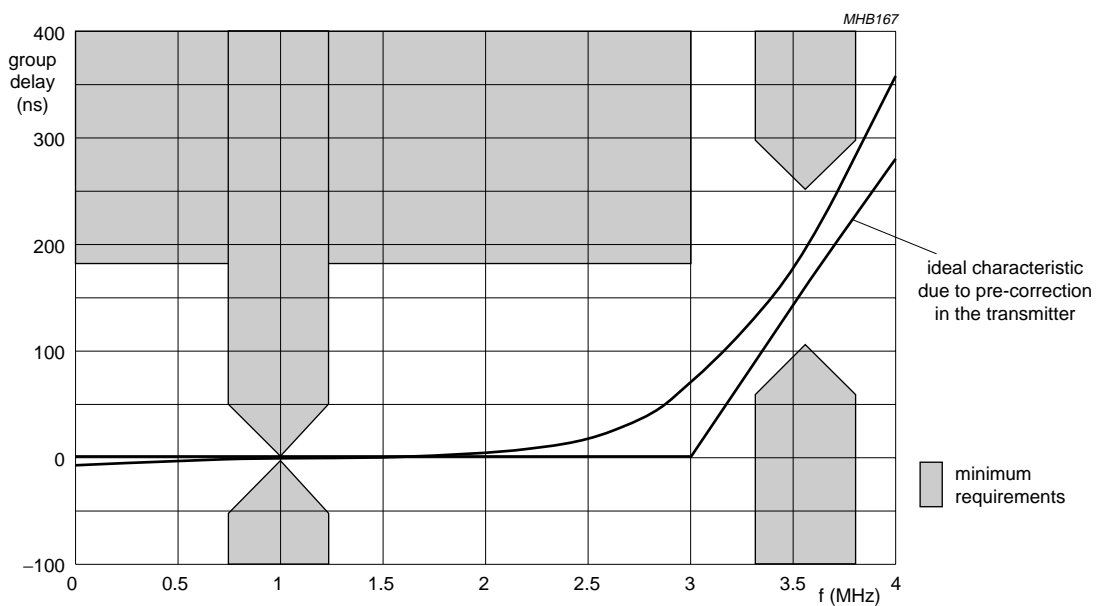


Fig.13 Typical amplitude response for sound trap at M/N standard (including Korea).



Overall delay is not shown, here the maximum ripple is specified.

Fig.14 Typical group delay for sound trap at M/N standard.

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TDA9885; TDA9886

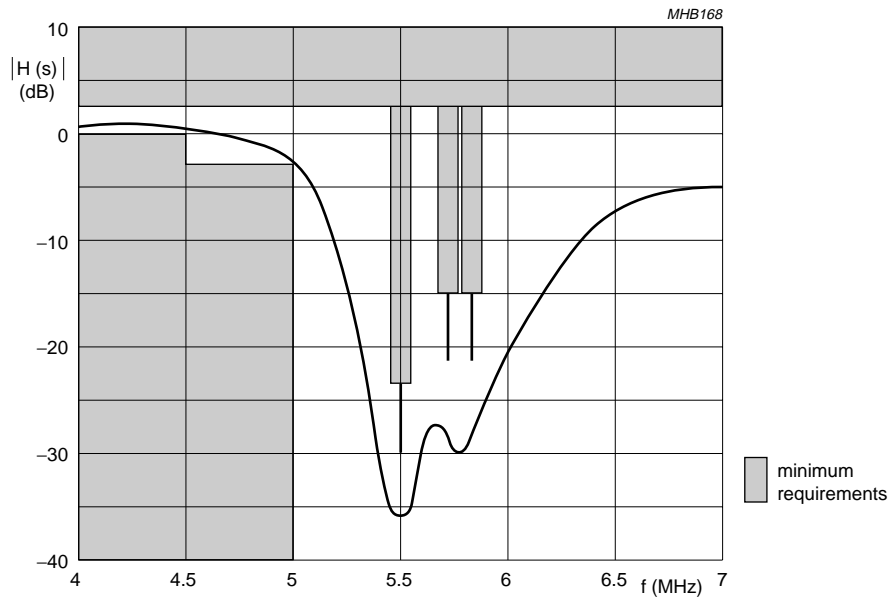
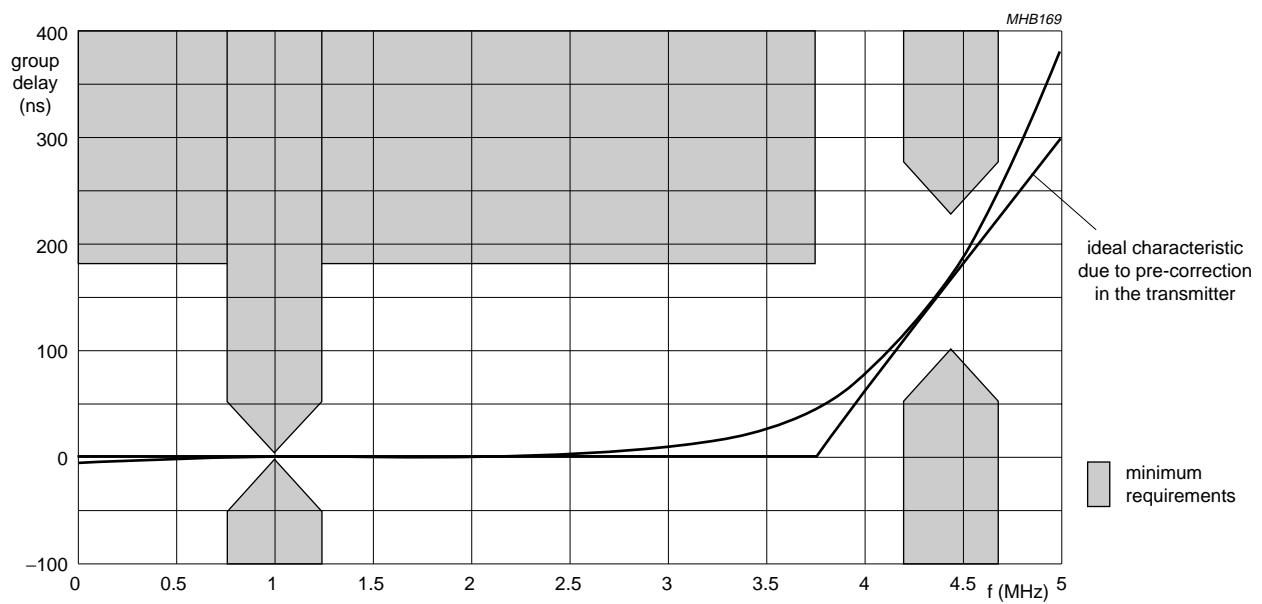


Fig.15 Typical amplitude response for sound trap at B/G standard.



Overall delay is not shown, here the maximum ripple is specified.

Fig.16 Typical group delay for sound trap at B/G standard.

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TDA9885; TDA9886

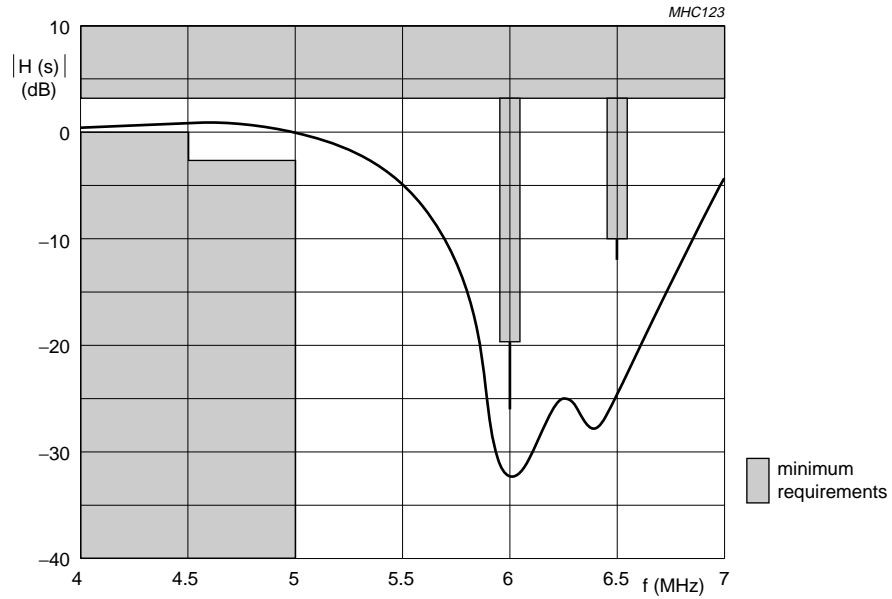


Fig.17 Typical amplitude response for sound trap at I standard.

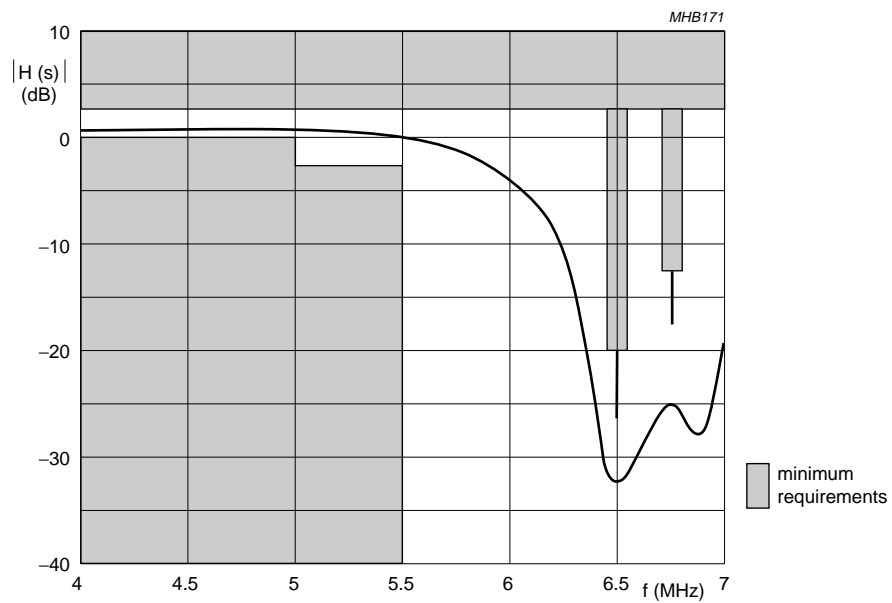
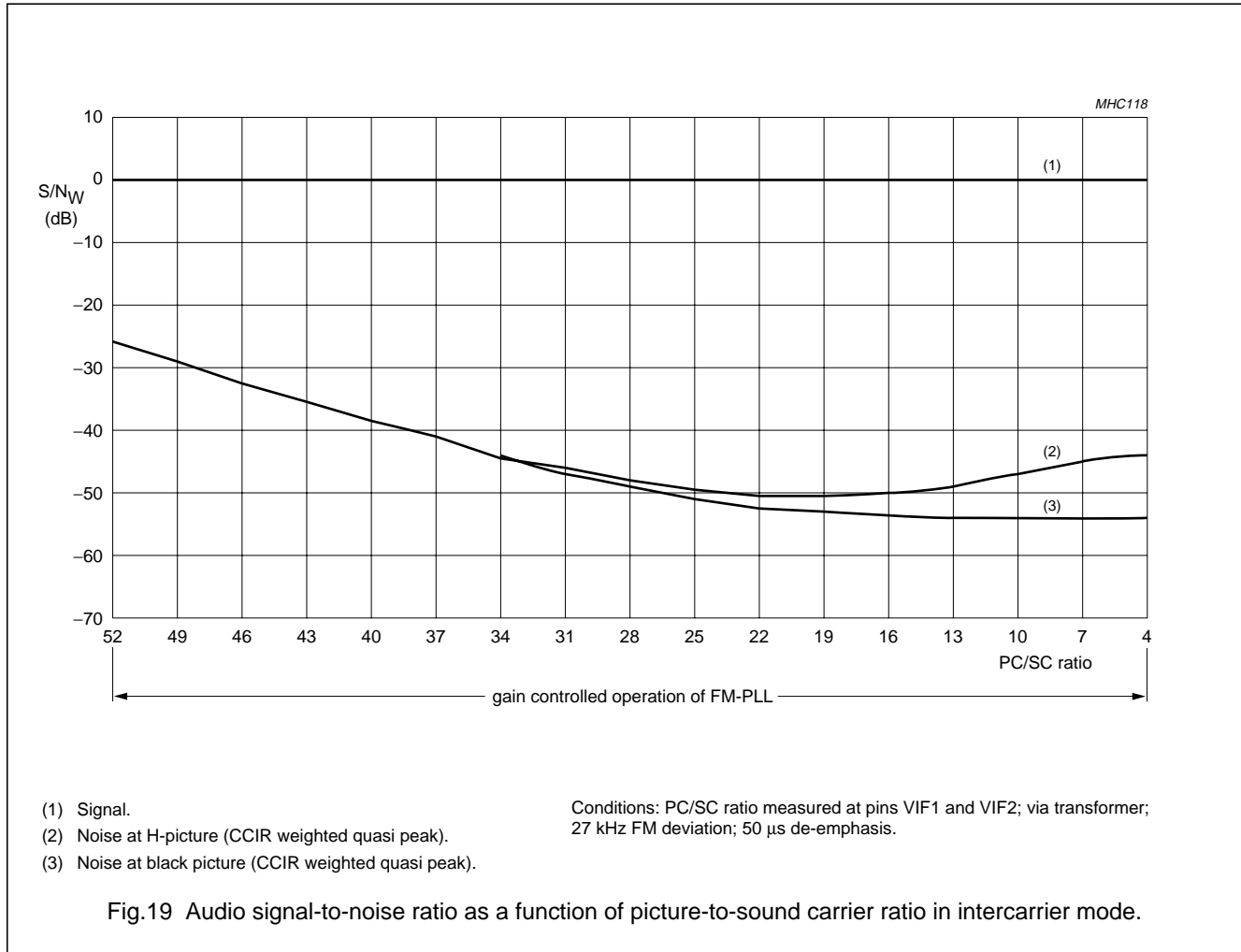


Fig.18 Typical amplitude response for sound trap at D/K standard.

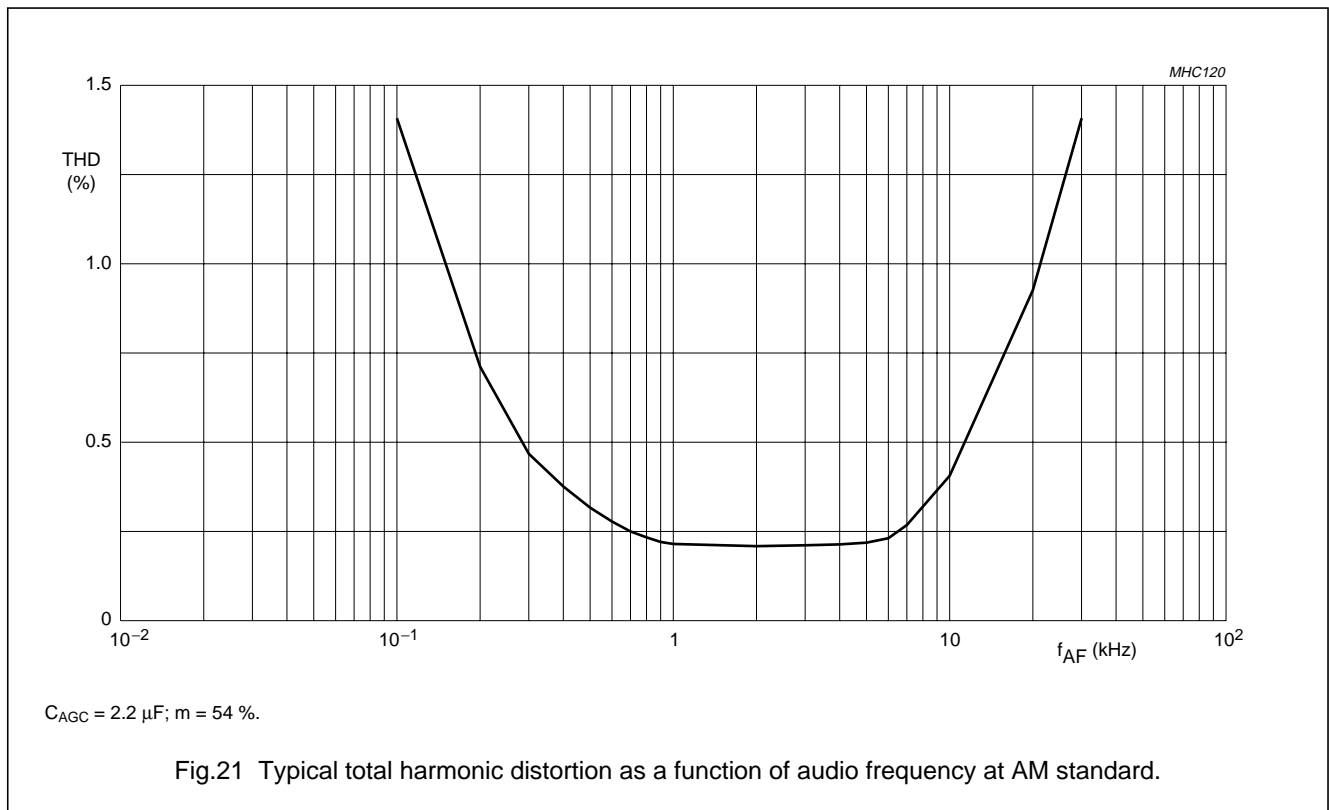
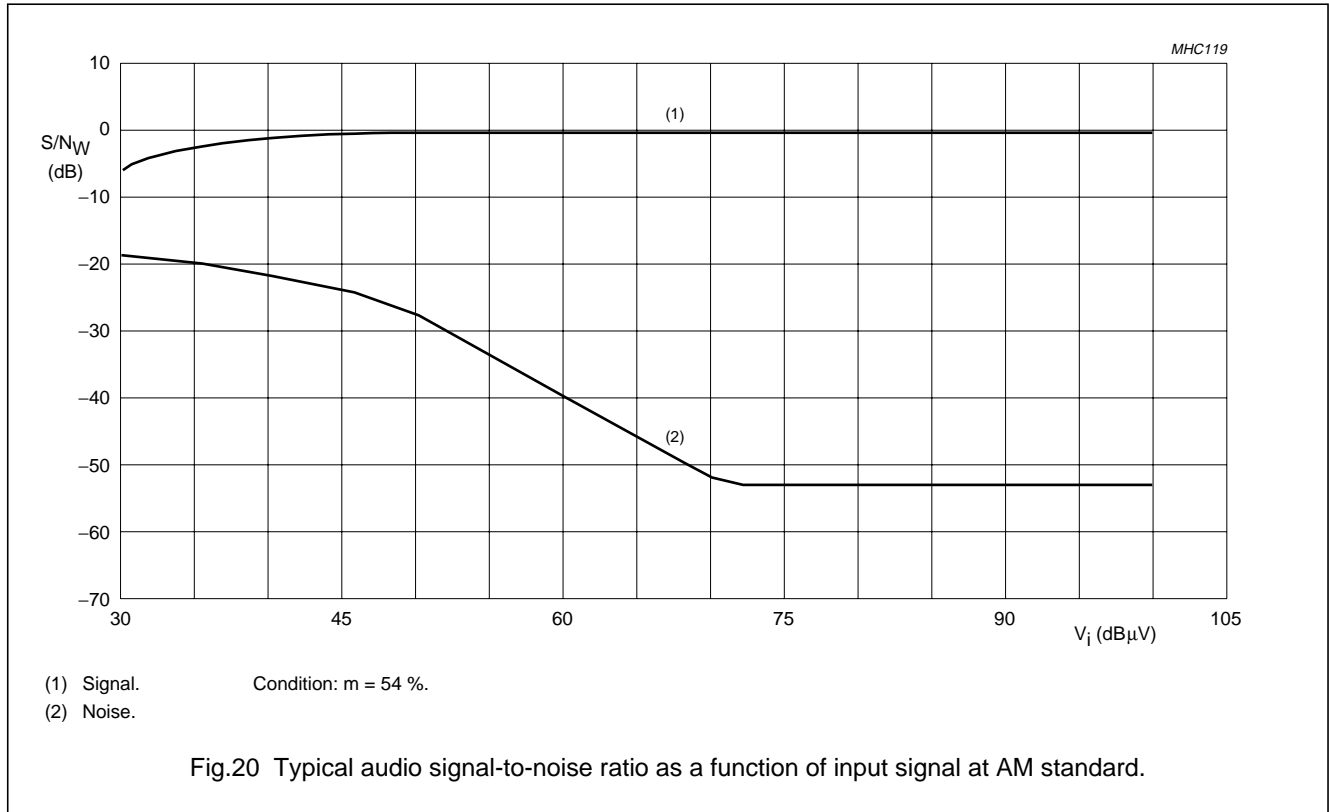
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TDA9885; TDA9886



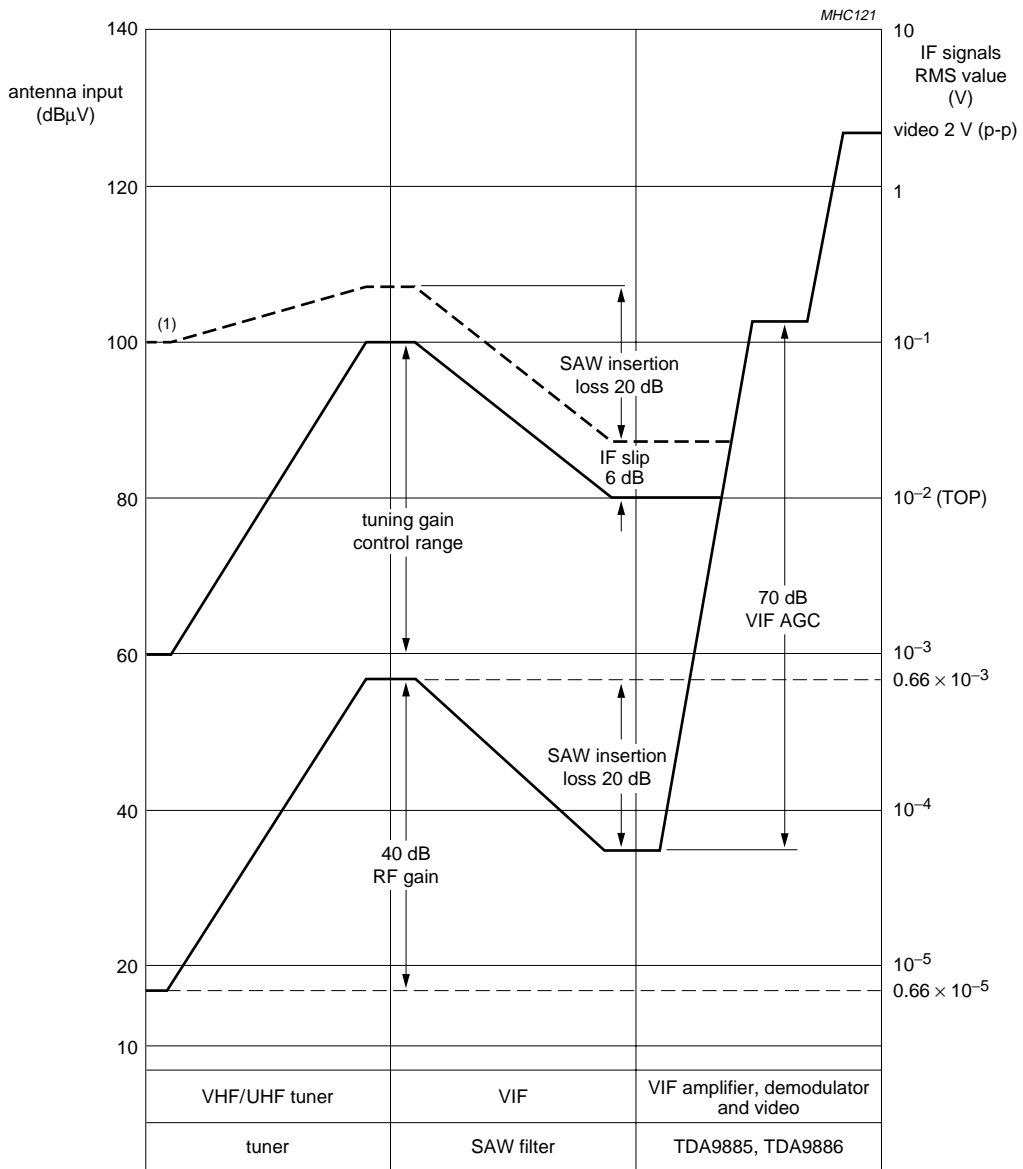
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(1) Depends on TOP.

Fig.22 Front-end level diagram.

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TDA9885; TDA9886

13 TEST AND APPLICATION INFORMATION

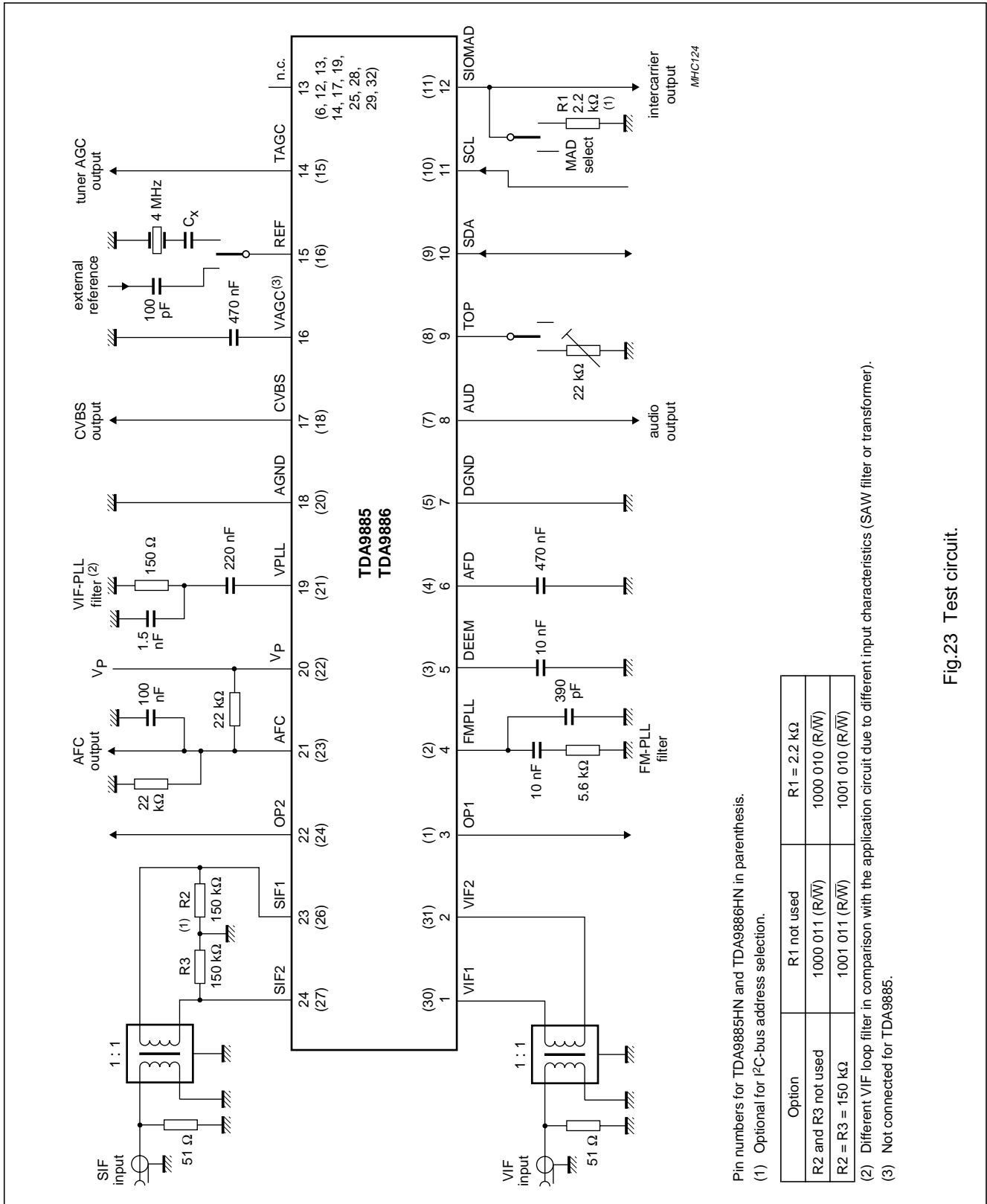
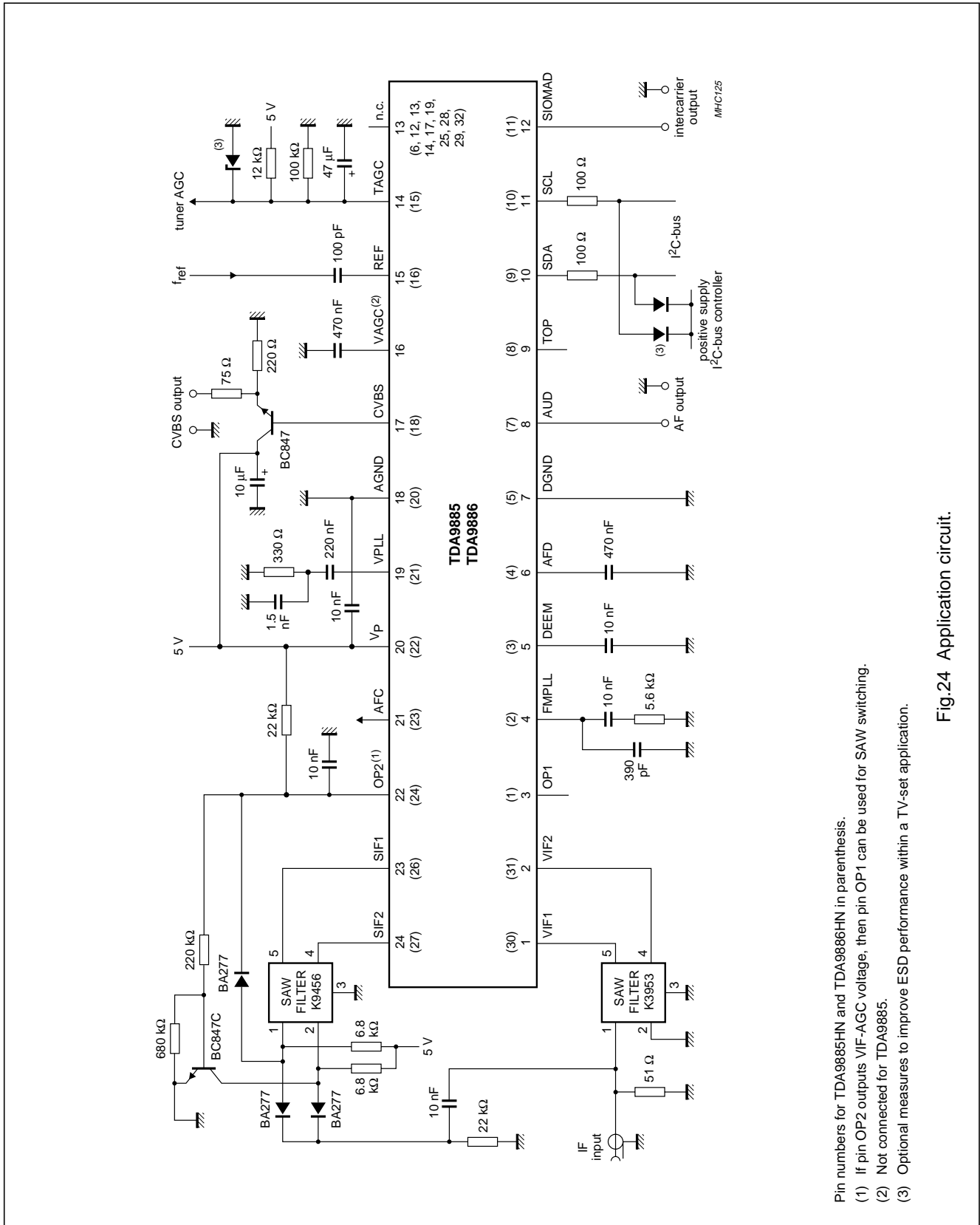


Fig.23 Test circuit.

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- Pin numbers for TDA9885HN and TDA9886HN in parenthesis.
- (1) If pin OP2 outputs VIF-AGC voltage, then pin OP1 can be used for SAW switching.
 - (2) Not connected for TDA9885.
 - (3) Optional measures to improve ESD performance within a TV-set application.

Fig.24 Application circuit.

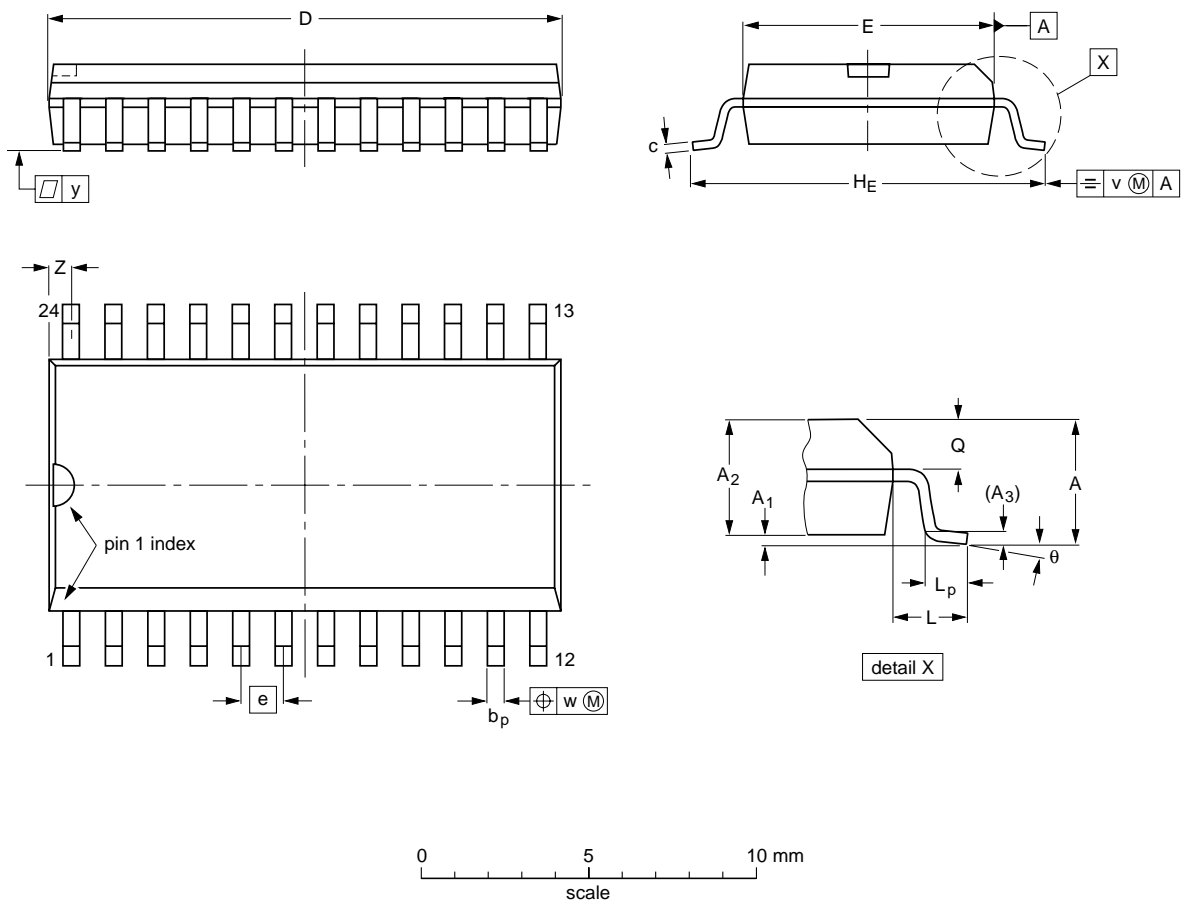
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TDA9885; TDA9886

14 PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

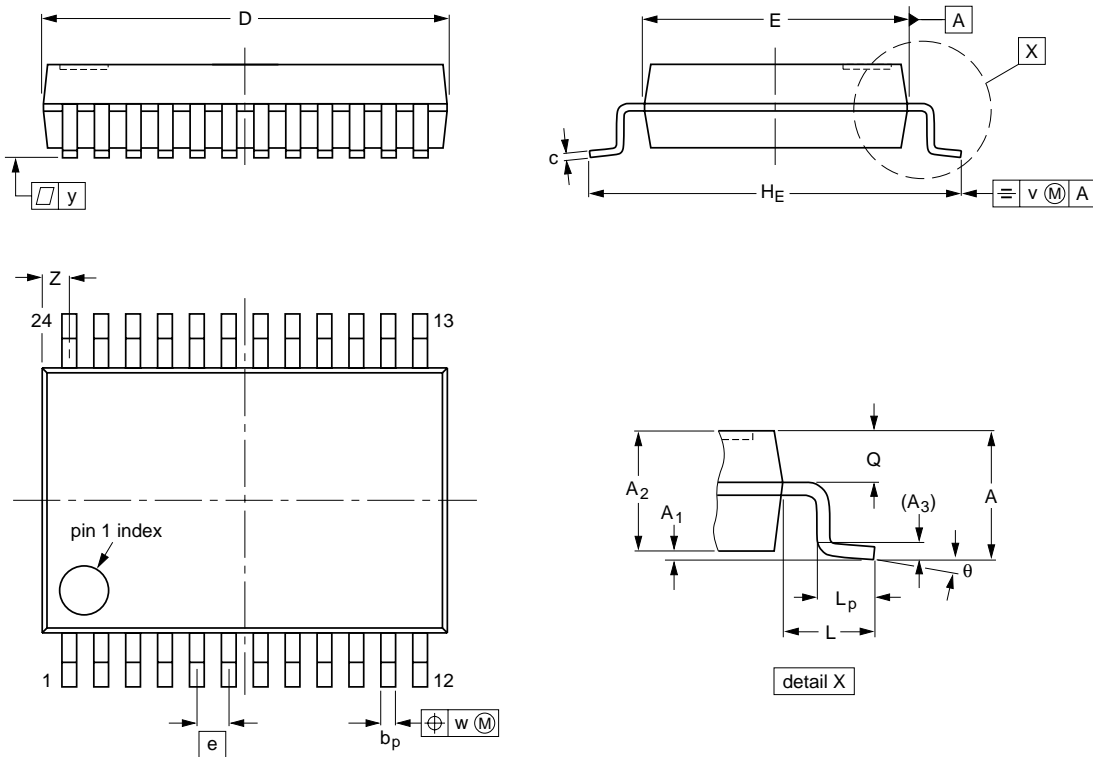
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT137-1	075E05	MS-013			99-12-27 03-02-19

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TDA9885; TDA9886

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

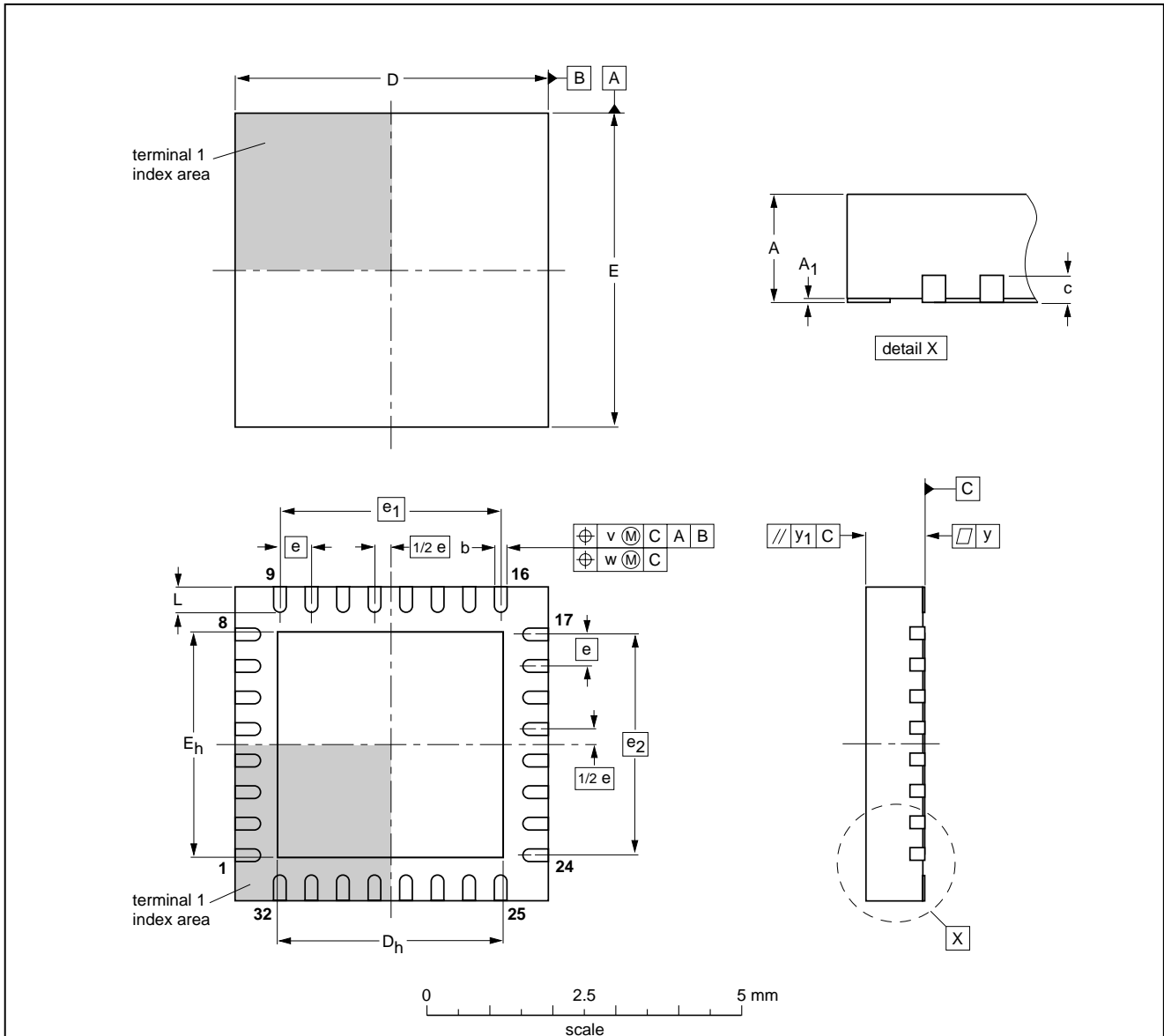
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	IEC	JEDEC	JEITA		
SOT340-1		MO-150			99-12-27 03-02-19

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

SOT617-3



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	e ₂	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-3	---	MO-220	---			-02-04-18- 02-10-22

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA and SSOP-T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, SSOP-T ⁽³⁾ , TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽⁴⁾	suitable
PLCC ⁽⁵⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁵⁾⁽⁶⁾	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ⁽⁷⁾	suitable
PMFP ⁽⁸⁾	not suitable	not suitable

Notes

- For more detailed information on the BGA packages refer to the "(LF)BGA Application Note" (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- Hot bar or manual soldering is suitable for PMFP packages.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

16 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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alignment-free IF-PLL demodulators**

TDA9885; TDA9886**19 PURCHASE OF PHILIPS I²C COMPONENTS**

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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