

# 31–35 GHz GaAs MMIC Driver Amplifier



AA035P3-00

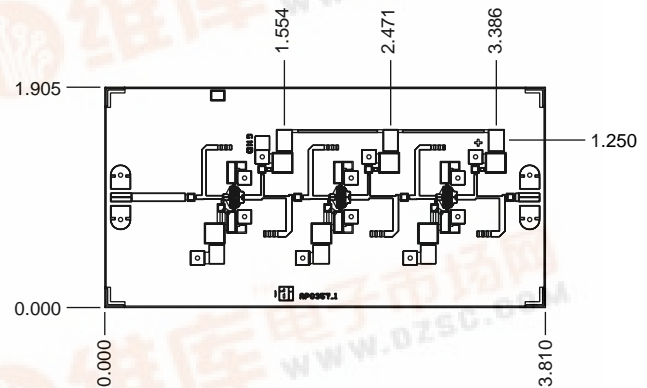
## Features

- Single Bias Supply Operation (5 V)
- 19 dB Typical Small Signal Gain
- 17 dBm Typical  $P_{1\text{ dB}}$  Output Power at 35 GHz
- 0.25  $\mu\text{m}$  Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

## Description

Alpha's three-stage reactively-matched Ka band GaAs MMIC driver amplifier has a typical  $P_{1\text{ dB}}$  of 17 dBm with 18 dB associated gain at 35 GHz. The chip uses Alpha's proven 0.25  $\mu\text{m}$  MESFET technology, which is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate solder or epoxy die attach processes. The amplifier is a self-bias design requiring a single positive drain bias to one of any three bonding sites. All chips are screened for S-parameters prior to shipment for guaranteed performance. A broad range of applications exist in both the high reliability and commercial areas where high gain and power are required.

## Chip Outline



Dimensions indicated in mm.

All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.  
Chip thickness = 0.1 mm.

## Absolute Maximum Ratings

Characteristic	Value
Operating Temperature ( $T_C$ )	-55°C to +90°C
Storage Temperature ( $T_{ST}$ )	-65°C to +150°C
Bias Voltage ( $V_D$ )	7 V <sub>DC</sub>
Power In ( $P_{IN}$ )	19 dBm
Junction Temperature ( $T_J$ )	175°C

## Electrical Specifications at 25°C ( $V_{DS} = 5\text{ V}$ )

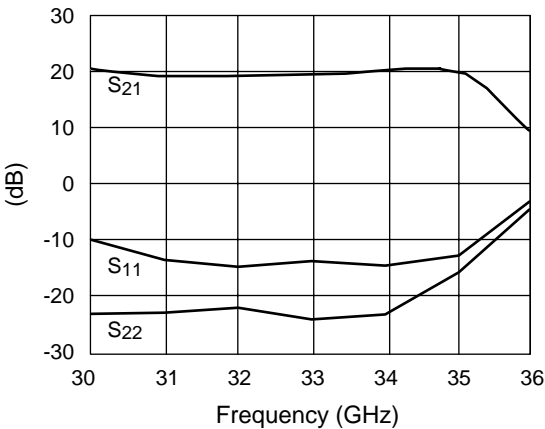
Parameter	Condition	Symbol	Min.	Typ. <sup>3</sup>	Max.	Unit
Drain Current		$I_{DS}$		275	350	mA
Small Signal Gain	F = 31–35 GHz	G	15	19		dB
Noise Figure <sup>1</sup>	F = 35 GHz	NF		10.5		dB
Input Return Loss	F = 31–35 GHz	$RL_I$		-14	-10	dB
Output Return Loss	F = 31–35 GHz	$RL_O$		-16	-10	dB
Output Power at 1 dB Gain Compression	F = 35 GHz	$P_{1\text{ dB}}$	15	17		dBm
Saturated Output Power	F = 35 GHz	$P_{SAT}$	16	19		dBm
Thermal Resistance <sup>2</sup>		$\Theta_{JC}$		66		°C/W

1. Not measured on a 100% basis.

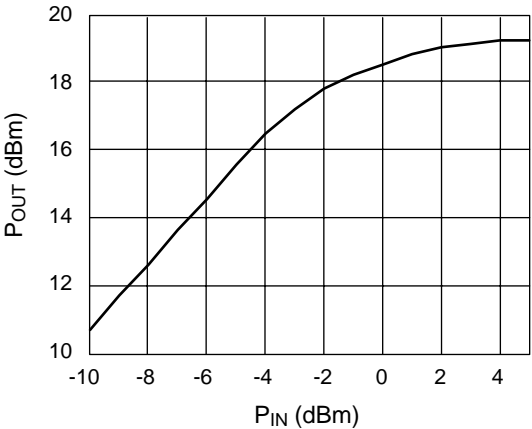
2. Calculated value based on measurement of discrete FET.

3. Typical represents the median parameter value across the specified frequency range for the median chip.

Typical Performance Data

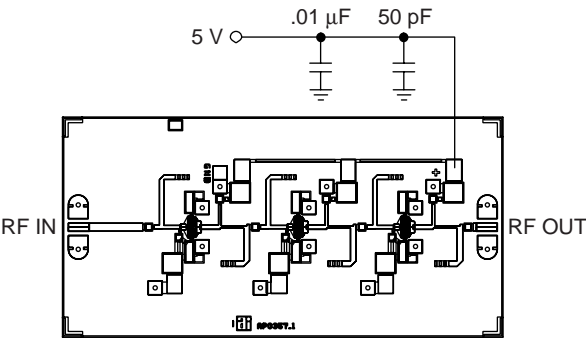


Typical Small Signal Performance  
S-Parameters ( $V_{DS} = 5\text{ V}$ )



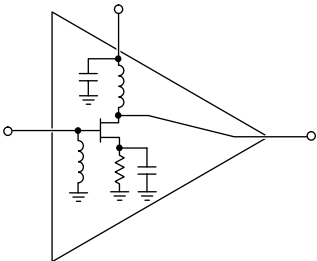
Output Characteristic as a  
Function of Input Drive Level  
( $F = 35\text{ GHz}$ ,  $V_{DS} = 5\text{ V}$ )

Bias Arrangement



For biasing on, adjust  $V_{DS}$  from zero to the desired value (4 V–6 V recommended). For biasing off, reverse the biasing on procedure.

Circuit Schematic



Detail A

