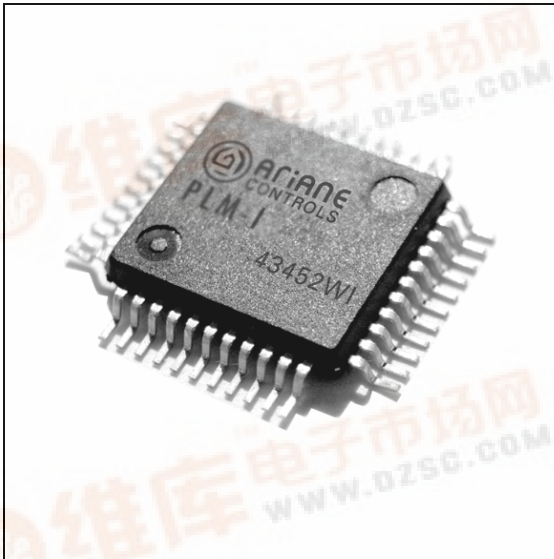# DATA SHEET

AC-PLM-1 Powerline Modem

DS01052 - January 2005 Revision March 2005

Features

- Very robust FSK demodulation technique, high noise immunity,
- Low-harmonic narrowband modulation
- Programmable baud rate from 100 bauds to 30,000 bauds
- Programmable carrier central frequency from 50 to 500 kHz
- Complete Medium Access Controls (MAC) logic on the device which can be disabled and implemented into the host to allow a better desired control
- CSMA/CD type collision detection and resolution
- Programmable packet-priority management with four levels (highest, high, standard and deferred)
- Packet queuing function
- Error detection (CRC 16)
- High-efficiency Forward Error Correction (FEC)
- Efficient nibble-oriented data encoding/decoding
- Full transaction-type management using unacknowledged and acknowledged messages
- General timer used for delay timing of retransmission, duplicate packet rejection
- Parallel and serial interface port (SPI compliant)
- Protocol neutrality, transports any high-level protocol packet (known or user-defined protocols) in a single network

Overview

The AC-PLM-1 ASIC is a single-chip digital modem implementing a half-duplex transmitter/receiver function to interface between a host and the power line. Using either a SPI or Parallel port, a host device is capable of sending and/or receiving information or commands to any other device connected to the power line. The modem includes a complete set of high-level functions, enabling designers to easily implement high-performance power line communication networks. The host can be any microcontroller with an SPI port or any computer with a parallel port.

◎ Communication media

The AC-PLM-1 offers the possibility to transport any communication data over AC power line, DC line or twisted pair i.e. dedicated lines. This offers the possibility to link multiple existing networks.

◎ Flexibility

The use of the AC-PLM-1 provides a lot of flexibility to your system. Based on the clock frequency, the baud rate and the carrier frequency, a number of parameters will be calculated using our tool. Those calculated parameters are used to configure the AC-PLM-1. After each soft or hard reset, the AC-PLM-1 expects to receive that string of parameters via its communication port. The CFGD pin indicates that the configuration string has been received with no error.

◎ Host

Being SPI compliant, the communication port of the AC-PLM-1 can be linked to any micro-controller the application requires. The same communication port allows any PC to receive any command from the AC-PLM-1.

The following table shows the functionality of the Communication port pins based on the status of the PORTYPE pin:

PIN	PORTYPE	
	Serial (0)	Parallel (1)
PORT0	PDAV	DIO0/PDAV
PORT1	LBUSY	DIO1/LBUSY
PORT2	PBUSY	DIO2/PBUSY
PORT3	SDI	DIO3
PORT4	SDO	DIO4
PORT5	PCKPOL	RW
PORT6	PCK	STR
PORT7	Chip Select	Chip Select

NOTE: The data from the transceiver is nibble-oriented. A complete byte will be received every two transmissions. An interrupt is generated when a nibble has been received by the AC-PLM-1.

◎ External Components

Few components are necessary to complete the functionality of the device. An external clock is required. It can come from an oscillator or if a microcontroller is used, its clock circuitry can be used to clock the transceiver.

Since the transceiver is using low-harmonic narrowband modulation, a ceramic filter is necessary to remove the out-of-band frequencies. Ariane Controls can provide you this component based on the central frequency chosen by your design team.

◎ Applications

The Ariane Controls PLM-1 chip is a type B technology used in cost - sensitive, medium baud rate applications.
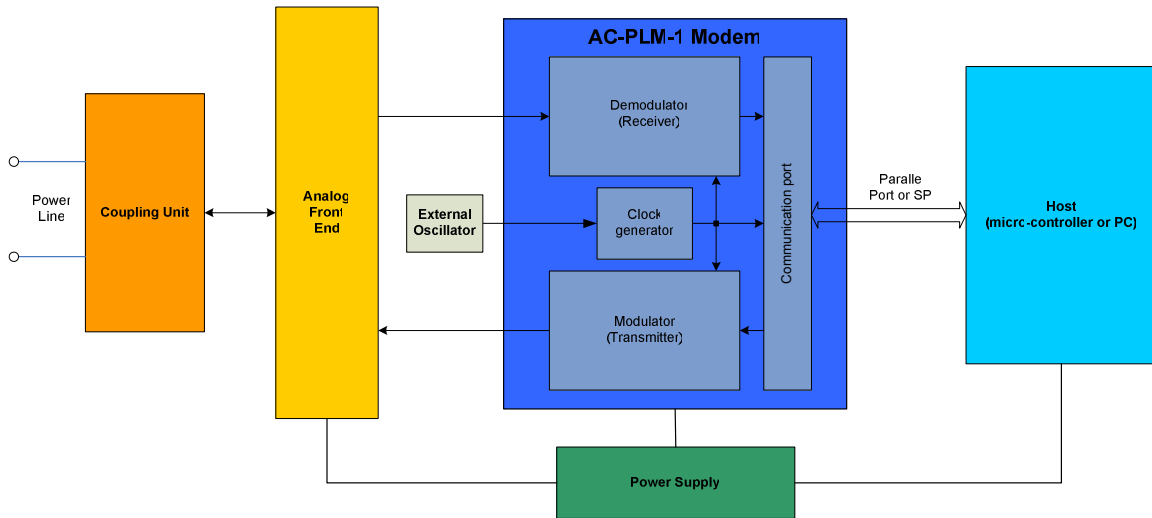
Utilities:
- Automatic Meter Reading (AMR)
- Remote Display
- Load Shedding
- Remote Diagnostic
- Street Light Monitoring

Building Automation:
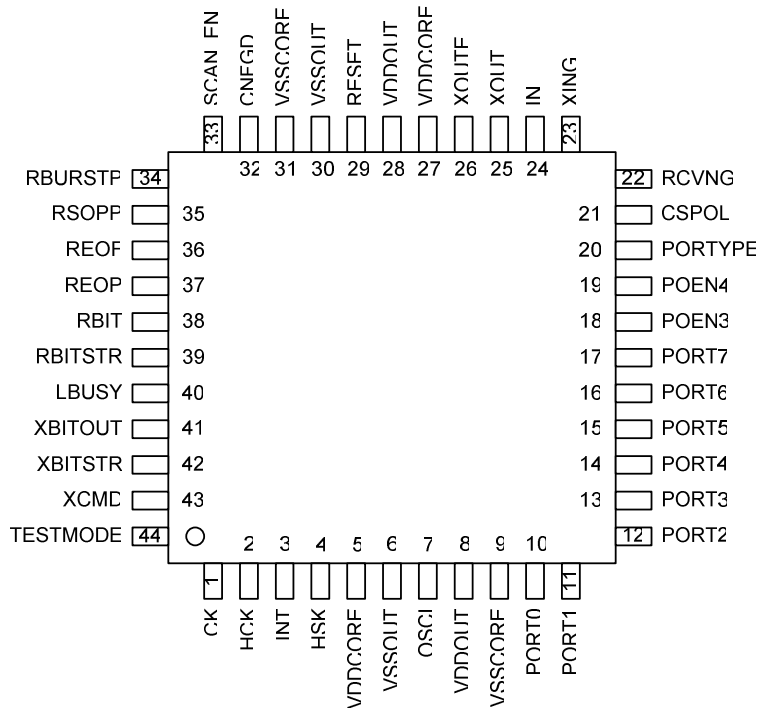- Light Switches
- Wall Outlets
- Thermostats/HVAC
- Clocks
- Sensors
- Alarm/Security
- People Care
- Access Controls

⌂ Transceiver Block Diagram

The external circuit diagrams can be provided upon request.

⌂ AC-PLM-1 Modem Pinout Diagram

⌂ AC-PLM-1 Modem Pin Descriptions

Pin Name	Type	Pin No.	Drive (mA)	Functions
CK	Output	1	1	Frequency carrier = OSCI/XDVI.
HCK	Output	2	1	OSCI clock output.
INT[2]	Output	3	2	Interrupt.
HSK[2]	Tri-state	4	2	Handshake signal.
VDDCORE	VCC	5,27	-	3.3V input.
VSSOUT	GND	6,30	-	Ground signal.
OSCI	Input	7	-	Input clock signal.
VDDOUT	VCC	8,28	-	3.3V input.
VSSCORE	GND	9,31	-	Ground signal.
PORT0[1,2]	Inout	10	2	Data IO 0 / Data available on the communication port.
PORT1[1,2]	Inout	11	2	Data IO 1 / Line busy indication.
PORT2[1,2]	Inout	12	2	Data IO 2 / Communication port busy indication.
PORT3[1,2]	Inout	13	2	Data IO 3 / Serial data in (SDI).
PORT4[1,2]	Inout	14	2	Data IO 4 / Serial data out (SDO).
PORT5[1,2]	Input	15	-	Clock polarity in serial mode / read-write enable in parallel mode. Read = 1'b1.
PORT6[1,2]	Input	16	-	Strobe or clock signal.
PORT7[1,2]	Input	17	-	Chip Select.
POEN3[2]	Output	18	2	Port output enable for PORT3. Output when POEN3 = 1.
POEN4[2]	Output	19	2	Port output enable for PORT0, 1, 2 and 4. Output when POEN4 = 1.
PORTYPE[1,2]	Input	20	-	Communication port type. 1 = Parallel, 0 = serial.
CSPOL[1,2]	Input	21	-	Chip Select polarity. 1 = CS active high.
RCVNG	Output	22	8	Receiving a valid packet. Can drive a LED. Active low.
XING	Output	23	8	Transmitting a valid packet. Can drive a LED. Active low.
IN[2]	Input	24	-	Receiver input.
XOUT[2]	Output	25	1	Transmitter output. Need to be filtered to eliminate second frequency generated by the chip.
XOUTE[2]	Output	26	1	Amplifier enable signal.
RESET	Output	29	-	Hardware reset. Active low. Internal pull-up.
CNFGD	Output	32	-	Configuration status. Active high. Can drive a LED.
SCAN_EN[3]	Input	33	-	Use to internal test. Internal pull-down. Must be tied to GND.
RBURSTP	Output	34	1	DEBUG pin. Receiver burst pulse. No connect.
RSOPP	Output	35	1	DEBUG pin. Receiver side. Start of packet pulse. No connect.
REOF	Output	36	1	DEBUG pin. Receiver side. End of field. No connect.
REOP	Output	37	1	DEBUG pin. Receiver side. End of packet. No connect.
RBIT	Output	38	1	DEBUG pin. Receiver side. A bit of a packet.
RBITSTR	Output	39	1	DEBUG pin. Receiver side. Strobe to validate a RBIT.
LBUSY	Output	40	1	DEBUG pin. Line busy indicator.
XBITOUT	Output	41	1	DEBUG pin. TX side. Output bit before modulation.
XBITSTR	Output	42	1	DEBUG pin. TX side. Output bit strobe.
XCMD	Output	43	1	DEBUG pin. TX side. Command indicator.
TESTMODE	Output	44	1	Use by BIST test. Internal pull-down. Must be tied to GND.

1. This pin has a permanent pull-up of 50Kohms.
2. This pin is 5V Tolerant.
3. This pin has a permanent pull-down.

◎ **SPI Timing Diagram**
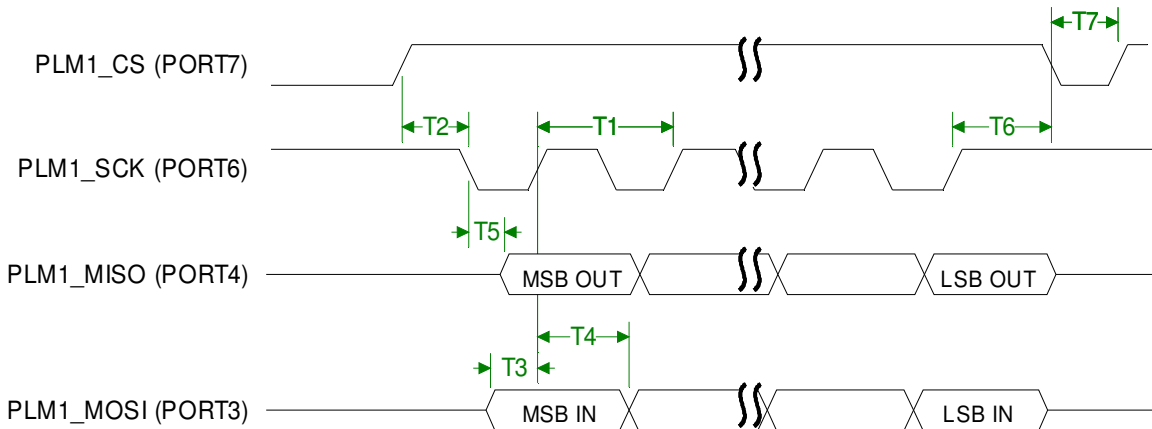
Num	Function	Min	Max	Unit
1	SCK period	4	32	t_{cyc}
2	Enable Time	4		t_{cyc}
3	Data Setup Time	30		ns
4	Data Hold Time	30		ns
5	Slave Access Time		2	t_{cyc}
6	Enable Log Time	2		t_{cyc}
7	Sequentiel Transfer Time	2		t_{cyc}

$t_{cyc} = 1/f_{OSCI}$

◎ **Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDCORE}	Supply Voltage	3.0	3.3	3.6	V
V_{DDOUT}	Supply Voltage	3.0	3.3	3.6	V
OSCI	Clock frequency	4.0	6.144	20	MHz
F_{IN}	Baud rate = bandwidth of the ceramic filter @ -6dB	0.100	2.544	30	kHz
$F_{carrier}$	Carrier frequency, i.e. central frequency of the ceramic filter	50	262	500	kHz
T_A	Ambient Temperature	-40	25	85	°C

◎ Electrical Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low-Level Voltage (3V TTL or 5V TTL Tolerant)	-	-	0.8	V
V_{IH}	Input Low-Level Voltage (3V TTL or 5V TTL Tolerant)	2.0	-	-	V
V_{OL}	Output Low-Level Voltage	-	-	0.4	V
V_{OH}	Output High-Level Voltage	2.4	-	-	V

◎ Absolute Maximum Ratings

Ambient operating temperature	-40 to 85°C
Storage Temperature	-55 to 125°C
Junction Temperature	88°C
Power dissipation	33 mW
The maximum DC current source by any VDD or VSS pin	±28 mA
Maximum Operating Frequency	20 MHz

◎ AC-PLM-1 Modem Pad Layout
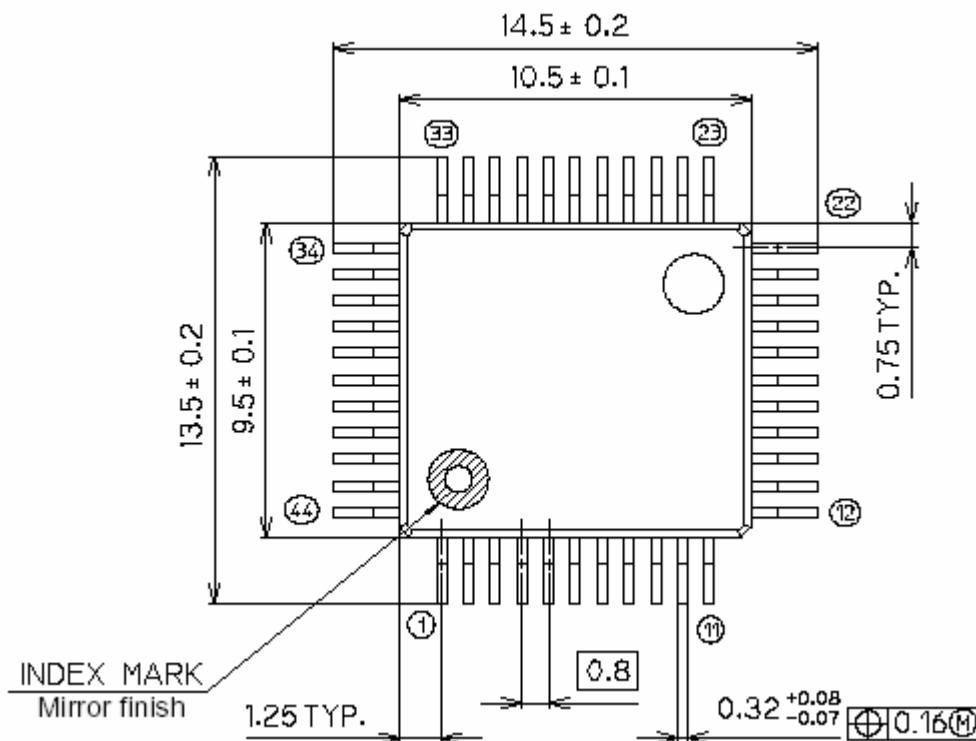
⬟ AC-PLM-1 Modem Package Diagram (PQFP-44)
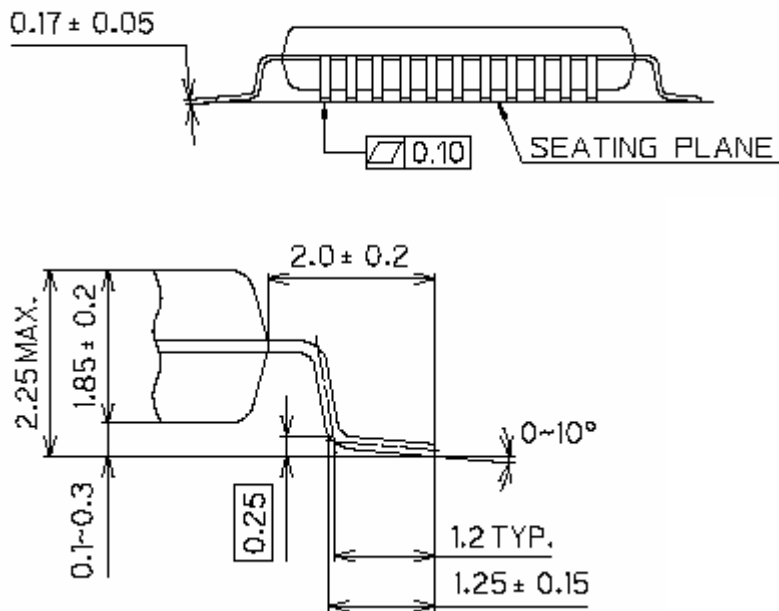
⬟ Ordering Information

Product number: AC-PLM-1
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⬟ References

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