MOTOROLA

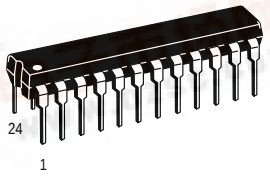
Octal Transceiver/Register With 3-State Outputs (Non-Inverting)

MC74AC652
MC74ACT652

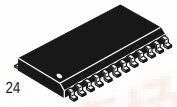
OCTAL TRANSCEIVER/ REGISTER WITH 3-STATE OUTPUTS (NON-INVERTING)

The MC74AC/ACT652 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in Figures 1 to 4.

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual-in-Line Package
- Outputs Source/Sink 24 mA
- ′ACT652 Has TTL Compatible Inputs



N SUFFIX
CASE 724-03
PLASTIC PACKAGE



DW SUFFIX
CASE 751E-04
SOIC PACKAGE

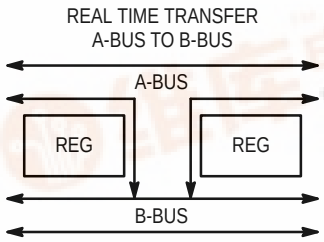


Figure 1

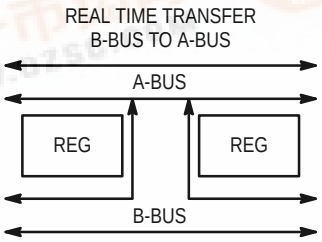


Figure 2

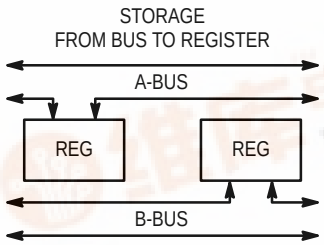


Figure 3

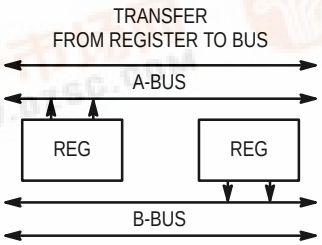


Figure 4

PIN NAMES

$A_0 – A_7$	Data Register A Inputs Data Register A Outputs
$B_0 – B_7$	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, $\overline{SBA}$	Transmit/Receive Inputs
GAB, GBA	Output Enable Inputs

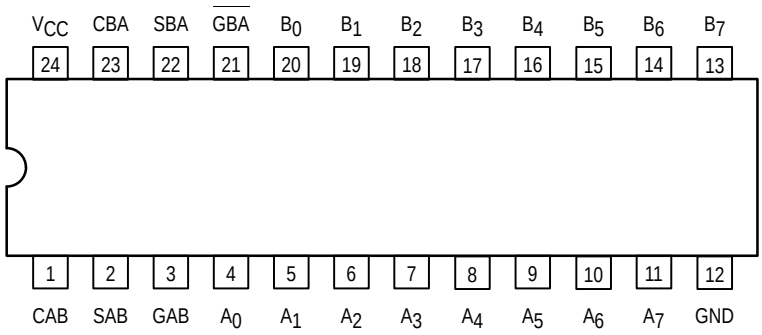
MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

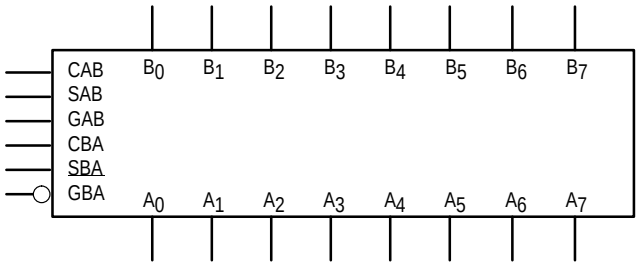
* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC652 MC74ACT652

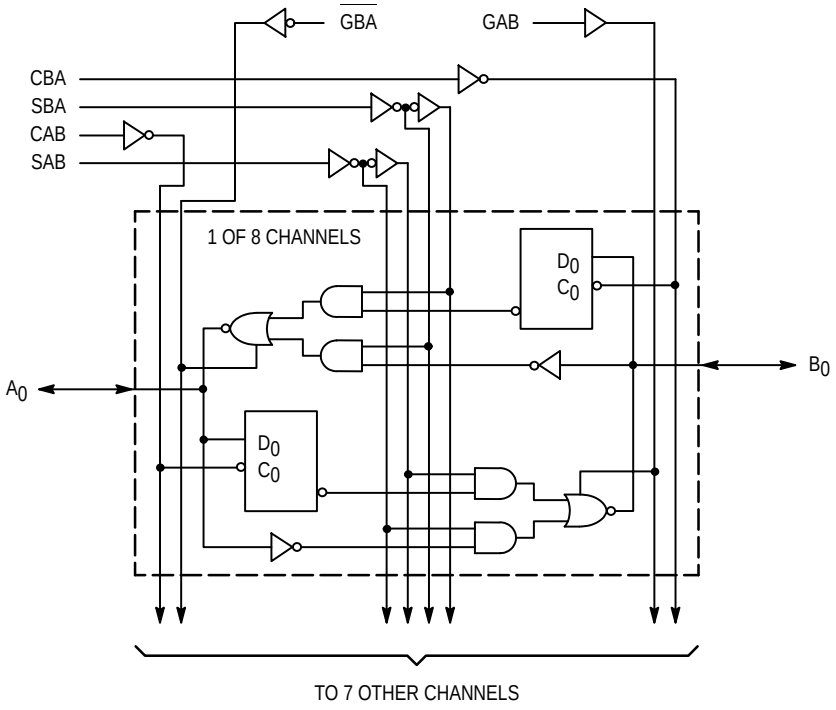
Pinout: 24-Lead Plastic Package (Top View)



LOGIC SYMBOL



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	$A_0 - A_7$	$B_0 - B_7$	
L L	H H	H or L ⇑	H or L ⇑	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	⇑ ⇑	H or L ⇑	X X**	X X	Input Input	Unspecified* Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ⇑	⇑ ⇑	X X	X X**	Unspecified* Output	Input Input	Hold A, Store B Store B in Both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GBA and GAB inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

** Select control = L: clocks can occur simultaneously.

H = HIGH Voltage Level; L = LOW Voltage Level; X = Immaterial; ⇑ = LOW-to-HIGH Transition

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Min	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current — HIGH				–24	mA
I_{OL}	Output Current — LOW				24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = – 50 μA
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} – 12 mA I_{OH} – 24 mA – 24 mA
V_{OL}	Minimum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O= V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one input loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = –40°C to +85°C C_L = 50 pF		Unit
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay CPBA or CPAB to A_n or B_n	3.0 5.0	4.0 2.5	17.0 12.0	3.0 2.0	19.0 14.0	ns
t_{PHL}	Propagation Delay CPBA or CPAB to A_n or B_n	3.0 5.0	3.0 2.0	14.5 10.5	2.5 1.5	16.5 12.0	ns
t_{PLH}	Propagation Delay A or B to B_n or A_n	3.0 5.0	3.0 2.0	14.0 9.5	2.5 1.5	16.0 11.0	ns
t_{PHL}	Propagation Delay A or B to B_n or A_n	3.0 5.0	2.5 1.5	13.0 9.0	2.0 1.0	15.0 10.5	ns
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n	3.0 5.0	3.0 2.5	14.0 10.0	2.5 2.0	16.0 11.5	ns
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n	3.0 5.0	2.5 2.0	13.5 10.0	2.0 1.5	15.5 11.5	ns
t_{PZH}	Output Enable Time OEBA to A_n	3.0 5.0	2.5 1.5	12.0 9.0	2.0 1.0	13.5 10.0	ns
t_{PZL}	Output Enable Time OEBA to A_n	3.0 5.0	2.5 1.5	12.0 9.0	2.0 1.0	14.0 10.5	ns
t_{PHZ}	Output Disable Time OEBA to A_n	3.0 5.0	3.0 2.0	13.0 11.0	2.5 1.5	14.0 12.0	ns
t_{PLZ}	Output Disable Time OEBA to A_n	3.0 5.0	2.5 2.0	12.5 10.5	2.0 1.5	14.0 12.0	ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	74ACT T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = – 50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} – 24 mA I_{OH} – 24 mA
V_{OL}	Minimum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = – 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} – 24 mA I_{OH} – 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1 V
I_{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one input loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = –40°C to +85°C C_L = 50 pF		Unit
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay CPBA or CPAB to A_n or B_n	5.0	4.0	14.5	3.5	16.5	ns
t_{PHL}	Propagation Delay CPBA or CPAB to A_n or B_n	5.0	3.5	14.5	3.0	16.5	ns
t_{PLH}	Propagation Delay A or B to B_n or A_n	5.0	2.5	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay A or B to B_n or A_n	5.0	2.5	11.5	2.0	13.0	ns
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n	5.0	2.5	12.0	2.0	13.5	ns
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n	5.0	3.0	12.0	2.5	13.5	ns
t_{PZH}	Output Enable Time OEBA to A_n	5.0	2.0	11.5	1.5	13.0	ns
t_{PZL}	Output Enable Time OEBA to A_n	5.0	2.5	11.5	2.0	13.0	ns
t_{PHZ}	Output Disable Time OEBA to A_n	5.0	3.0	13.0	2.5	14.0	ns
t_{PLZ}	Output Disable Time OEBA to A_n	5.0	2.5	12.5	2.0	14.0	ns
t_{PZH}	Output Enable time OEAB to B_n	5.0	2.5	12.0	2.0	13.5	ns
t_{PZL}	Output Enable Time OEAB to B_n	5.0	2.5	12.0	2.0	13.5	ns
t_{PHZ}	Output Enable Time OEAB to B_n	5.0	3.5	13.5	3.0	14.5	ns
t_{PLZ}	Output Enable Time OEAB to B_n	5.0	3.0	13.5	2.5	15.0	ns
t_s	Setup Time, HIGH or LOW A_n or B_n to CPBA or CPAB	5.0	7.0		8.0		ns
t_h	Hold Time, HIGH or LOW A_n or B_n to CPBA or CPAB	5.0	2.5		2.5		ns
t_w	CPAB, CPBA Pulse Width HIGH or LOW	5.0	6.0		7.0		ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

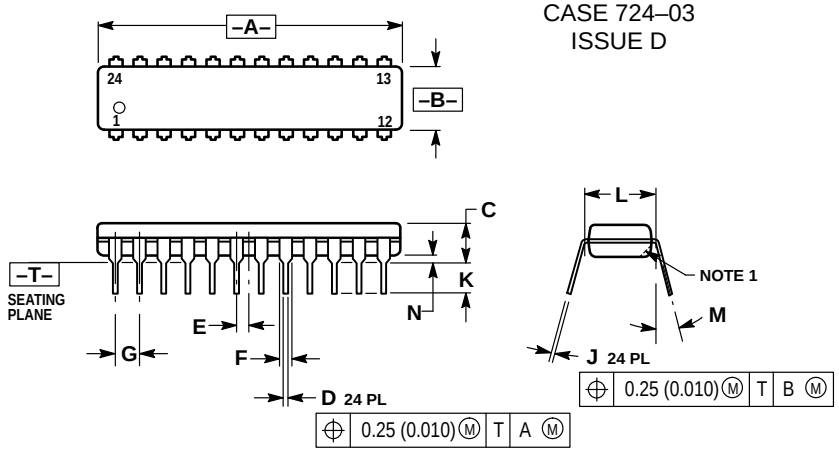
CAPACITANCE

Symbol	Parameter	74ACT Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0 V

MC74AC652 MC74ACT652

OUTLINE DIMENSIONS

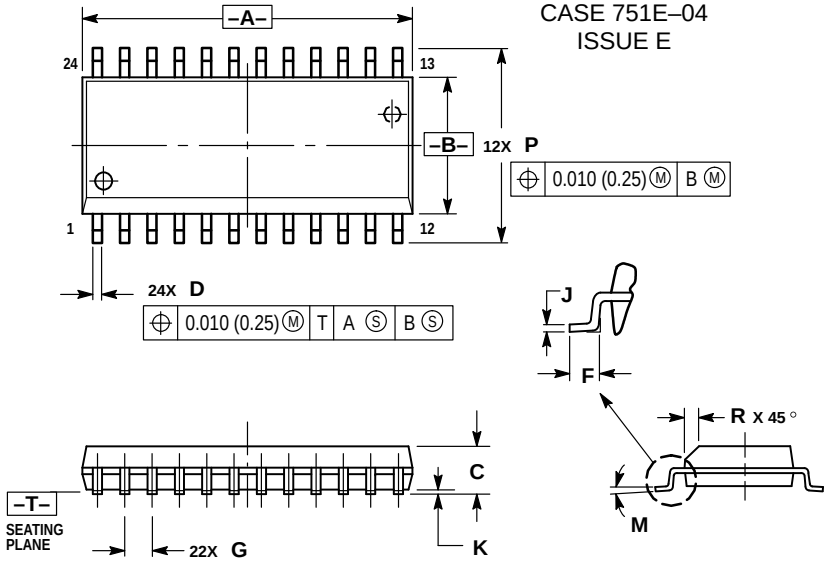
N SUFFIX
PLASTIC DIP PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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