

TOSHIBA**TC74HC697AP/AF**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC697AP, TC74HC697AF**SYNCHRONOUS PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH OUTPUT REGISTER
(MULTIPLEXED 3-STATE OUTPUTS)**

The TC74HC697A is high speed CMOS UP / DOWN COUNTERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It counts on the rising edge of the Counter Clock (CCK) input when "counter mode" is selected. If the up / down ($U/\overline{D}$) input is held high, the internal counter counts up. Conversely, if $U/\overline{D}$ is held low, it counts down.

The internal counters outputs are latched into the output registers on the rising edge of the Register Clock (RCK) input.

The outputs (QA ~ QD) are selected as either internal counter or registered outputs by the output select ($R/\overline{C}$) input. When high, the outputs are counter outputs and when low, they are registered outputs.

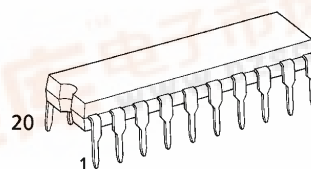
Two enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a carry ($\overline{RCO}$) output are provided to enable cascading of the counters.

This facilitates easy implementation of n-bit counters without using external gates.

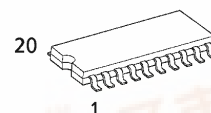
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

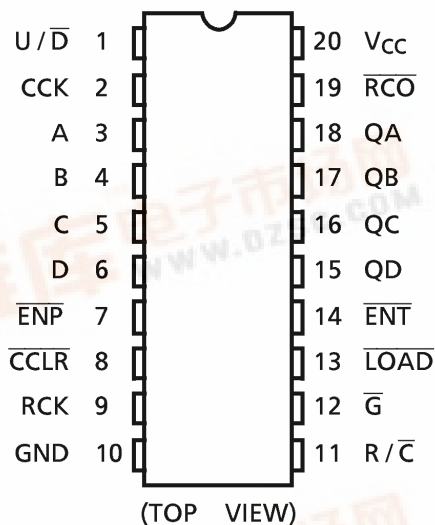
- High Speed..... $f_{MAX} = 38\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability.....15 LSTTL Loads
For QA ~ QD
10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance..... $|I_{OH}| = |I_{OL}| = 6\text{mA}$ (Min.)
For QA ~ QD
 $|I_{OH}| = |I_{OL}| = 4\text{mA}$ (Min.)
For $\overline{RCO}$
- Balanced Propagation Delays... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range... V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS697



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)



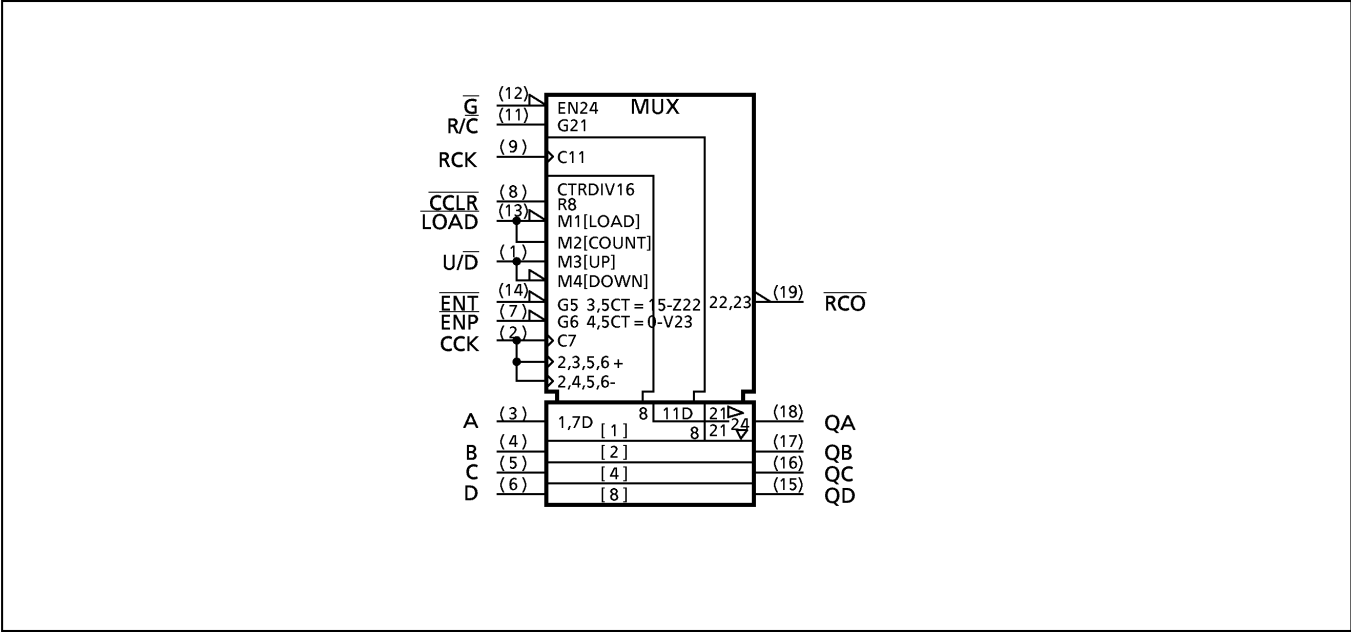
F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)

PIN ASSIGNMENT

980508EBA2

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IEC LOGIC SYMBOL



980508EBA2'

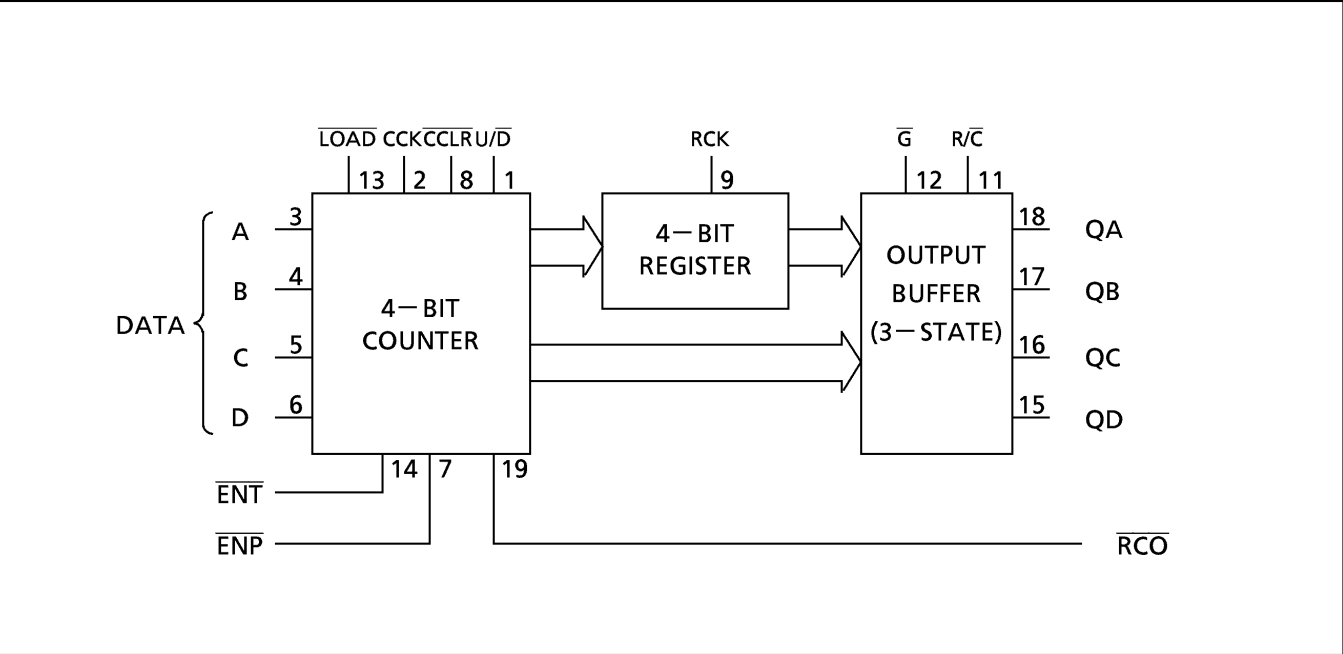
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TRUTH TABLE

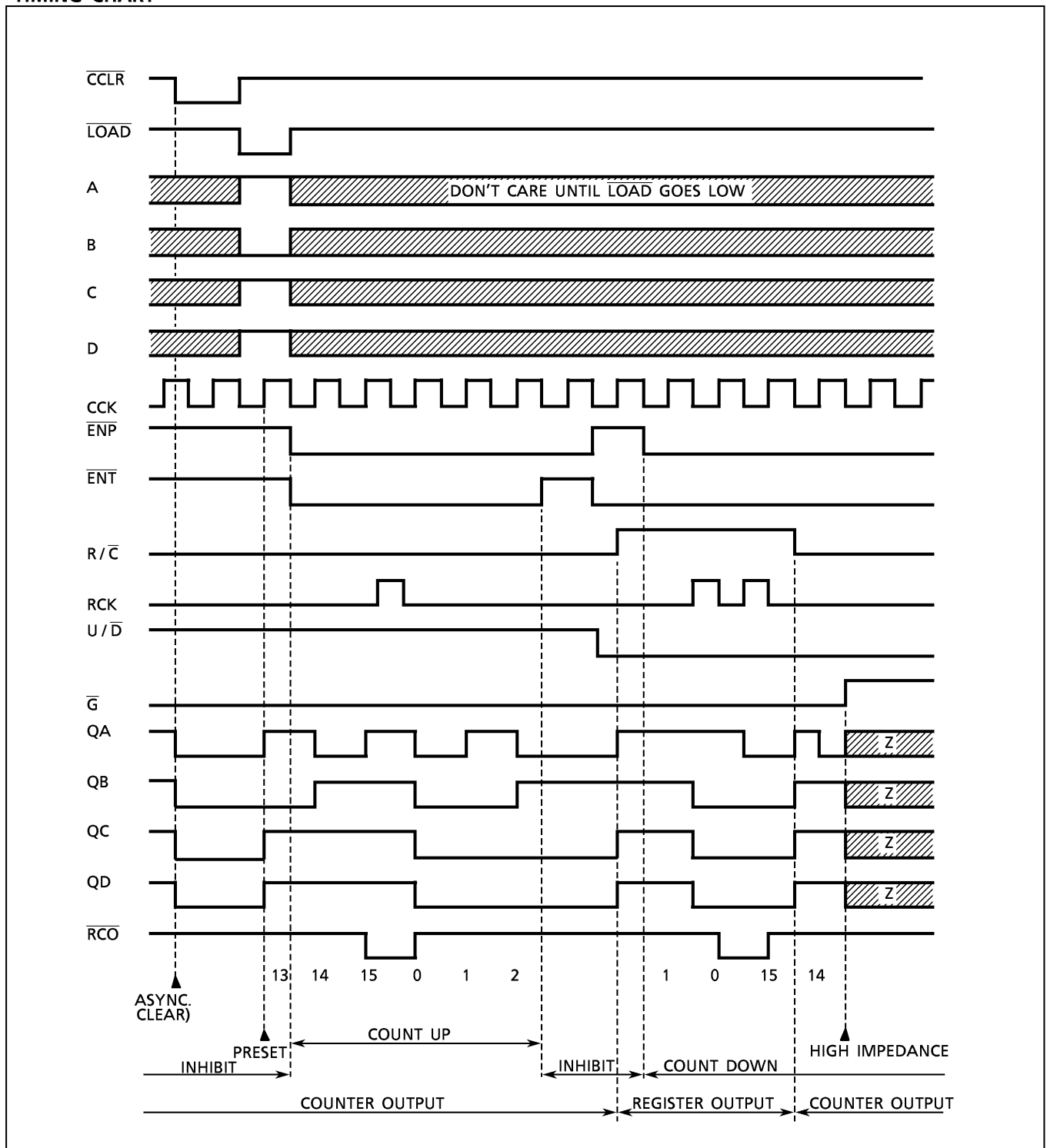
INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	U/D	RCK	R/C	G	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH INPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X		X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X		X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H		X	X	L	L					
H	H	L	L		H	X	L	L	COUNT UP				COUNT
H	H	L	L		L	X	L	L	COUNT DOWN				COUNT
H	X	X	X		X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X		H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X		H	L	NO CHANGE				NO COUNT

X : Don't Care
Z : High Impedance
a~d : The level of steady state inputs at inputs A through D respectively.
a'~d' : The level of steady atate outputs at internal counter outputs QA' through QD' respectively.
 $RCO = (UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT)$

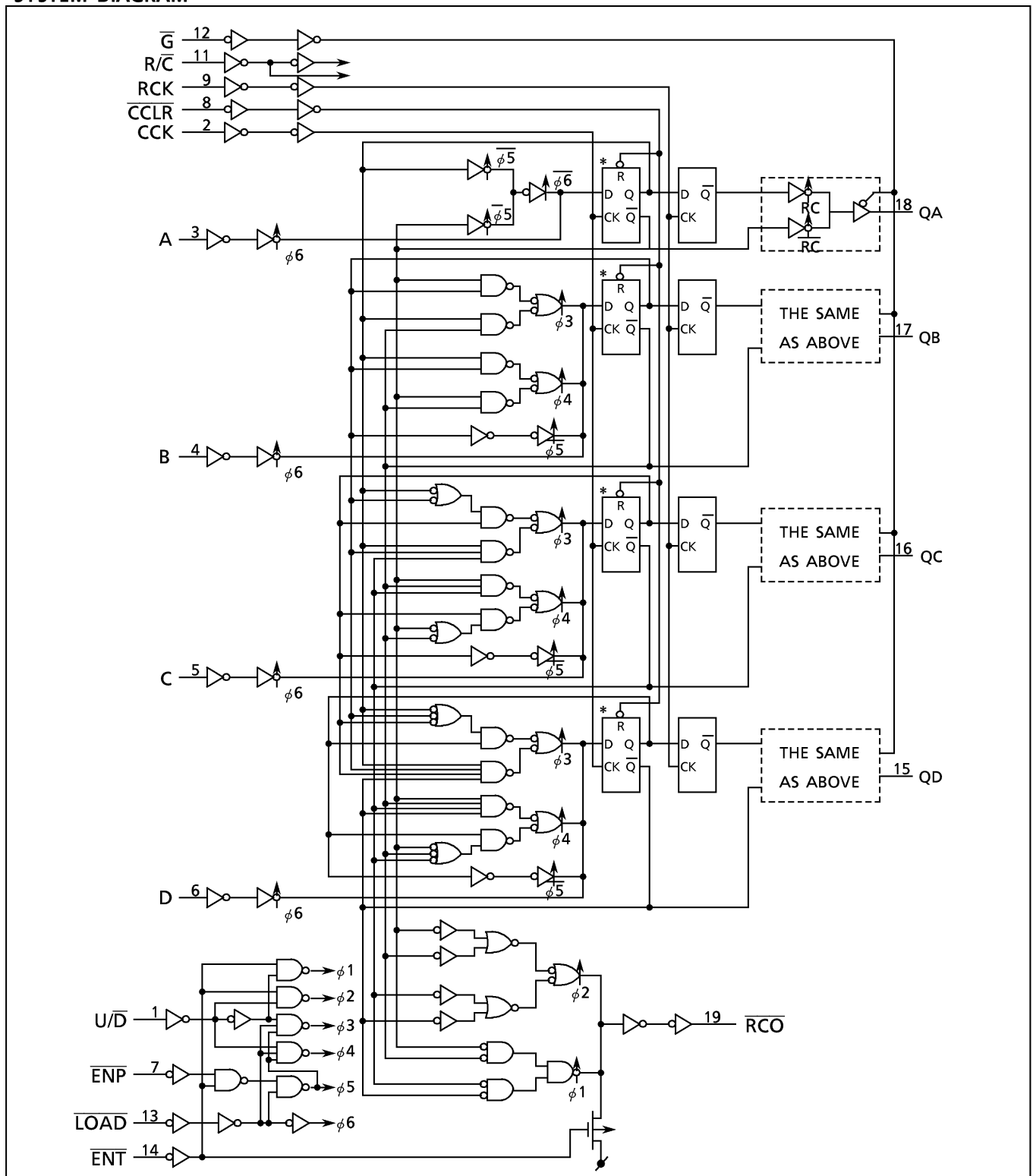
BLOCK DIAGRAM



TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current ^($\overline{RCO}$) ($Q_A \sim Q_D$)	I_{OUT}	± 25 ± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~ 500 ($V_{CC} = 4.5\text{V}$) 0~ 400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V _{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			$\overline{\text{RCO}}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		Q _A ~ Q _H	I _{OH} = -6 mA I _{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$\overline{\text{RCO}}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		Q _A ~ Q _H	I _{OL} = 4 mA I _{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		4.5 6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$		$T_a = -40\sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{\text{CCLR}}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time ($\overline{\text{LOAD}}$, $\overline{\text{ENT}}$, $\overline{\text{ENP}}$)	t_s		2.0	—	150	190	
			4.5	—	30	38	
			6.0	—	13	32	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Set-up Time ($\text{U}/\overline{\text{D}}$)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (CCK—RCK)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Hold Time (A, B, C, D)	t_h		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	
Minimum Hold Time	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time	t_{rem}		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	
Clock Frequency	f		2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{\text{RCO}}$)	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CCK— $\overline{\text{RCO}}$)	t_{pLH} t_{pHL}		—	24	41	
Propagation Delay Time ($\overline{\text{ENT}}$ — $\overline{\text{RCO}}$)	t_{pLH} t_{pHL}		—	13	23	
Propagation Delay Time ($\overline{\text{CCLR}}$ — $\overline{\text{RCO}}$)	t_{pLH}		—	23	38	
Maximum Clock Frequency	f_{MAX}		25	38	—	MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Qn)	t_{TLH} t_{THL}		50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output Transition Time (RCO)	t_{PLH} t_{PHL}		50	2.0	—	30	75	—	95	
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation Delay Time (CCK—Q)	t_{PLH} t_{PHL}		50	2.0	—	90	195	—	245	
				4.5	—	26	39	—	49	
				6.0	—	19	33	—	42	
			150	2.0	—	103	235	—	295	
				4.5	—	31	47	—	59	
				6.0	—	23	40	—	50	
Propagation Delay Time (RCK—Q)	t_{PLH} t_{PHL}		50	2.0	—	82	180	—	225	
				4.5	—	24	36	—	45	
				6.0	—	18	31	—	38	
			150	2.0	—	95	220	—	275	
				4.5	—	29	44	—	55	
				6.0	—	22	37	—	47	
Propagation Delay Time (R/C—Q)	t_{PLH} t_{PHL}		50	2.0	—	60	145	—	180	
				4.5	—	19	29	—	36	
				6.0	—	14	25	—	31	
			150	2.0	—	73	185	—	230	
				4.5	—	24	37	—	46	
				6.0	—	18	31	—	39	
Propagation Delay Time (CCLR—Q)	t_{PHL}		50	2.0	—	89	195	—	245	
				4.5	—	26	39	—	49	
				6.0	—	20	33	—	42	
			150	2.0	—	102	235	—	295	
				4.5	—	31	47	—	59	
				6.0	—	24	40	—	50	
Propagation Delay Time (CCK—RCO)	t_{PLH} t_{PHL}		50	2.0	—	108	235	—	295	
				4.5	—	31	47	—	59	
				6.0	—	23	40	—	50	
Propagation Delay Time (ENT—RCO)	t_{PLH} t_{PHL}		50	2.0	—	63	135	—	170	
				4.5	—	18	27	—	34	
				6.0	—	14	23	—	29	
Propagation Delay Time (CCLR—RCO)	t_{PLH}		50	2.0	—	98	220	—	275	
				4.5	—	29	44	—	55	
				6.0	—	23	37	—	47	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Enable Time ($\bar{G}-Q$)	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	50	2.0	—	45	115	—	145	ns
				4.5	—	15	23	—	29	
			150	6.0	—	12	20	—	25	
				2.0	—	58	155	—	195	
Output Disable Time ($\bar{G}-Q$)	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	50	4.5	—	20	31	—	39	ns
				6.0	—	16	26	—	33	
			150	2.0	—	32	115	—	145	
				4.5	—	17	23	—	29	
Maximum Clock Frequency	f_{MAX}		50	6.0	—	14	20	—	25	MHz
				2.0	5	11	—	4	—	
				4.5	25	38	—	20	—	
				6.0	29	52	—	24	—	
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Output Capacitance	C_{OUT}				—	13	—	—	—	
Power Dissipation Capacitance	$C_{\text{PD}} (1)$				—	72	—	—	—	

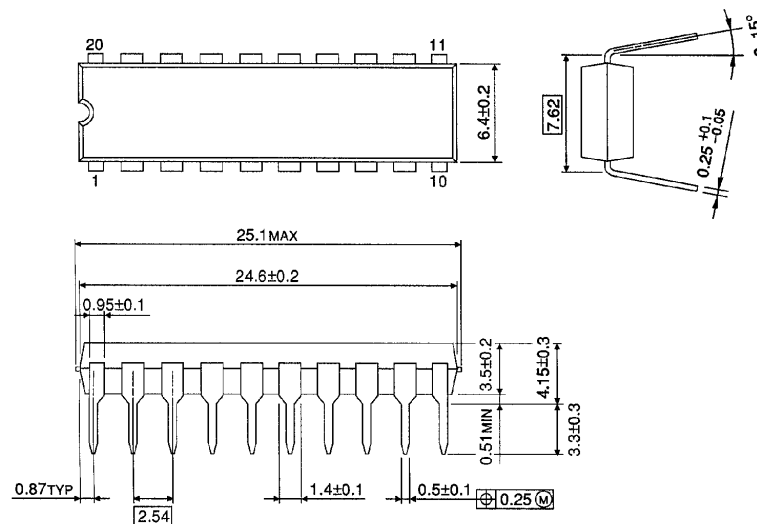
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

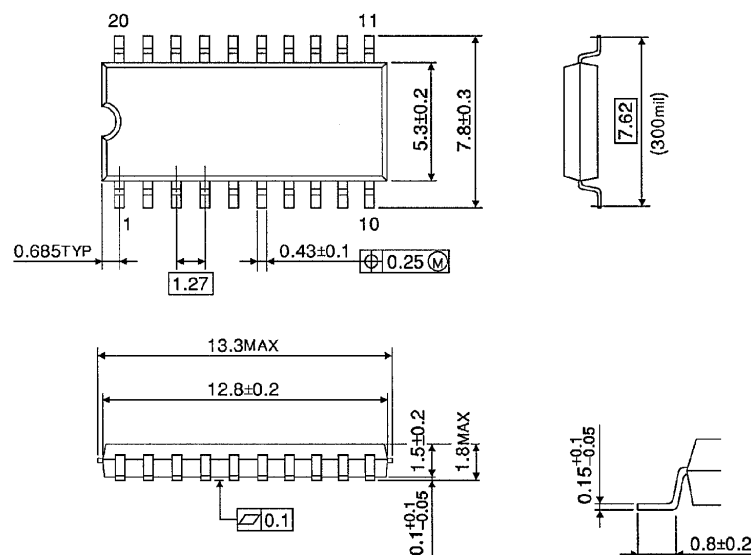
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm



Weight : 0.22g (Typ.)