FAIRCHILD SEMICONDUCTOR™

January 1990
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# 74ACQ646 • 74ACTQ646
# Quiet Series™ Octal Transceiver/Register with 3-STATE Outputs

## General Description

The ACQ/ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in Figure 1, Figure 2, Figure 3 and Figure 4.

The ACQ/ACTQ utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

## Features

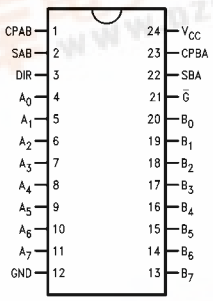
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC/ACT646

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ACQ646SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACQ464ASPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| 74ACTQ646SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACTQ464ASPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Connection Diagram




## Pin Descriptions

| Pin Names | Descriptions |
|---|---|
| $A_0$–$A_7$ | Data Register A Inputs |
| | Data Register A Outputs |
| $B_0$–$B_7$ | Data Register B Inputs |
| | Data Register B Outputs |
| CPAB, CPBA | Clock Pulse Inputs |
| SAB, SBA | Transmit/Receive Inputs |
| $\overline{G}$ | Output Enable Input |
| DIR | Direction Control Input |

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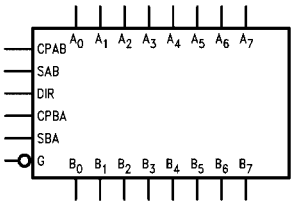
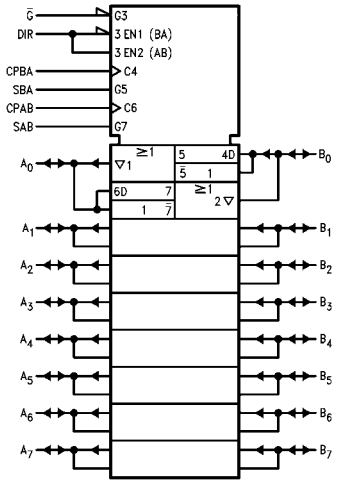
## Logic Symbols




IEEE/IEC




## Function Table

| Inputs | | | | | | Data I/O (Note 1) | | Function |
|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | DIR | CPAB | CPBA | SAB | SBA | $A_0$–$A_7$ | $B_0$–$B_7$ | |
| H | X | H or L | H or L | X | X | | | Isolation |
| H | X | ↓ | X | X | X | Input | Input | Clock $A_n$ Data into A Register |
| H | X | X | ↓ | X | X | | | Clock $B_n$ Data into B Register |
| L | H | X | X | L | X | | | $A_n$ to $B_n$—Real Time (Transparent Mode) |
| L | H | ↓ | X | L | X | Input | Output | Clock $A_n$ Data into A Register |
| L | H | H or L | X | H | X | | | A Register to $B_n$ (Stored Mode) |
| L | H | ↓ | X | H | X | | | Clock $A_n$ Data into A Register and Output to $B_n$ |
| L | L | X | X | X | L | | | $B_n$ to $A_n$—Real Time (Transparent Mode) |
| L | L | X | ↓ | X | L | Output | Input | Clock $B_n$ Data into B Register |
| L | L | X | H or L | X | H | | | B Register to $A_n$ (Stored Mode) |
| L | L | X | ↓ | X | H | | | Clock $B_n$ Data into B Register and Output to $A_n$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

**Real Time Transfer**
**A-Bus to B-Bus**

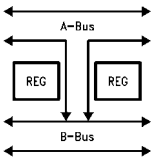



**FIGURE 1.**

**Real Time Transfer**
**B-Bus to A-Bus**

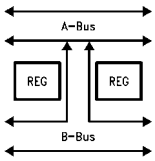



**FIGURE 2.**

**Storage from**
**Bus to Register**

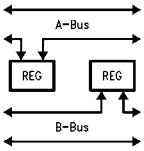



**FIGURE 3.**

**Transfer from**
**Register to Bus**

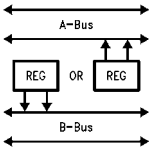
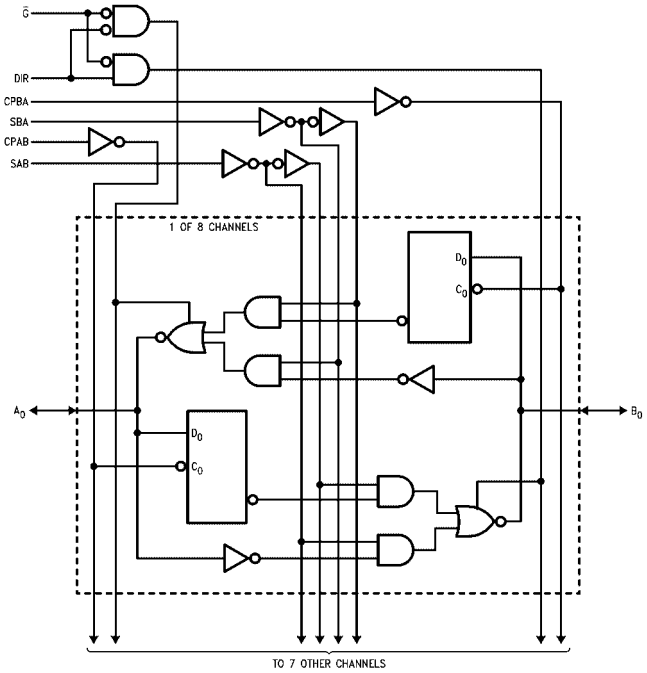



**FIGURE 4.**

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source | |
| or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source | |
| or Sink Current | ±300 mA |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| ACQ | 2.0V to 6.0V |
| ACTQ | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ΔV/Δt | |
| ACQ Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.0V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ΔV/Δt | |
| ACTQ Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for ACQ

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level | 3.0 | 1.5 | 2.1 | 2.1 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.9 | 0.9 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level | 3.0 | 2.99 | 2.9 | 2.9 | | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | | $I_{OH}$ = −12 mA |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.85 | 4.76 | | $I_{OH}$ = −24 mA (Note 3) |
| $V_{OL}$ | Maximum LOW Level | 3.0 | 0.002 | 0.1 | 0.1 | | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 3) |
| $I_{IN}$ (Note 5) | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 4) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 5) | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{OZT}$ | Maximum I/O Leakage Current ($A_n$, $B_n$ Inputs) | 5.5 | | ±0.6 | ±6.0 | μA | $V_I$(OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 1.1 | 1.5 | | V | Figures 5, 6 (Note 6)(Note 7) |

## DC Electrical Characteristics for ACQ (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | −0.6 | −1.2 | | V | Figures 5, 6 (Note 6)(Note 7) |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 3.1 | 3.5 | | V | (Note 6)(Note 8) |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.9 | 1.5 | | V | (Note 6)(Note 8) |

**Note 3:** Maximum of 8 outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

**Note 6:** Plastic DIP package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

**Note 8:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 5V (ACQ). Input-under-test switching 5V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$) f = 1 MHz.

## DC Electrical Characteristics for ACTQ

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V | $I_{OUT} = -50\ \mu A$ |
| | | 4.5<br>5.5 | | 3.86<br>4.86 | 3.76<br>4.76 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OH} = -24$ mA<br>$I_{OH} = -24$ mA (Note 9) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V | $I_{OUT} = 50\ \mu A$ |
| | | 4.5<br>5.5 | | 0.36<br>0.36 | 0.44<br>0.44 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OL} = 24$ mA<br>$I_{OL} = 24$ mA (Note 9) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | µA | $V_I = V_{CC}$, GND |
| $I_{OZT}$ | Maximum I/O Leakage Current ($A_n$, $B_n$ Inputs) | 5.5 | | ±0.6 | ±6.0 | µA | $V_I = V_{IL}$, $V_{IH}$<br>$V_O = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max |
| $I_{OHD}$ | Output Current (Note 10) | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | µA | $V_{IN} = V_{CC}$ or GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 1.1 | 1.5 | | V | Figures 5, 6 (Note 11)(Note 12) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | −0.6 | −1.2 | | V | Figures 5, 6 (Note 11)(Note 12) |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 1.7 | 2.0 | | V | (Note 11)(Note 13) |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 | | V | (Note 11)(Note 13) |

**Note 9:** All outputs loaded; thresholds on input associated with output under test.

**Note 10:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 11:** Plastic DIP Package.

**Note 12:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

**Note 13:** Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics for ACQ

| Symbol | Parameter | $V_{CC}$ (V) (Note 14) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 3.5 | 9.0 | 12.0 | 3.5 | 13.0 | ns |
| | Bus to Bus | 5.0 | 2.5 | 6.5 | 9.0 | 2.5 | 9.5 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 3.5 | 9.0 | 12.0 | 3.5 | 13.0 | ns |
| | Bus to Bus | 5.0 | 2.5 | 6.5 | 9.0 | 2.5 | 9.5 | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 3.5 | 10.0 | 13.0 | 3.5 | 14.0 | ns |
| | Clock to Bus | 5.0 | 2.5 | 7.0 | 9.5 | 2.5 | 10.5 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 3.5 | 10.0 | 13.0 | 3.5 | 14.0 | ns |
| | Clock to Bus | 5.0 | 2.5 | 7.0 | 9.5 | 2.5 | 10.5 | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 3.5 | 9.5 | 12.5 | 3.5 | 13.5 | ns |
| | SBA or SAB to $A_n$ or $B_n$ | 5.0 | 2.5 | 6.5 | 9.0 | 2.5 | 10.0 | |
| | (w/$A_n$ or $B_n$ HIGH or LOW) | | | | | | | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 3.5 | 9.5 | 12.5 | 3.5 | 13.5 | ns |
| | SBA or SAB to $A_n$ or $B_n$ | 5.0 | 2.5 | 6.5 | 9.0 | 2.5 | 10.0 | |
| | (w/$A_n$ or $B_n$ HIGH or LOW) | | | | | | | |
| $t_{PZH}$ | Enable Time | 3.3 | 3.5 | 10.5 | 14.5 | 3.5 | 15.5 | ns |
| | $\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 2.5 | 8.0 | 10.5 | 2.5 | 11.5 | |
| $t_{PZL}$ | Enable Time | 3.3 | 3.5 | 10.5 | 14.5 | 3.5 | 15.5 | ns |
| | $\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 2.5 | 8.0 | 10.5 | 2.5 | 11.5 | |
| $t_{PHZ}$ | Disable Time | 3.3 | 2.5 | 8.0 | 11.0 | 2.5 | 12.0 | ns |
| | $\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 1.5 | 5.0 | 7.5 | 1.5 | 8.0 | |
| $t_{PLZ}$ | Disable Time | 3.3 | 2.5 | 8.0 | 11.0 | 2.5 | 12.0 | ns |
| | $\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 1.5 | 5.0 | 7.5 | 1.5 | 8.0 | |
| $t_{PZH}$ | Enable Time | 3.3 | 4.5 | 11.0 | 15.5 | 4.5 | 17.0 | ns |
| | DIR to $A_n$ or $B_n$ | 5.0 | 3.0 | 8.5 | 11.0 | 3.0 | 11.5 | |
| $t_{PZL}$ | Enable Time | 3.3 | 4.5 | 11.0 | 15.5 | 4.5 | 17.0 | ns |
| | DIR to $A_n$ or $B_n$ | 5.0 | 3.0 | 8.5 | 11.0 | 3.0 | 11.5 | |
| $t_{PHZ}$ | Disable Time | 3.3 | 1.5 | 8.0 | 11.0 | 1.5 | 12.0 | ns |
| | DIR to $A_n$ or $B_n$ | 5.0 | 1.0 | 5.0 | 7.5 | 1.0 | 8.0 | |
| $t_{PLZ}$ | Disable Time | 3.3 | 1.5 | 8.0 | 11.0 | 1.5 | 12.0 | ns |
| | DIR to $A_n$ or $B_n$ | 5.0 | 1.0 | 5.0 | 7.5 | 1.0 | 8.0 | |
| $t_{OS}$ | Output to Output Skew (Note 15) | 3.3 | | 1.0 | 1.5 | | 1.5 | ns |
| | | 5.0 | | 0.5 | 1.0 | | 1.0 | |

**Note 14:** Voltage Range 3.3 is 3.3V ± 0.3V.
Voltage Range 5.0 is 5.0V ± 0.5V

**Note 15:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design. Not tested.

## AC Operating Requirements for ACQ

| Symbol | Parameter | $V_{CC}$ (Note 16) | $T_A = +25°C$ | $T_A = -40°C$ to $+85°C$ | Units |
|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | |
| $t_S$ | Setup Time, HIGH or LOW | 3.3 | | 3.0 | 3.0 | ns |
| | Bus to Clock | 5.0 | | 3.0 | 3.0 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | | 1.5 | 1.5 | ns |
| | Bus to Clock | 5.0 | | 1.5 | 1.5 | |
| $t_W$ | Clock Pulse Width | 3.3 | | 4.0 | 4.0 | ns |
| | HIGH or LOW | 5.0 | | 4.0 | 4.0 | |

**Note 16:** Voltage Range 5.0 is 5.0V ± 0.5V
Voltage Range 3.3 is 3.3V ± 0.3V

## AC Electrical Characteristics for ACTQ

| Symbol | Parameter | $V_{CC}$ (V) (Note 17) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Clock to Bus | 5.0 | 2.5 | 8.5 | 10.5 | 2.5 | 11.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Bus to Bus | 5.0 | 2.0 | 8.0 | 10.0 | 2.0 | 10.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>SBA or SAB to $A_n$ or $B_n$<br>(w/$A_n$ or $B_n$ HIGH or LOW) | 5.0 | 2.5 | 8.5 | 10.5 | 2.5 | 11.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Enable Time<br>$\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 2.5 | 10.0 | 12.0 | 2.5 | 12.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable Time<br>$\overline{G}$ to $A_n$ or $B_n$ | 5.0 | 1.0 | 7.0 | 8.5 | 1.0 | 9.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Enable Time<br>DIR to $A_n$ or $B_n$ | 5.0 | 2.5 | 10.0 | 12.0 | 2.5 | 12.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable Time<br>DIR to $A_n$ or $B_n$ | 5.0 | 1.0 | 7.0 | 8.5 | 1.0 | 9.0 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output to Output<br>Skew (Note 18) Select to Bus<br>or Clock to Bus | 5.0 | | 0.5 | 1.0 | | 1.0 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output to Output<br>Skew (Note 18)<br>Bus to Bus | 5.0 | | 1.0 | 1.5 | | 1.5 | ns |

**Note 17:** Voltage Range 5.0 is 5.0V ± 0.5V

**Note 18:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design. Not tested.

## AC Operating Requirements for ACTQ

| Symbol | Parameter | $V_{CC}$ (V) (Note 19) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW<br>Bus to Clock | 5.0 | | 3.0 | 3.0 | ns |
| $t_H$ | Hold Time, HIGH or LOW<br>Bus to Clock | 5.0 | | 1.5 | 1.5 | ns |
| $t_W$ | Clock Pulse Width<br>HIGH or LOW | 5.0 | | 4.0 | 4.0 | ns |

**Note 19:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{I/O}$ | Input/Output Capacitance | 15.0 | pF | $V_{CC}$ = 5.0V |
| $C_{PD}$ | Power Dissipation Capacitance | 90.0 | pF | $V_{CC}$ = 5.0V |

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

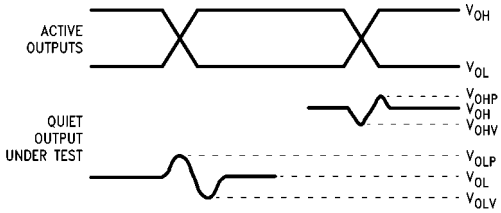



**FIGURE 5. Quiet Output Noise Voltage Waveforms**

**Note 20:** $V_{OHV}$ and $V_{OLP}$ are measured with respect to ground reference.

**Note 21:** Input pulses have the following characteristics: f = 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, skew < 150 ps.

$V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure $V_{OLP}$ and $V_{OLV}$ on the quiet output during the worst case transition for active and enable. Measure $V_{OHP}$ and $V_{OHV}$ on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$ and $V_{IHD}$:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, $V_{IL}$,until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input LOW voltage level at which oscillation occurs is defined as $V_{ILD}$.
- Next decrease the input HIGH voltage level, $V_{IH}$, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input HIGH voltage level at which oscillation occurs is defined as $V_{IHD}$.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

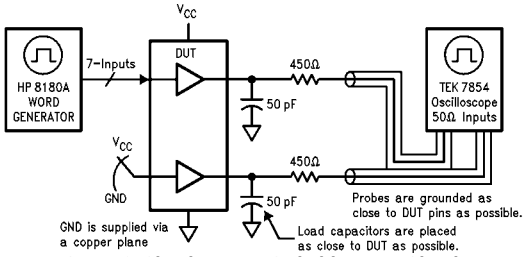
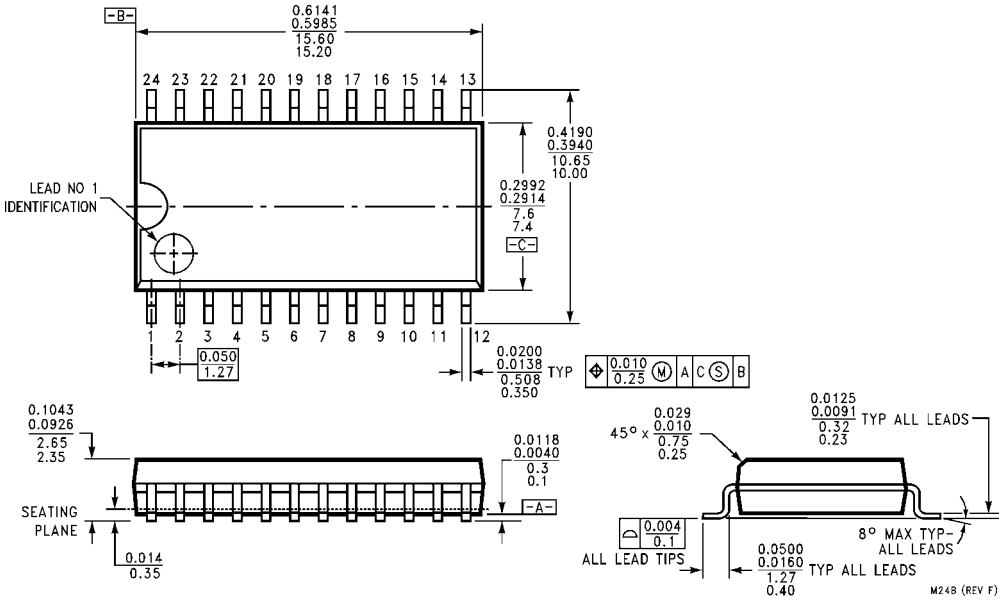


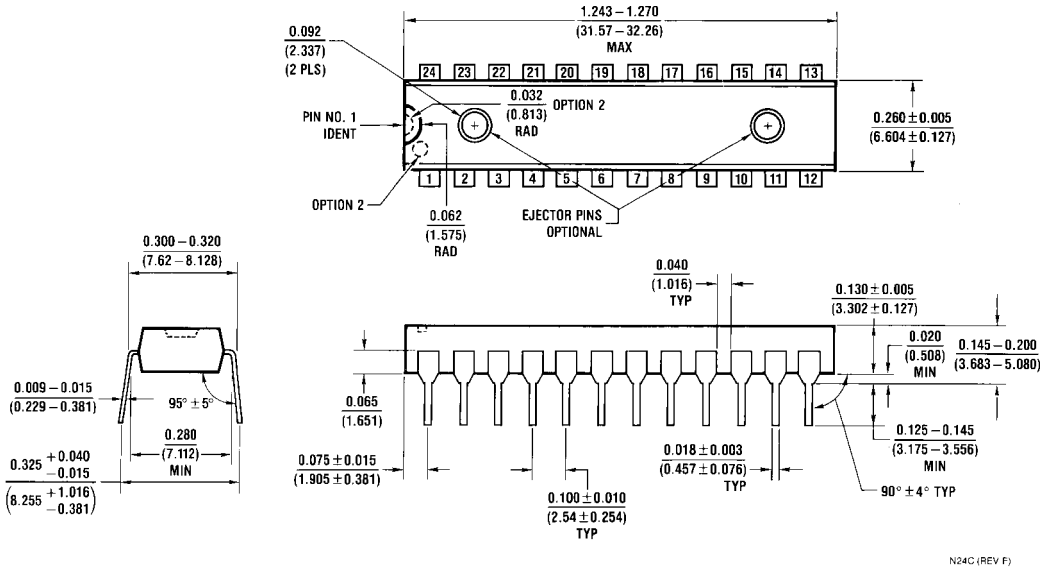

**FIGURE 6. Simultaneous Switching Test Circuit**

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M24B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N24C**



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