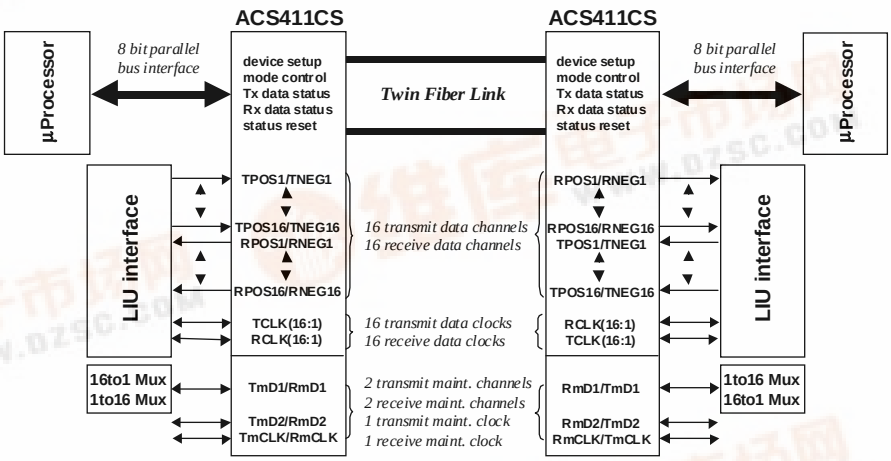
Acapella Optical Modem IC

ACS9000 SERIES

ACS411CS Main Features

* Three chip set supporting full duplex serial transmission over twin optical fiber, one fiber with WDM.
* Configurable parallel microprocessor bus interface.
* Up to 16 independent synchronous data channels.
  1 x OC1 (STS1) @ 51.840Mbps
  1 x E3/T3
  4 x E2, 7 x T2
  16 x E1/T1
* Select between NRZ and pseudo-bipolar HDB3/AMI/B3ZS/ B6ZS/B8ZS input data coding types.
* Incorporates 2 x 256kbps maintenance channels with option of multi channel operation with a framing signal.
* Link budgets of 27dB with Laser + PIN on single mode fiber.
* Conforms to all jitter attenuation, jitter transfer and input jitter tolerance specification defined by AT&T, ITU-T and Bellcore recommendations.
* Bit Error Rate (BER) of < 10^{-10}
* ACS9020 available in 64 pin TQFP and ACS4110 available in 176 pin TQFP package.



Twin fiber full duplex system using ACS411CS chip set with external T1/E1 Framer ICs and microprocessor.

General Description

The ACS411CS is a complete controller, driver and receiver chipset supporting full-duplex synchronous transmission up to 51.840Mbps over single/twin optical fiber. The designer can share the available bandwidth over 1 to 16 main channels.

In addition to the main channels, the ACS411CS provides two independent maintenance channels with a data rate selectable up to 256kbps. On the electrical side the ACS411CS has a selectable interface for either NRZ or the pseudo bipolar data coding types HDB3/AMI/B3ZS/B6ZS/B8ZS.

The ACS411CS has a parallel microprocessor bus interface. This can be used for device set-up, diagnostics, control and status analysis. Additional flags for Tx data status, Rx data status and alarm indication for both near

Acapella Optical Modem IC ACS411CS

The ACS411CS comprises a chip set of two/three (link budget dependent) highly integrated devices, the ACS9020 and ACS4110. The ACS9020 is an analogue device and the ACS4110 is predominately a digital device.

The ACS9020 contains the Laser/LED driver as well as the PIN receiver circuitry. Since the devices are transmitting and receiving continuously, for long haul applications two ACS9020 devices are required, one configured as the transmitter and the other configured as the receiver.

The ACS4110 comprises the logic necessary to time compress and decompress the data, plus clock recovery and all the logic associated with valid data transmission and reception and locking status. The ACS4110 also has a configurable parallel microprocessor bus interface for device configuration (control) and status analysis. The device setup is also possible via the far end (remote control) or directly via pins for the basic device setup.

For the purpose of this specification the chip-set will be referred to as the ACS411CS and the individual devices as the ACS9020 or ACS4110.

For low link budget applications (up to 10dB) two chips, the ACS9020 analogue IC (including laser driver and PIN receiver circuitry) and the ACS4110 are sufficient.

For applications requiring a higher link budget (up to 30dB) a three chip solution has to be used, where the laser driver and PIN receiver circuitry are separated.

Inter-Modem Coding

The inter-IC coding between communication modems is 8B10B. Whilst transparent to the user, 8B10B encoding ensures that there is no DC component in the signal, and provides frequent data transitions, factors which ease the task of data recovery and clock extraction.

The coding rules are continuously checked to ensure the integrity of the link, and errors are indicated on the ERRL and ERRC pins *(see section headed ERRC and ERRL - Error Detection).*

Transmit and Receive functions

Data presented at the near-end TPOS/TNEG is time-compressed, encoded in the 8B10B format and transmitted over the fiber link to the far end receiver. Similarly, data presented at the far-end TPOS/TNEG is time-compressed, encoded in the 8B10B format and transmitted over the other fiber link to the near end.

PORB

The Power On Reset (PORB) pin resets the device if forced low for 2ms or more. In normal operation PORB should be held High. It is recommended that PORB is connected to VD+ via a 100KΩ resistor and to GND via a 100nF capacitor.

System Clock

The system clock on the ACS411CS is derived locally using the on-chip crystal oscillator and multiplying PLL.

The oscillator (XTO/I) requires the use of a fundamental parallel resonance crystal with appropriate padding capacitors. The crystal specification should be:

Calibration tolerance: +/- 20ppm @ 25°C

Temp. tolerance: +/-20ppm @ -40 to +85°C

Temperature range: -40 to +85°C

Load condition: parallel load 15pF

Padding capacitor: 18-22pF (tune for desired tolerance)

The system clock defines the burst frequency at which data is transmitted over the optical link via the optical interface. The receive circuitry within the ACS4110 recovers the clock from the received data at the RXDAT inputs and produces a clock that is synchronised to the incoming data stream. The system clock must have a maximum tolerance of +/-50ppm over the desired temperature range.

Optical Operational Modes

The ACS411CS has four optical operational modes, all supporting twin fiber. The ACS9020 can also utilise Lasers/LED and PIN combinations, including a PIN with an internal Trans-Impedence Amplifier (TIA) controlled by PINRX.

The twin fiber Laser modes in Table 1 may be converted to single fiber operation simply by interfacing to Wave Division Multiplexer (WDM) device indicated by mode 5.

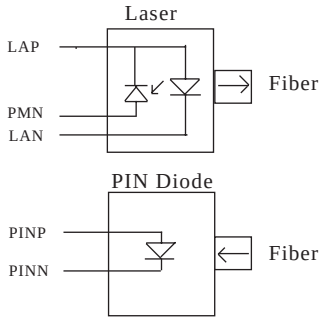
Mode	Optical Device
1	Laser and PIN diode without TIA.
2	Laser and PIN diode with integrated TIA.
3	LED and PIN diode without TIA.
4	LED and PIN diode diode with integrated TIA.
5	WDM

Table 1: Optical modes

Mode 1 - Laser & PIN without integrated TIA

In mode 1, the device is configured for use with a Laser and a PIN Diode without a TIA. In this configuration it is important to employ the TIA available within the ACS9020. The ACS9020 TIA is activated by setting PINRX = High.

In this configuration, the PIN Diode should be connected to the PINP/PINN pins so that the TIA/ Post-Amp combination on the ACS9020 is used.

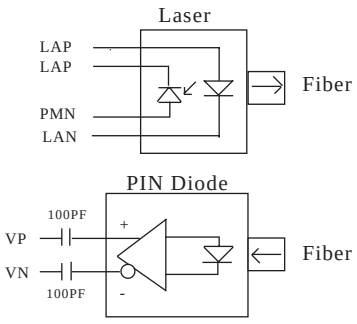


Mode 1: 3-pin Laser and PIN.

Mode 2 - Laser and & PIN Receiver with a TIA.

In mode 2, the device is configured for use with a Laser and PIN Diode with an integrated TIA (Pin Receiver). In this mode it is important to bypass the TIA on the ACS9020 device.The VP/VN inputs are activated by setting PINRX = Low.

In this mode, the outputs from the PIN Receiver should be connected to the VP/VN inputs of the ACS9020 Post-Amp via AC coupling capacitors as shown in the diagram below.

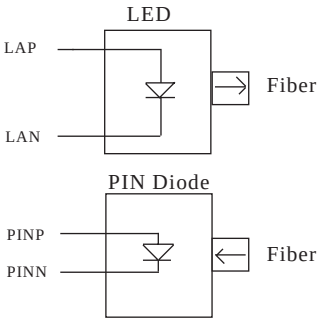


Mode 2: 4-pin Laser and PIN with integrated TIA.

Mode 3- LED & PIN without integrated TIA

In mode 3, the device is configured for use with a LED and a PIN Diode without a TIA. In this configuration it is important to employ the TIA available within the ACS9020. The ACS9020 TIA is activated by setting PINRX = High.

In this configuration, the PIN Diode should be connected to the PINP/PINN pins so that the TIA/ Post-Amp combination on the ACS9020 is used.

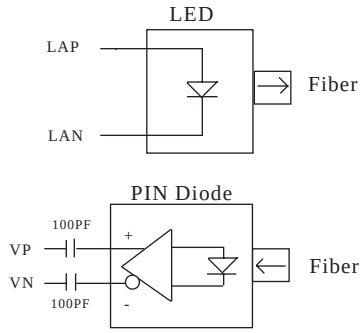


Mode 3: LED and PIN.

Mode 4 - LED & PIN with a TIA.

In mode 4, the device is configured for use with an LED and PIN Diode with an integrated TIA (Pin Receiver). In this mode it is important to bypass the TIA on the ACS9020 device.The VP/VN inputs are activated by setting PINRX = Low.

In this mode, the outputs from the PIN Receiver should be connected directly to the VP/VN inputs of the ACS9020 Post-Amp via AC coupling capacitors as shown in the diagram below.

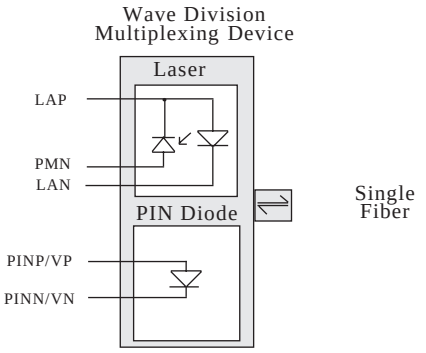


Mode 4: LED and PIN with internal TIA.

Mode 5 - WDM Bidirectional Device

The device can be configured for use with a WDM device (with and without a TIA) to realise a single fiber link. The electrical connections are the same as those for mode1 and mode2 dependent on whether the WDM bidirectional device has a TIA included or not.

If the device has a TIA integrated then the receivers Positive/Negative differential outputs are connected to VP/VN respectively via AC coupling capacitors with PINRX set Low.



WDM device containing 3-pin Laser and PIN.

If the device does not have an integrated TIA then the PIN Diodes's Cathode/Anode is connected to PINP/PINN respectively with PINRX set High.

Control of LED Current

To minimise the switching delay, a permenent bias current is maintained through the LED. A second current source called the modulation current varies the intensity of the output light power such that:

Optical Low current = Bias current.

Optical high current = Bias current + Modulation current

Unlike Lasers, LED's have a linear relationship between current and output light power. Also, the output power of LEDs does not vary significantly with temperature. Therefore, LEDs are driven with a predetermined biased current and modulation current fixed by the resistors between RBIASET and GND and RMODSET and GND respectively. In order to fix the modulation current the signal MODFIX should be set = High.

The bias current is determined by a resistor connected between pin RBIASSET and Ground.The bias current can be calculated from the formula below:

$$I_{(LAN)}(BIAS) = 50/ R_{RBIASSET}$$

Where $R_{RBIASSET}$ > 1Kohm, tolerance +/- 20%

I = Amps

The modulation current is determined by a resistor connected between pin RMODSET and Ground.The modulation current can be calculated from the formula below:

$$I_{(LAN)}(MOD) = 100/ R_{RMODSET}$$

Where $R_{RMODSET}$ > 1Kohm, tolerance +/- 20%

I = Amps

When setting the bias current and the modulation current it is important to ensure that the sum of the component currents do not exceed 100 mA.

$$I_{(LAN)} = I_{(BIAS)} + I_{(MOD)} <= 100\ mA$$

The bias current and modulation currents should be set to give the appropraite extinction ratio. The extinction ratio is the ratio of the optical high power compared to the optical low power.

Eg. An extinction ratio of 13db, is where the optical high power is 20 times the optical low power.

Control of LASER Current

To minimise switching the delay, a permenent bias current is maintained through the LASER. A second current source called the modulation current varies the intensity of the output light power such that:

Optical Low current = Bias current.

Optical high current = Bias current + Modulation current

For Lasers, there is a non-linear relationship between the output power and the applied current. In addition, Laser output power will vary significantly with temperarure for a constant current. For these reason Laser drive current must be controlled so as to maintain a constant optical output power from the Laser. The monitor pin resident in the laser converts the incident light power (typically leaked from the rear facet of the laser itself) to a monitor current, which is directly compared to a preset programmed current (the current flowing through RMODSET). The Laser drive current is automatically adjusted to maintain the original preset light level over the temperature and voltage range. The designer should be aware that whilst the control loop maintains the current generated by the monitor-pin within a tolerance of 2%, there is additional uncertainty attributed to the monitor-pin's temperature coefficient of responsivity. Data relating to the Laser characteristics should be acquired from the Laser supplier.

The bias current is set in the same way as it is for the LED driver. The bias current is determined by a resistor connected between pin RBIASSET and GND. The bias current can be calculated from the formula below:

$$I_{(LAN)}(BIAS) = 50/ R_{RBIASSET}$$

Where $R_{RBIASSET}$ > 1Kohm, tolerance +/- 20%

I = Amps

Whilst the bias current flowing through the Laser is fixed, the modulated component is automatically regulated to maintain a near constant output light power. In order to activate the automatic regulation of the modulation current it is important that the pin MODFIX is set Low.

The monitor-pin current is set by a variable resistor ($R_{RMODSET}$) connected between pin RMODSET and Ground. Acapella recommends that $R_{RMODSET}$ should comprise a logarithmic potentiometer of value 50

Kohms. It is important that $R_{RMODSET}$ is inserted and adjusted to its maximum resistance value of 50 Kohms prior to applying power to the ACS9020 for the first time and prior to following the procedure detailed in section headed, *Laser Adjustment Procedure*.

$$I_{(PMN - AVERAGE)} (BIAS + MOD) = 1/ R_{RMODSET}$$

Where $R_{RMODSET}$ > 1Kohm, tolerance +/- 20%

TXMON and TxFLG

TXMON is used to monitor the current delivered to the LED or Laser. TXMON is a current source that proportionally mirrors the current flow through the LED or Laser. By placing an appropriate external resistor R_{TXMON} between TXMON and GND, the voltage developed (referenced to GND), will be proportional to the transmit current. During the Laser setup procedure TXMON should be monitored to ensure that the Laser manufacturer's maximum current specification is not exceeded.

The transmit current monitor is a current source flowing from VDD out of pin TXMON. This current is representative of the Laser/LED drive current.

$I_{TXMON} = I_{BIAS}/50 + I_{MOD}/100$

I_{BIAS} is the Low level bias current.

I_{MOD} is the peak Modulation level bias current. The average modulation current is half this value.

Average drive current, $I_{AVG} = (I_{BIAS} + I_{MOD}) /2$

Therefore $I_{TXMON} = I_{AVG}/50$

TXMON may also be employed during normal operation to continuously check the Laser current. The voltage developed across R_{TXMON} is compared within an internally generated reference voltage of 1.25V. In the event that the reference voltage is exceeded, the TXFLAG is set High, otherwise it is set Low. In this way, the value of resistor on TXMON can be chosen to activate TXFLAG at any desired transmit current

e.g. If R_{TXMON} = 1KW, then TXFLAG will be set if I_{AVG} exceeds 62.5mA.

If desired, TXFLAG activation can be delayed by adding a damping capacitor between TXMON and GND.

Laser Adjustment Procedure

The output power from the Laser should be measured with an optical power meter during the setup procedure. In addition TXMON may be monitored to ensure that manufacturers maximum current limits are not exceeded during the set-up process. Select one of the laser drive modes in accordance with the section headed, *Optical Operational Modes.*

Start be setting the current control resistors $R_{RMODSET}$ and $R_{RBIASSET}$ to their highest values (at least 50Kohm is recommended).

The bias current is then set to the desired level by adjusting the variable resistor $R_{RBIASSET.}$ Since the bias current sets the optical low-level for the Laser, it is essential that the Laser driver data inputs are set at a continuous logic low level. The resistor value (typically a 50K potentiometer) is reduced until the desired bias current is achieved or until the desired low-level optical output power is achieved. It should be understood that since the bias current is fixed (not regulated), the low level optical output power will vary across the temperature and voltage range.

Once the bias current is set, the modulation current maybe set by adusting the variable resistor $R_{RMODSET.}$ The automatic power regulation circuitry for the modulation current maintains the average optical output power and not the peak power. For this reason, during the set-up process in the absence of the appication data, it is recommended that the Laser driver is stimulated with a square wave. Most application data used in fiber optic transmission is dc-balanced (equal number of ones and zeros), so a square-wave is an accurate representation of the real data.

The resistor value (typically a 50K potenmtiometer) is reduced until the desired optical-high ouput power is achieved. The modulation ouput power will then be regulated such that the average ouput optical output power (bias + modulation) is mainatined over the recommended temperature and voltage range.

Receive Monitor RXMON and RXFLAG

The ACS9020 incorporates a power meter which generates a current source on the RXMON pin, which is proportional to the received signal strength. A voltage is generated on an internal 50Kohm resistor which is continuously compared with an internally generated reference of 1.25 volts.

The RXFLAG is set when the RXMON voltage exceeds the 1.25 volt reference. The flag is used to indicate that there is sufficient signal strength to give a minimum differential output signal on the receiver output pins DOUTP and DOUTN. If the voltage on DOUTP/DOUTN exceeds 500 mV peak-to-peak then the RXMON voltage will exceed 1.25 Volts and the RXFLAG will be set.

Because of process tolerances on the internal resistor and the internally generated reference voltage, the RXFLAG should be considered only as a guide to the receive signal strength. The receive threshold can be adjusted by placing a 1Mohm external potentiometer between the RXMON pin and Ground.

Transmit monitor TXMON and TXFLAG

TXMON is used to monitor the current delivered to the LED or Laser. TXMON is a current source that proportionally mirrors the current flow through the LED or Laser. By placing an appropriate external resistor R_{TXMON} between TXMON and GND, the voltage developed (referenced to GND), will be proportional to the transmit current. During the Laser setup procedure TXMON should be monitored to ensure that the Laser manufacturer's maximum current specification is not exceeded.

The transmit current monitor is a current source flowing from VDD out of pin TXMON. This current is representative of the Laser/LED drive current.

$I_{TXMON} = I_{BIAS}/50 + I_{MOD}/100$

I_{BIAS} is the Low level bias current.

I_{MOD} is the peak Modulation level bias current. The average modulation current is half this value.

Average drive current, $I_{AVG} = (I_{BIAS} + I_{MOD}) /2$

Therefore $I_{TXMON} = I_{AVG}/50$

TXMON may also be employed during normal operation to continuously check the Laser current. The voltage developed across R_{TXMON} is compared within an internally generated reference voltage of 1.25V. In the event that the reference voltage is exceeded, the TXFLAG is set High, otherwise it is set Low. In this way, the value of resistor on TXMON can be chosen to activate TXFLAG at any desired transmit current

e.g. If R_{TXMON} = 1KΩ, then TXFLAG will be set if I_{AVG} exceeds 62.5mA.

If desired, TXFLAG activation can be delayed by adding a damping capacitor between TXMON and GND.

Receive Monitor RXMON and RXFLAG

The ACS9020 incorporates a power meter which generates a current source which is proportional to the received optical current.

There is an internal resistor of value of 50KΩ +/- 20 % connected between RXMON and GND which converts the current into a voltage.

RXMON is compared with 1.25V. If RXMON exceeds 1.25V, then output RXFLAG is set = 1, otherwise RXFLAG is set = 0. With the internal resistor of 50KΩ. By adding an external parallel resistor between RXMON and GND, this threshold may be increased.

Transmission Clock TCLK

There are 16 independent Transmit clocks TCLK(16:1) on the ACS4110. For the purpose of this specification, these signals will be referred to collectively as TCLK. The ACS4110 gives a choice between internally and externally generated transmit clocks. When the CKC pin is held Low, the set of TCLK clocks are configured as outputs producing a clock at the frequency defined by DR(3:1).

When the CKC pin is held High, the set of TCLK clocks are configured as inputs, and will accept an externally produced transmission clock with a tolerance of up to 250ppm with respect to the transmission rate determined by DR(3:1).

The data appearing on TPOS/TNEG is valid on the rising or falling edge of the TCLK clock dependent on the setting of TRSEL *(see Figure 22. Timing diagrams)*. This is the case for both internally and externally generated transmission clocks.

Receive Clock RCLK

There are 16 independent Receive clocks RCLK(16:1) on the ACS4110. For the purpose of this specification, these signals will be referred to collectively as RCLK.

The data appearing on RPOS/RNEG is valid on the rising or falling edge of the RCLK clock dependent on the setting of RESEL *(see Figure 22. Timing diagrams)*. To ensure that the average receive frequency is the same as the transmitted frequency, RCLK is generated from a Phase-Lock Loop (PLL) system (except where master mode has been selected). The PLL makes periodic corrections to the output RCLK clock by subtracting or adding a single crystal clock bit-period, so that the average frequency of the RCLK clock tracks the average frequency of the transmit clock of the far-end modem (or system master clock). This decompression/de-jittering function is covered in more detail in section headed, *Jitter Characteristics.*

The recovery and de-jittering functions comply to jitter tolerance and jitter transfer specifications of the selected data rates. The algorithm that determines the transfer function and response of the PLLs is modified (shaped) according to the selected data rate.

System Frequencies and Clock Generation

The crystal clock frequency and the multiplying factors of the MPLL are determined by the choice of data rates. Table 2 lists the required frequencies of the system.

Mode	Data Rate MHz	XTAL MHz	Fsys MHz
16 x T1	1.544	23.160	69.480
16 x E1	2.048	22.528	67.584
7 x T2	6.312	23.144	69.432
4 x E2	8.448	22.528	67.584
1 x E3	34.368	22.912	68.736
1 x T3	44.736	22.368	67.104
1 x OC1	51.840	25.920	77.760

Table 2: System frequencies

Data Coding

The main synchronous channels may use any of the following coding methods: NRZ, AMI, HDB3, B3ZS, B6ZS and B8ZS. The desired mode is selected by POL(3:1) input pins, as shown in Table 3.

Data Coding	POL3	POL2	POL1
NRZ	0	0	0
AMI	0	0	1
HDB3	0	1	0
B8ZS	0	1	1
B6ZS	1	0	0
B3ZS	1	0	1
NRZ	1	1	0
NRZ	1	1	1

Table 3: Line coding selection

For Non-Return-to-Zero (NRZ) coding, data is applied directly to TPOS inputs, and output data appears only on the RPOS output pins. When using NRZ code, unconnected TNEG input pins will automatically pull-up to VD+. In addition, the ACS411CS will assert a continuous Low on redundant RNEG output pins.

AMI, B3ZS, B6ZS, B8ZS and HDB3 coding is normally bipolar. However, it is possible to interface with the ACS411CS using two inputs and outputs rather than a single bipolar interface. Data equivalent to positive excursions of the bipolar AMI/BxZS/HDB3 signal are applied as a logic High to TPOS, while data equivalent to negative excursions are applied as a logic High to TNEG. Similarly, AMI/BxZS/HDB3 positive excursions will appear as a logic High on RPOS and negative excursions will appear as a logic High on RNEG.

It is anticipated that most users of the ACS411CS will interface directly with a E1/T1 framers. All the popular framers provide POS/NEG bipolar interfaces which will directly connect to the ACS4110.

If required, a detailed description of the AMI/HDB3/BxZS coding rules are available from Acapella.

Data Rate Selection

For the purpose of this specification TPN1 represents the set of signals TPOS1 and TNEG1, and RPN1 represents the set of signals RPOS1 and RNEG1. See section headed, *Data Coding* for a description of the coding types.

The maximum recommended crystal (XTAL) is 26.88MHz. An internal multiplier factors the XTAL frequency by 3. The maximum bandwidth is 51.840MHz (OC1). This bandwidth can be utilised in various ways, it may be divided up over 1, 4, 7 or 16 channels.

All 16 main channels are completely independent. One channel consists of the following 6 signals:

Transmit side:
TPOS +ve in bipolar signal or NRZ data
TNEG -ve in bipolar signal TPOS
TCLK transmit clock (internal or external)
Receive side:
RPOS +ve in bipolar signal or NRZ data
RNEG -ve in bipolar signal or NRZ data
RCLK receive clock

The data rate can be selected via the data rate selection bits DR(4:1), either directly via pins or via the microprocessor interface. The selection determines the number of active channels in combination with the selected crystal frequency and the line data rate in accordance with Table 4.

DR Pins 3	2	1	TCLK (MHz)	Nos. of channels	Tmode
1	1	0	1.544	16	16 x T1
1	0	1	2.048	16	16 x E1
1	0	0	6.312	7	7 x T2
0	1	1	8.448	4	4 x E2
0	1	0	34.368	1	1 x E3
0	0	1	44.736	1	1 x T3
0	0	0	51.840	1	1 x OC1

Table 4: Data rate and channel selection

Channels not used in a specific mode are disabled. For example in 4 x E2 mode channels 1 to 4 are carrying E2 data rates, and channels 5 to 16 are disabled. All channels can be disabled individually via the microprocessor interface, or alternatively via far-end remote control.

Diagnostic modes (main channel)

The ACS4110 has four diagnostic/configuration modes implemented for the main channels, configured by CM(3:1). The following diagnostic / configuration modes are implemented for the main channels:

- full duplex
- full duplex slave
- full duplex master
- remote loop-back
- local loop-back

The modes are selectable via CM(3:1) either directly via pins, via the microprocessor interface or via remote control setup. All modes remote loop-back and local loop-back are selectable individually for each channel via the microprocessor interface. Table 5. shows the selection of diagnostic modes and configurations.

CM(3:1)	Diagnostic Mode/Configuration
111	local loop-back initiated from far end (remote setup only)
110	remote loop-back initiated from far end
101	local loop-back
100	remote loop-back
011	full duplex master
010	full duplex slave
001	full duplex slave/remote full duplex (remote setup only)
000	full duplex

Table 5: Selection of diagnostic modes

In remote setup (ENRSB=0), the far-end device will be setup complementary to the near-end device (control device) according to the Table 6.

CM(3:1)	Near End initiate (Control device)	Far End initiate (Remote control device)
111	full duplex	local loop-back
110	*	remote loop-back
101	local loop-back	full duplex
100	remote loop-back	*
011	full-fuplex master	full-duplex slave
010	full-duplex slave	full-duplex master
001	full-duplex slave	full-duplex
000	full duplex	full duplex

Table 6: Selection of diagnostic modes

* Remote Loop-back Detect.

For a remote loop-back initiated from the far end device, CM(3:1)=110, the initiating end transmitting and receiving the data will be setup as full duplex (see Figure:1).

For remote loop-back, CM(3:1)=100, the remote loopback is initiated from the near end.

In both cases, the data that is looped back will be the data applied to the near end device (see Figure:1).

All modes are selectable via CM(3:1) either directly via pins or via the microprocessor interface. All the diagnostic modes, including remote loop-back and local loop-back are selectable individually for each main and maintenance channel via the microprocessor interface.

Full-Duplex

In the full-duplex configuration, the RCLK clock of both devices track the average frequency of the corresponding TCLK clock of the opposite end of the link. The receiving Digital-Phase-Lock Loop (DPLL) system makes periodic adjustments to the RCLK clock to ensure that the average frequency is exactly the same as the far-end TCLK clock. In summary, each TCLK is an independent master clock and each RCLK a slave of the far-end TCLK clock.

The relationship between TmCLK and RmCLK are treated similarly.

Full-Duplex Slave

In slave mode, the TCLK and RCLK clock is derived from the TCLK clock of the far-end modem, such that their average frequencies are identical. Clearly, it is essential that only one modem within a communicating pair is configured in slave mode. The CKC pin should be forced to GND, so that TCLK is always configured as an output.

The relationship between TmCLK and RmCLK are treated similarly. The CKM pin should be forced to GND, so that TmCLK is always configured as an output.

Full-Duplex Master

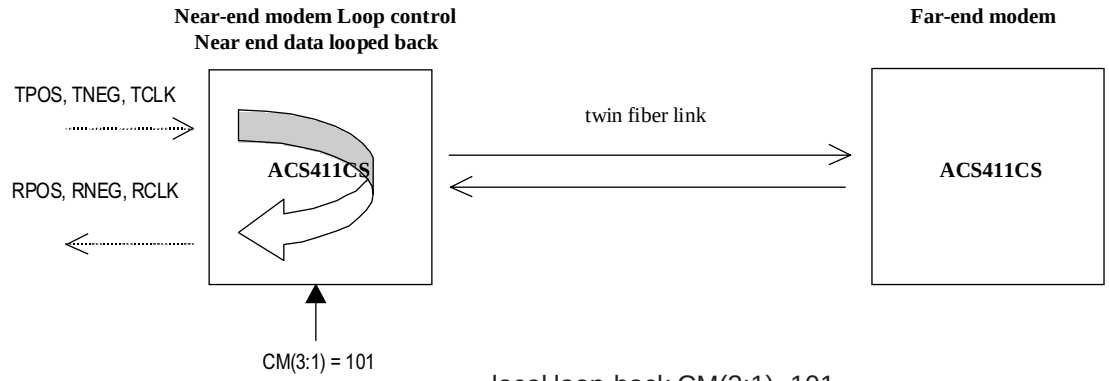
In master mode, the local RCLK clock is internally generated from the local TCLK clock. The local TCLK clock may be internally or externally generated. Master mode is only valid if the far-end device is configured in slave mode or if the far-end TCLK clock is derived from the far-end RCLK clock. Only one modem within a communicating pair may be configured as a master.

The relationship between TmCLK and RmCLK are treated similarly.

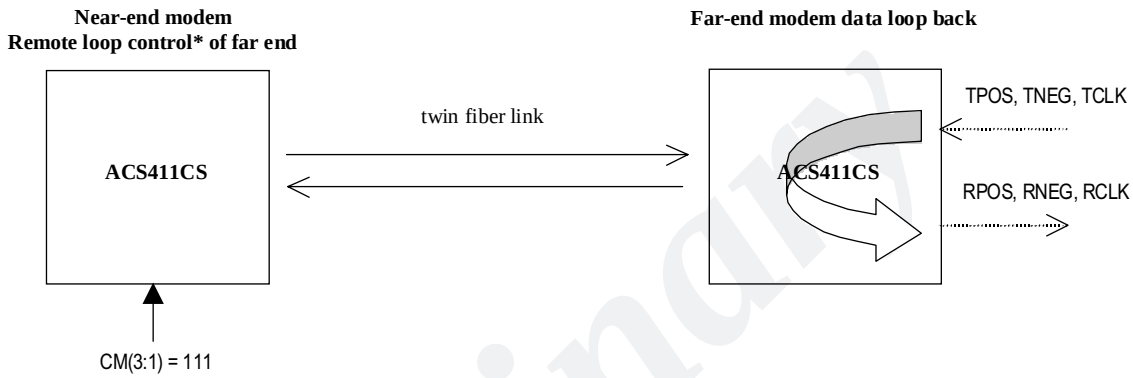
Local Loopback

In local loopback mode, TPN and TmD data is looped back inside the near-end modem and is output at its own RPN and RmD outputs.

Data received from the far-end device is ignored, except to maintain lock. If concurrent requests occur for local and remote loopback, local loopback is selected. The local loopback diagnostic mode is used to test data flow up to, and back from, the local ACS4110 and does not test the integrity of the link itself. Therefore, local loopback operates independently of synchronisation with a second modem (i.e. DCD may be High or Low). The local

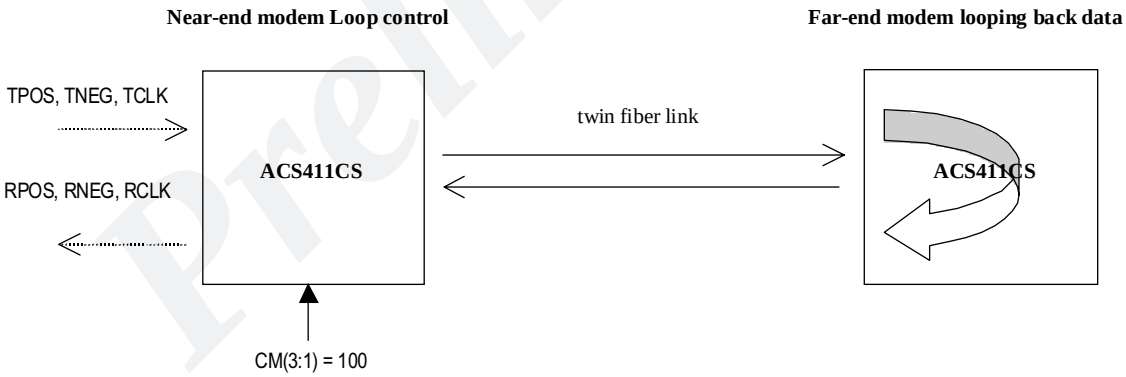


local loop-back CM(3:1)=101

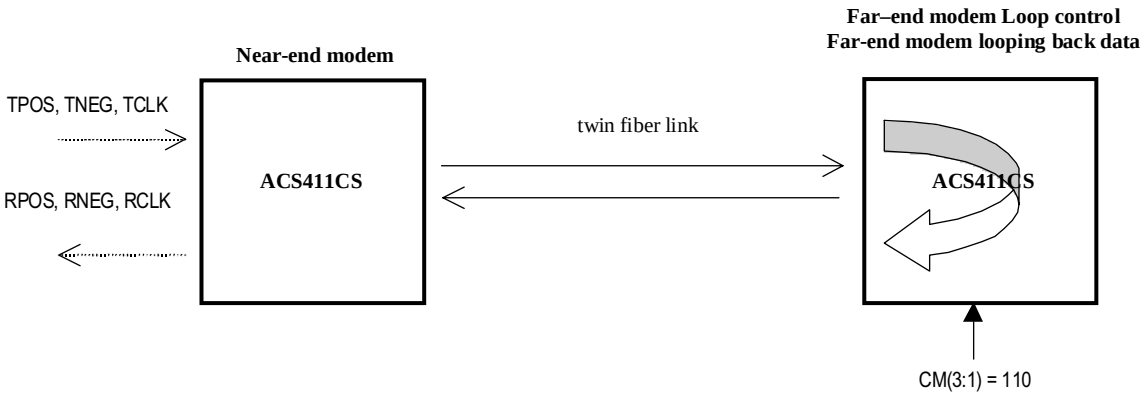


local loop-back initiated by far end modem CM(3:1)=111

Figure 1: Local loopback control configurations.



Remote loop-back CM(3:1)=100



Remote loop-back initiated by far end modem CM(3:1)=110

Figure 2: Remote loopback control configurations.

loopback test can be initiated via the microprocessor interface (in all microprocessor modes), giving independent control for each channel. All channels can be simultaneously initiated into local loopback when the microprocessor mode is disabled via the CM(3:1) pins.

Remote Loopback

In remote loopback mode, both modems are exercised completely, as well as the Lasers/LEDs and the fiber optic link. The remote loopback test is normally used to check the integrity of the entire link from the near-end (initiating modem).

Whilst a device is responding to a request for remote loopback from the far-end, requests from the near-end to initiate remote loopback will be ignored.

The remote back request can be initiated by either the near end modem (the near-end modem sends a request to the far-end modem to loopback its received data) or by the far end modem itself. In both cases the far end modem loops back the received data to the near end.

The remote loopback test can be initiated via the microprocessor interface (in all microprocessor modes), giving independent control for each channel. All channels can be simultaneously initiated into remote loopback when the microprocessor mode is disabled via the CM(3:1) pins.

Maintenance channel

The ACS4110 offers up to 2 synchronous maintenance channel consisting of the following signals:

Transmit Side

TMD1	transmit NRZ data/framing
TMD2	transmit NRZ data/framing
TmCLK	transmit clock (internal or external)

Receive Side

RMD1	receive NRZ data/framing
RMD2	receive NRZ data/framing
RmCLK	receive clock

Maintenance Data Rate Selection

The data rate can be selected via the maintenance data rate selection bits MSEL(3:1), either directly via pins or via the microprocessor interface.

TMD1/RMD1 and TMD2/RMD2 support up to 256kbps synchronous data synchronised to TmCLK/RmCLK. They can be used as two independent channels giving a total available bandwidth to 512kbps.
Alternatively, TMD1 or TMD2, together with a specific data rate selection, can be used to divide the bandwidth of the remaining maintenance channel into sub-channels with a certain data rate, defined in Table 7.

MSEL(3:1)	Data Rate (kbps)
101	8
100	16
011	32
010	64
001	128
000	256

Table 7: Maintenance Channel Data Rate Selection

For example: 4 x 16kbps maintenance channels.
select MSEL(3:1) = 010, total available bandwidth on TMD1 is 64kbps and frame every 4th bit. The "framing" channel TMD2 is bit locked to the data channel TMD1.

Diagnostic Modes and Configuration

The diagnostic and configuration modes available for the main channels are also available for the maintenance channels. CM(3:1) also controls the maintenance channels, while all modes including remote loopback and local loopback are also selectable individually via the microprocessor interface.

Transmit and Receive Clock

The ACS4110 gives the choice between internally or externally generated TmCLK under the control of the CKM pin. When the CKM pin is held Low, TmCLK is configured as an output producing a clock at the data rate determined by MSEL(3:1). When the CKM pin is held High, TmCLK is configured as an input, and will accept an externally produced transmission clock at the data rate determined by MSEL(3:1).

Input data appearing on the TMD1/2 inputs is latched into the device on either the rising or falling edge of the TmCLK clock depending on the setting of TRSEL. This data appears at the RMD1/2 outputs of the far-end modem on the rising or falling edge of the RmCLK clock depending on the setting of RESEL (*see Figure 21. Timing diagrams*). To ensure that the average receive frequency is the same as the transmitted frequency, RmCLK is generated from a Digital Phase-Lock Loop (DPLL) system.

Whilst the TMD1/RMD1 and TMD2/RMD2 maintenance channels have a fixed phase relationship with each other, they do not have a fixed phase relationship with the main TPOS/TNEG data transmission channels.

TmCLK and the reference clock for the (digital) clock recovery and de-jittering PLLs (DPLL) for RmCLK are derived digitally from the system clock for 256kbps by the division factors shown in Table 8. If lower data rates than 256kbps are selected, the 256kHz clock will be divided down by a factor 2/4/8/16/32 determined by MSEL(3:1).

Mode	FSys/256 kbps
16 x T1	271.40625
16 x E1	264
7 x T2	271.21875
4 x E2	264
1 x E3	268.5
1 x T3	262.125
1 x OC1	303.75

Table 8: System Clock Division Factors for Maintenance Clock Generation (256kbps)

ERRC and ERRL - Error Detection

These signals can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the data, maintenance and TCLK inputs, the ACS411CS modem transmits data over the link in each direction at the Fsys system frequency. This transmit and control data is used to maintain the timing and synchronisation.

The transmit and control data is constantly monitored to make sure it is compatible with the 8B10B format. If a coding error is detected ERRL will go High and will remain High until reset. ERRL may be reset by asserting PORB, or by removing the fiber optic cable from one side of the link thereby forcing the device temporarily out of lock.

ERRC produces a pulse on detection of each coding error. These pulses may be accumulated by means of an external electronic counter. In the microprocessor modes, the value on an internal accumulating 8 bit counter can be read via the bus interface address 0x1D.

Please note that ERRL and ERRC detect 8B10B coding errors and not data errors, nevertheless because of the complexity of the coding rules employed on the ACS411CS, the absence of detected errors on these pins will give a good indication of a high quality link.

Microprocessor Interface

Bus Interface Mode Selection

The ACS4110 incorporates an 8-bit parallel microprocessor bus interface, which can be configured for the following modes via the bus interface mode control pins UPSEL(3:1) as defined in Table 9.

UPSEL(3:1)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Table 9: Microprocessor Interface Mode Selection

Note: Bit 0 is the least significant bit for all modes used here, and the byte structure complies to little endian format (byte 0 is least significant and stored at lowest address).

In OFF Mode, the bus interface is disabled. Control of the device is solely via I/O pins. This will result in limited programmability, as for example individual set-ups for remote loop-back and local loop-back for each channel are not possible, only a collective one. In this mode, all BUS I/O pins are tri-stated or used as additional input pins (ie. POL(3:1), CKLOCAL).

EPROM mode

The EPROM mode (UPSEL = 1) enables the device to read its set-up from a memory device. An internal state machine controls the access to the memory. All addresses in the memory map are read, and the device is set up according to the corresponding data. The access time is scaled to interface with the AMD AM27C020 at lowest speed (250ns) specification.

The valid read addresse 0, 0xAA is used to check if a memory device is actually attached to the device. If no memory is attached, the bus interface reverts to the default OFF mode. All other read addresses are not valid. The bus interface pins used in EPROM mode are defined in Table 10.

Pin	Dir	Description
CSB	O	Active low chip select/output enable
A(4:0)	O	Address output to EPROM
AD(7:0)	I	Data input from EPROM

Table 10: uP Bus Interface Pins for EPROM mode.

MULTIPLEXED mode

The MULTIPLEXED mode (UPSEL = 2) enables the ACS4110 to interface with a microprocessor using a combined multiplexed address/data bus. The bus interface pins are defined in Table 11.

Pin	Dir	Description
CSB	I	Active low chip select
ALE	I	Address latch enable
RDB	I	Active low read enable
WRB	I	Active low write enable
AD(7:0)	IO	Address / Data bus
RDY	O	Ready

Table 11: uP Bus Interface Pins for MULTIPLEXED mode.

INTEL mode

The INTEL mode (UPSEL = 3) enables the ACS4110 to interface with a Intel 80x86 type microprocessor bus. The bus interface pins used are defined in Table 12.

Pin	Dir	Description
CSB	I	Active low chip select
RDB	I	Active low read enable
WRB	I	Active low write enable
A(4:0)	I	Address bus
AD(7:0)	IO	Data bus
RDY	O	Ready

Table 12: uP Bus Interface Pins for INTEL mode.

MOTOROLA mode

The MOTOROLA mode (UPSEL = 4) enables the ACS4110 to interface with a Motorola 680x0 type microprocessor bus. The bus interface pins used are defined in Table 13.

Pin	Dir	Description
CSB	I	Active low chip select
WRB	I	Read / write bar select
A(4:0)	I	Address bus
AD(7:0)	IO	Data bus
RDY	O	Active low data transfer acknowledge (DTACK)

Table 13: uP Bus Interface Pins for MOTOROLA mode.

SERIAL mode

The SERIAL mode (uPSEL = 5) enables the ACS4110 to interface with a serial microprocessor bus. The bus interface pins are defined in Table 14.

Pin	Dir	Description
CSB	I	Active low chip select
ALE	I	= SCLK: Serial interface clock
A(1)	I	= CLKE: Active SCLK edge selection control bit
A(0)	I	= SDI: Serial data input
AD(0)	O	= SDO: Serial data output

Table 14: uP Bus Interface Pins for SERIAL mode.

Remote Control

The device setup of one modem can be over-ridden with the device set up from the other modem when remote control is enabled from the ENRSB pin. To enable remote control mode, ENRSB pin is held Low (Logic 0). If a modem is set up in remote control, the data from the control modem overides the local microprocessor interface or pin set-up of the remote controlled modem. The signals that will be over-ridden are defined in Table 15.

Name	Description
ch_enb(16:1)	Channel enable defined in local microprocessor for individual channel setup
DR(3:1)	Data rate select
POL(3:1)	Line code polarity select
CM(2:1)	Configuration mode(full-duplex/master/slave)
TRSEL	Clock edge select for transmit clocks
RESEL	Clock edge select for receive clocks
CKM	Clock direction select maintenance channel
CKC	Clock direction select main channels(combined)
MSEL(3:1)	Maintenance channel data rate select

Table 15: Remote Control Device Setup.

Remote control is only possible in one direction (only one modem allowed with ENRSB = 0).

The near-end modem has to be setup as the control device (ENRSB=0) in order to configure the far-end by remote control. If both modems are setup as control devices (ENRSB=0), data transmission and reception will be disabled.

When in remote setup, the signal CKLOCAL selects whether the Tx/Rx clock settings (CKC, CKM, RESEL, TRSEL, trsel_m and resel_m) should be taken from the controlling device (CKLOCAL=0) or locally (CKLOCAL=1).

The diagram in Figure 1 shows the configurations in Remote Control mode.

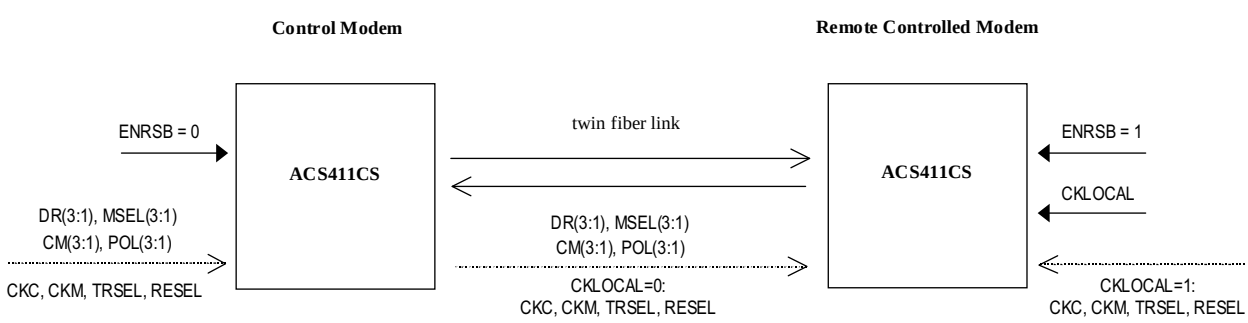
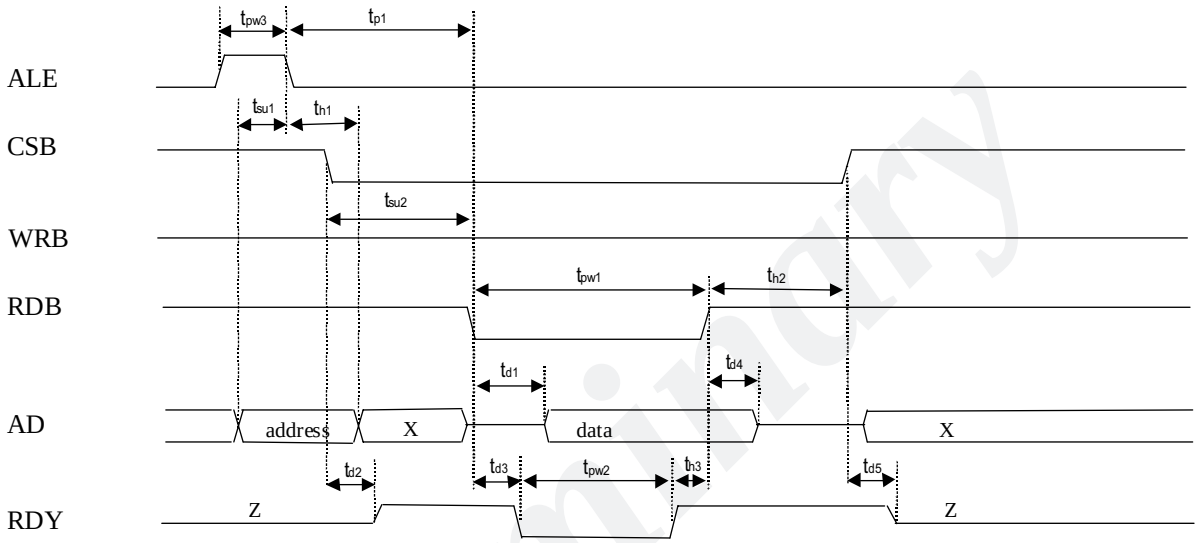


Figure 3: Remote Control Mode and ENRSB.

uP Interface timing - MULTIPLEXED mode

In MULTIPLEXED mode, the device is configured to interface with a microprocessor using a multiplexed address/data bus. The following figures show the timing diagrams of write and read accesses for this mode.

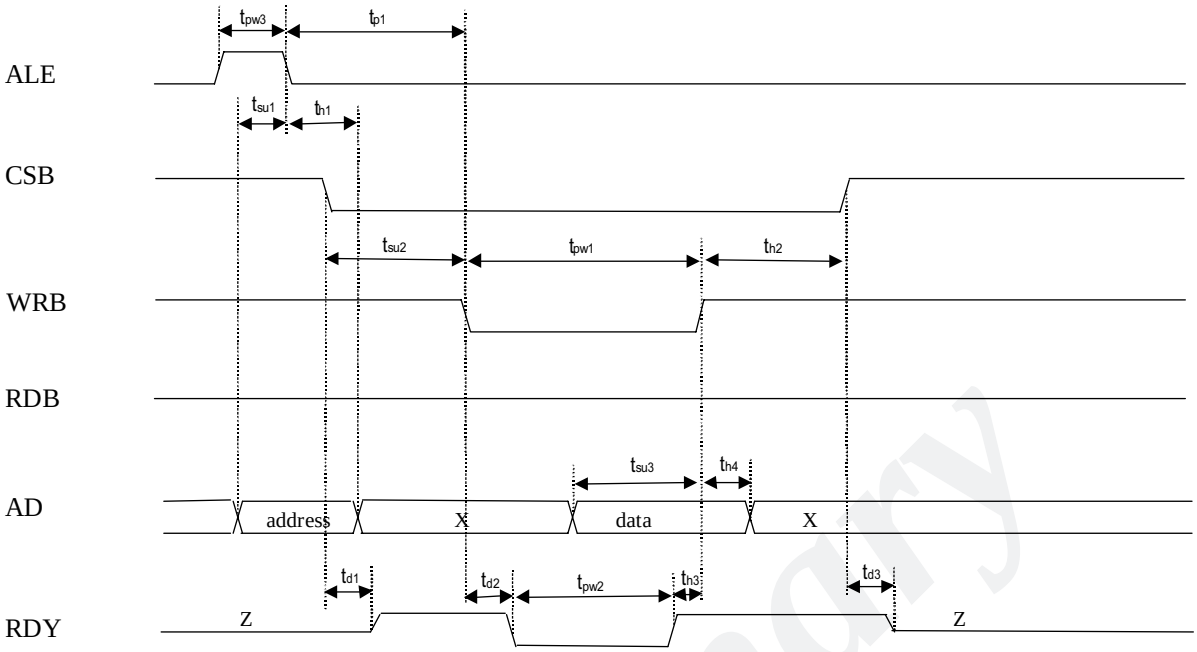
The RDY low time Trdy is at least 2 CLKX cycles after WRB/RDB going low.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup AD address valid to ALE ↓	5 *		
tsu2	Setup CSB ↓ to RDB ↓	0		
td1	Delay RDB ↓ to AD data valid			10 *
td2	Delay CSB ↓ to RDY active			10 *
td3	Delay RDB ↓ to RDY ↓			10 *
td4	Delay RDB ↑ to AD data High-Z			10 *
td5	Delay CSB ↑ to RDY High-Z			10 *
tpw1	RDB low time	60		
tpw2	RDY low time	20		60
tpw3	ALE high time	10 *		
th1	Hold AD address valid after ALE ↓	5 *		
th2	Hold CSB low after RDB ↑	0		
th3	Hold RDB low after RDY ↑	0		
tp1	Time between ALE ↓ and RDB ↓	0 *		
tp2	Time between consecutive accesses (RDB ↑ to ALE ↑)	60		

Figure 4: Read access timing in MULTIPLEXED Mode.

Note: preliminary timing information. Timing values marked with * TBA.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup AD address valid to ALE ↓	5 *		
tsu2	Setup CSB ↓ to WRB ↓	0		
tsu3	Setup AD data valid to WRB ↑	10 *		
td1	Delay CSB ↓ to RDY active			10 *
td2	Delay WRB ↓ to RDY ↓			10 *
td3	Delay CSB ↑ to RDY High-Z			10 *
tpw1	WRB low time	60		
tpw2	RDY low time	20		60
tpw3	ALE high time	10 *		
th1	Hold AD address valid after ALE ↓	5 *		
th2	Hold CSB low after WRB ↑	0		
th3	Hold WRB low after RDY ↑	0		
th4	AD data hold valid after WRB ↑	5 *		
tp1	Time between ALE ↓ and WRB ↓	0 *		
tp2	Time between consecutive accesses (WRB ↑ to ALE ↑)	60		

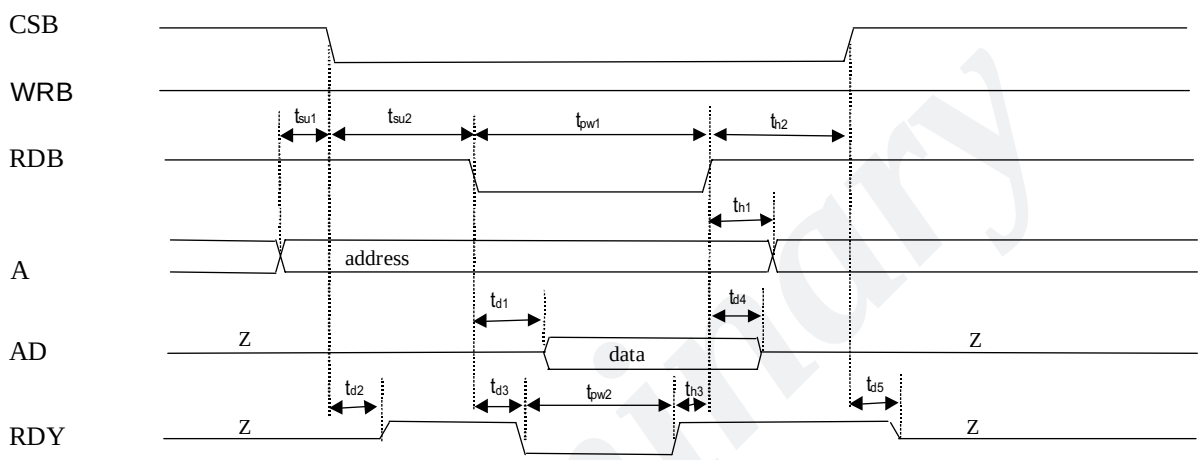
Figure 5: Write access timing in MULTIPLEXED Mode.

Note: preliminary timing information. Timing values marked with * TBA.

uP Interface timing - INTEL mode

In INTEL mode, the device is configured to interface with a microprocessor using a 80x86 type bus. The following figures show the timing diagrams of write and read accesses for this mode.

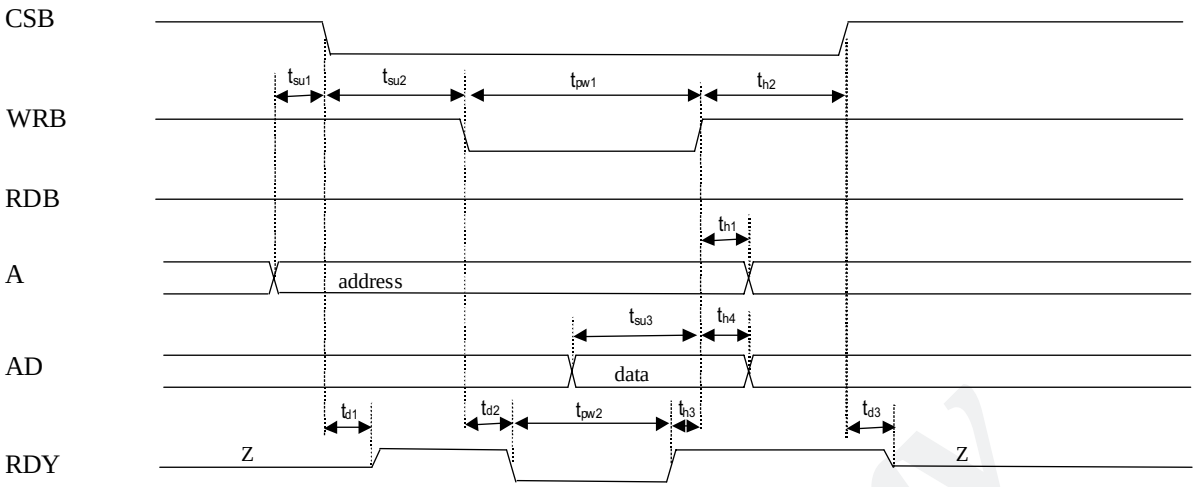
The RDY low time Trdy is at least 2 CLKX cycles after WRB/RDB going low.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup A valid to CSB ↓	0		
tsu2	Setup CSB ↓ to RDB ↓	0		
td1	Delay RDB ↓ to AD valid			10 *
td2	Delay CSB ↓ to RDY active			10 *
td3	Delay RDB ↓ to RDY ↓			10 *
td4	Delay RDB ↑ to AD High-Z			10 *
td5	Delay CSB ↑ to RDY High-Z			10 *
tpw1	RDB low time	60		
tpw2	RDY low time	20		60
th1	Hold A valid after RDB↑	0		
th2	Hold CSB low after RDB ↑	0		
th3	Hold RDB low after RDY ↑	0		
tp	Time between consecutive accesses (RDB ↑ to RDB ↓ or RDB ↑ to WRB ↓)	60		

Figure 6: Read access timing in INTEL Mode.

Note: preliminary timing information. Timing values marked with * TBA.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup A valid to CSB ↓	0		
tsu2	Setup CSB ↓ to WRB ↓	0		
tsu3	Setup D valid to WRB ↑	10 *		
td1	Delay CSB ↓ to RDY active			10 *
td2	Delay WRB ↓ to RDY ↓			10 *
td3	Delay CSB ↑ to RDY High-Z			10 *
tpw1	WRB low time	60		
tpw2	RDY low time	20		60
th1	Hold A valid after WRB ↑	5 *		
th2	Hold CSB low after WRB ↑	0		
th3	Hold WRB low after RDY ↑	0		
th4	AD hold valid after WRB ↑	5 *		
tp	Time between consecutive accesses (WRB ↑ to WRB ↓ or WRB ↑ to RDB ↓)	60		

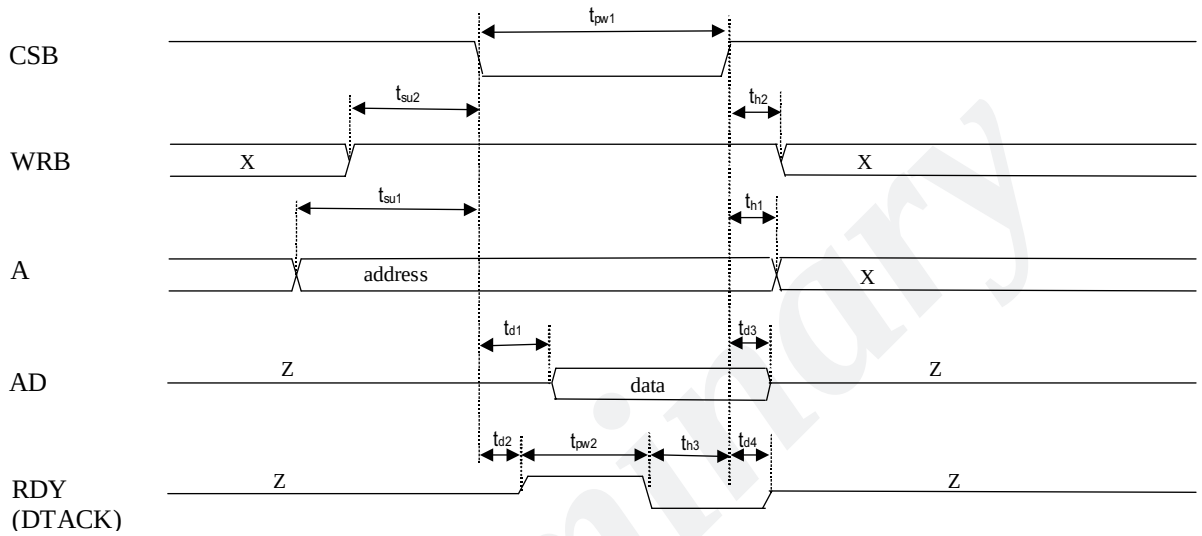
Figure 7: Write access timing in INTEL Mode.

Note: preliminary timing information. Timing values marked with * TBA.

uP Interface timing - MOTOROLA mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus. The following figures show the timing diagrams of write and read accesses for this mode.

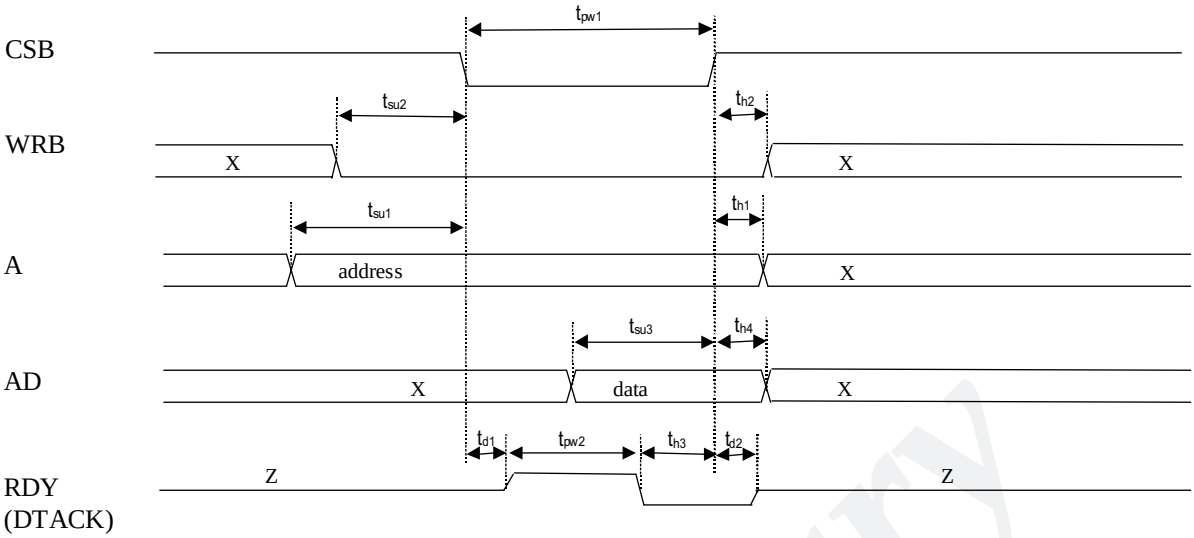
The Dtack high time Trdy is at least 2 CLKX cycles after CSB going low.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup A valid to CSB ↓	0		
tsu2	Setup WRB valid to CSB ↓	5 *		
td1	Delay CSB ↓ to AD valid			10 *
td2	Delay CSB ↓ to DTACK ↑			10 *
td3	Delay CSB ↑ to AD High-Z			10 *
td4	Delay CSB ↑ to RDY High-Z			10 *
tpw1	CSB low time	60		
tpw2	DTACK high time	20		60
th1	Hold A valid after CSB↑	0		
th2	Hold WRB high after CSB ↑	5 *		
th3	Hold CSB low after DTACK ↓	0		
tp	Time between consecutive accesses (CSB ↑ to CSB ↓)	60		

Figure 8: Read access timing in MOTOROLA Mode.

Note: preliminary timing information. Timing values marked with * TBA.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup A valid to CSB ↓	0		
tsu2	Setup WRB valid to CSB ↓	5 *		
tsu3	Setup AD valid to CSB ↑	10 *		
td1	Delay CSB ↓ to DTACK ↑			10 *
td2	Delay CSB ↑ to RDY High-Z			10 *
tpw1	CSB low time	60		
tpw2	DTACK high time	20		60
th1	Hold A valid after CSB ↑	5 *		
th2	Hold WRB low after CSB ↑	5 *		
th3	Hold CSB low after DTACK↓	0		
th4	Hold AD valid after CSB↑	5 *		
tp	Time between consecutive accesses (CSB - to CSB ↓)	60		

Figure 9: Read access timing in MOTOROLA Mode.

Note: preliminary timing information. Timing values marked with * TBA.

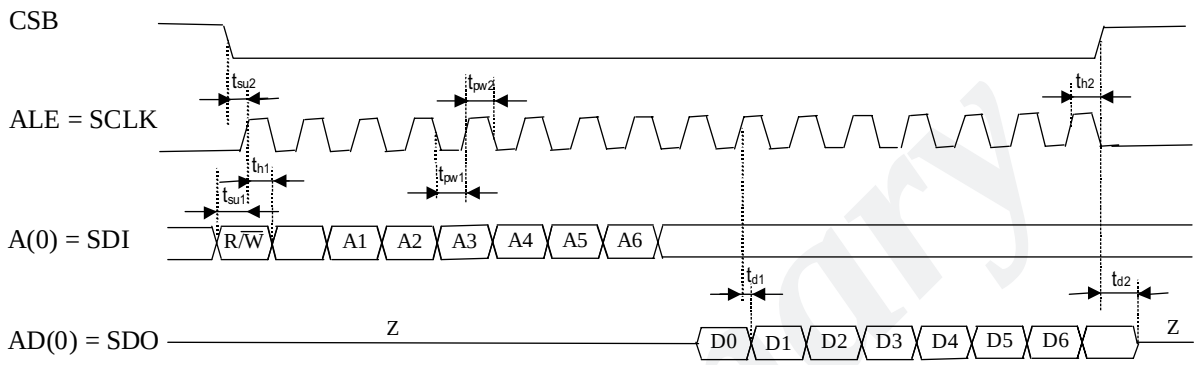
uP Interface timing - SERIAL mode

In SERIAL mode, the device is configured to interface with a serial microprocessor bus. The following figures show the timing diagrams of write and read accesses for this mode.

During read access the output data sdo (AD(0)) is clocked out on the rising edge of SCLK (ALE) when the active edge selection control bit CLKE (A(1)) is 0, and on the falling edge when CLKE is 1. Address, read/write control bit and write data are always clocked into the interface on the rising edge of SCLK.

Both input data sdi and clock SCLK are oversampled , filtered and synchronized to the system clock CLKX.

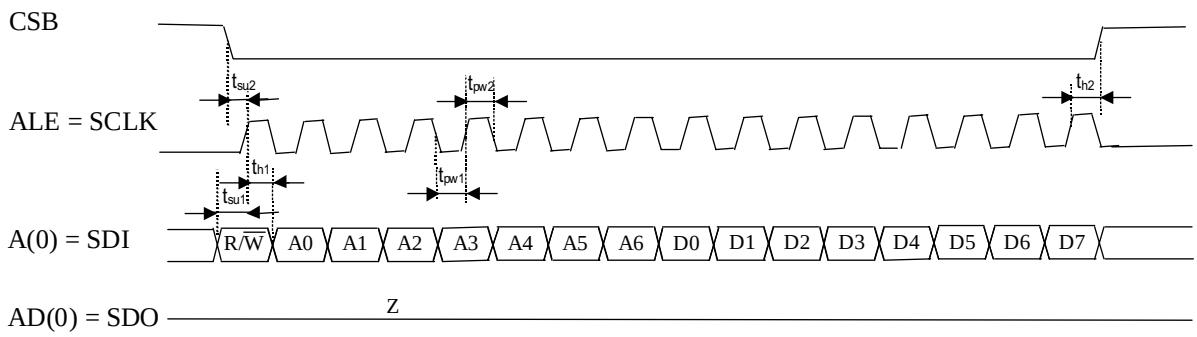
The serial interface clock (SCLK) is not required to run when no access is performed (CSB = 1).



Symbol	Parameter	Min	Typ	Max
tsu1	Setup SDI valid to SCLK ↑	10 *		
tsu2	Setup CSB ↓ to SCLK ↑	10 *		
th1	Hold SDI to SCLK ↑	10 *		
th2	Hold SCLK ↑ to CSB ↑	10 *		
tpw1	SCLK low time	240		
tpw2	SCLK high time	240		
td1	Delay SCLK ↑ (SCLK ↓ for CLKE = 1) to SDO valid			20 *
td2	Delay CSB ↑ to SDO High-Z			120
tp	Time between consecutive accesses (CSB ↑ to CSB ↓)	250		

Figure 10: Read access timing in SERIAL Mode.

Note: preliminary timing information. Timing values marked with * TBA.



Symbol	Parameter	Min	Typ	Max
tsu1	Setup SDI valid to SCLK ↑	10 *		
tsu2	Setup CSB ↓ to SCLK↑	10 *		
th1	Hold SDI to SCLK ↑	10 *		
th2	Hold SCLK ↑ to CSB ↑	10 *		
tpw1	SCLK low time	240		
tpw2	SCLK high time	240		
tp	Time between consecutive accesses (CSB ↑ to CSB ↓)	250		

Figure 11: Write access timing in SERIAL Mode.

Note: preliminary timing information. Timing values marked with * TBA.

uP Interface timing - EPROM mode

In EPROM mode, the ACS4110 takes control of the bus as master, and reads the device set-up from an AMD AM27C020 type EPROM at lowest speed (250ns) after device start-up (system reset). The EPROM access state machine in the up interface sequences the accesses. The following figures show the timing diagrams of the read access for this mode.

For a more detailed timing specification, see AMD Am27C020 data sheet, July 1993, p. 2-95.

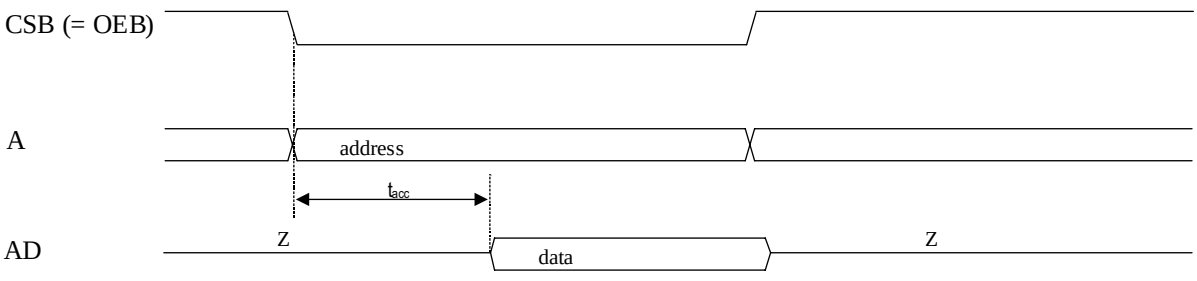
If the microprocessor interface is enabled (UPSEL / = 0), the default start-up values are taken over from the pin values as default during reset for the following control pins:

CM(3:1)

CKC, CKM, TRSEL , RESEL

MSEL(3:1), ENRSB

DR(3:1)



Symbol	Parameter	Min	Typ	Max
tacc	Delay CSB ↓ or A change to AD valid	-	-	590

Figure 12: Read access timing in EPROM Mode.

Note: preliminary timing information. Timing values marked with * TBA.

Memory Map

Table 15 shows the memory map of the ACS4110. The location names are chosen to match the corresponding pin names. Signals not directly equivalent to pins are in lower case.

The device identification number id<7:0> on address 0x00 is used in EPROM mode to check if an external memory device is connected. The value to be programmed is 0xAA.

The whole chip set-up except DR<3:1> can be controlled individually for each channel.

The error counter errc<7:0> (address 0x1D) is an 8-bit saturating counter for the ERRC error pulse. A write of a 0x00 mask to this address clears the counter to 0x00.

The status signals ERRL, fail_ne, fail_fe can also be cleared by writing a 0 to the specific bit in the address. For example, writing a mask of 0xDF to address 0x1C clears the ERRL signal, but leaves other status signals unchanged.

If the microprocessor interface is enabled (UPSEL /= 0), the default start-up values of all control bits except POL(3:1) and CKLOCAL are taken over from the pin values as default during reset.

Address	Bit	Access	Name	Description
0x00	7-0	R	id<7:0>	Device identification number.
0x01	7-0	R/W	ch_enb<8:1>	Channel enable (active low) for channels 1 to 8.
0x02	7-0	R/W	ch_enb<16:9>	Channel enable (active low) for channels 9 to 16.
0x03	7-0	R/W	cm1<8:1>	Configuration mode CM bit 1 for channels 1 to 8.
0x04	7-0	R/W	cm1<16:9>	Configuration mode CM bit 1 for channels 9 to 16.
0x05	7-0	R/W	cm2<8:1>	Configuration mode CM bit 2 for channels 1 to 8.
0x06	7-0	R/W	cm2<16:9>	Configuration mode CM bit 2 for channels 9 to 16.
0x07	7-0	R/W	cm3<8:1>	Configuration mode CM bit 3 for channels 1 to 8.
0x08	7-0	R/W	cm3<16:9>	Configuration mode CM bit 3 for channels 9 to 16.
0x09	7-0	R/W	pol1<8:1>	Line code polarity POL bit 1 for channels 1 to 8.
0x0A	7-0	R/W	pol1<16:9>	Line code polarity POL bit 1 for channels 9 to 16.
0x0B	7-0	R/W	pol2<8:1>	Line code polarity POL bit 2 for channels 1 to 8.
0x0C	7-0	R/W	pol2<16:9>	Line code polarity POL bit 2 for channels 9 to 16.
0x0D	7-0	R/W	pol3<8:1>	Line code polarity POL bit 3 for channels 1 to 8.
0x0E	7-0	R/W	pol3<16:9>	Line code polarity POL bit 3 for channels 9 to 16.
0x0F	7-0	R/W	ckc<8:1>	Clock direction select for channels 1 to 8.
0x10	7-0	R/W	ckc<16:9>	Clock direction select for channels 9 to 16.
0x11	7-0	R/W	trsel<8:1>	Transmit clock edge select for channels 1 to 8.
0x12	7-0	R/W	trsel<16:9>	Transmit clock edge select for channels 9 to 16.
0x13	7-0	R/W	resel<8:1>	Receive clock edge select for channels 1 to 8.
0x14	7-0	R/W	resel<16:9>	Receive clock edge select for channels 9 to 16.
0x15	7	-		
	6-4	R/W	cm_m<3:1>	Configuration mode CM for maintenance channel.
	3	R/W	CKLOCAL	Local Tx/Rx CLK setup in remote control mode
	2	R/W	CKM	Clock direction select maintenance channel.
	1	R/W	trsel_m	Transmit clock edge select for maintenance channel.
	0	R/W	resel_m	Receive clock edge select for maintenance channel.
0x16	7	-		
	6-4	R/W	MSEL<3:1>	Maintenance channel data rate select.
	3	R/W	ENRSB	Enable remote control setup.
	2-0	R/W	DR<3:1>	Data rate select.
0x17	7-0	R	rl_det<8:1>	Near-end remote loop-back detect channels 1 to 8.
0x18	7-0	R	rl_det<16:9>	Near-end remote loop-back detect channels 9 to 16.
0x19	7-0	R	ll_det<8:1>	Far-end local loop-back detect channels 1 to 8.
0x1A	7-0	R	ll_det<16:9>	Far-end local loop-back detect channels 9 to 16.
0x1B	7-2	-		
	1	R	rlm_det	Near-end remote loop-back detect for maintenance channel.
	0	R	llm_det	Far-end local loop-back detect for maintenance channel.
0x1C	7	R	DCD	Data carrier detect status.
	6	R	LOSS	Loss of signal status.
	5	R/W	ERRL	Error latch.
	4	-		
	3	R/W	fail_ne	Alarm indication for near-end receive fail.
	2	R/W	fail_fe	Alarm indication for far-end receive fail.
	1	R	resync_ne	Near-end device has entered re-synchronization.
	0	R	resync_fe	Far-end device has entered re-synchronization.
0x1D	7-0	R/W	errc<7:0>	8-bit saturating error counter (reset by write).
0x1E	7-0	R/W	tm<7:0>	Test mode select.
0x1F	7-0	-		

Table 15: Memory Map

Laser/LED Considerations

Since LEDs or Lasers from different suppliers may emit different wavelengths, it is recommended that the Lasers/LEDs in a communicating pair of modems are obtained from the same supplier. Acapella will assist with contact names and addresses on request.

Power Supply Decoupling

The ACS9020 contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the Laser/LED. The modem should have an independent power trace to the point where power enters the board.

The Laser/LED should be sited very close to the PMN, PINP, PINN, LAN and LAP pins. A generous ground plane should be provided, especially surrounding the sensitive PINP and PINN tracks from the ACS9020 pins to the optical component. The modem should be protected from EMI/RFI sources in the standard ways.

LOSS (Loss Of Synchronisation)

There are two conditions that will make LOSS go to Logic 1. These are:

i) Loss of synchronisation - synchronisation windows incorrectly aligned i.e DCD=0.

ii) 64 received symbols break the 8B10B encoding rules in a sequence of 256 symbols.

In order to return LOSS to the Logic 0 state the following criteria must be met:

i) The devices must be synchronised - synchronisation windows correctly aligned i.e DCD=1.

ii) There are no received symbols in a sequence of 256 symbols which break the 8B10B coding rules.

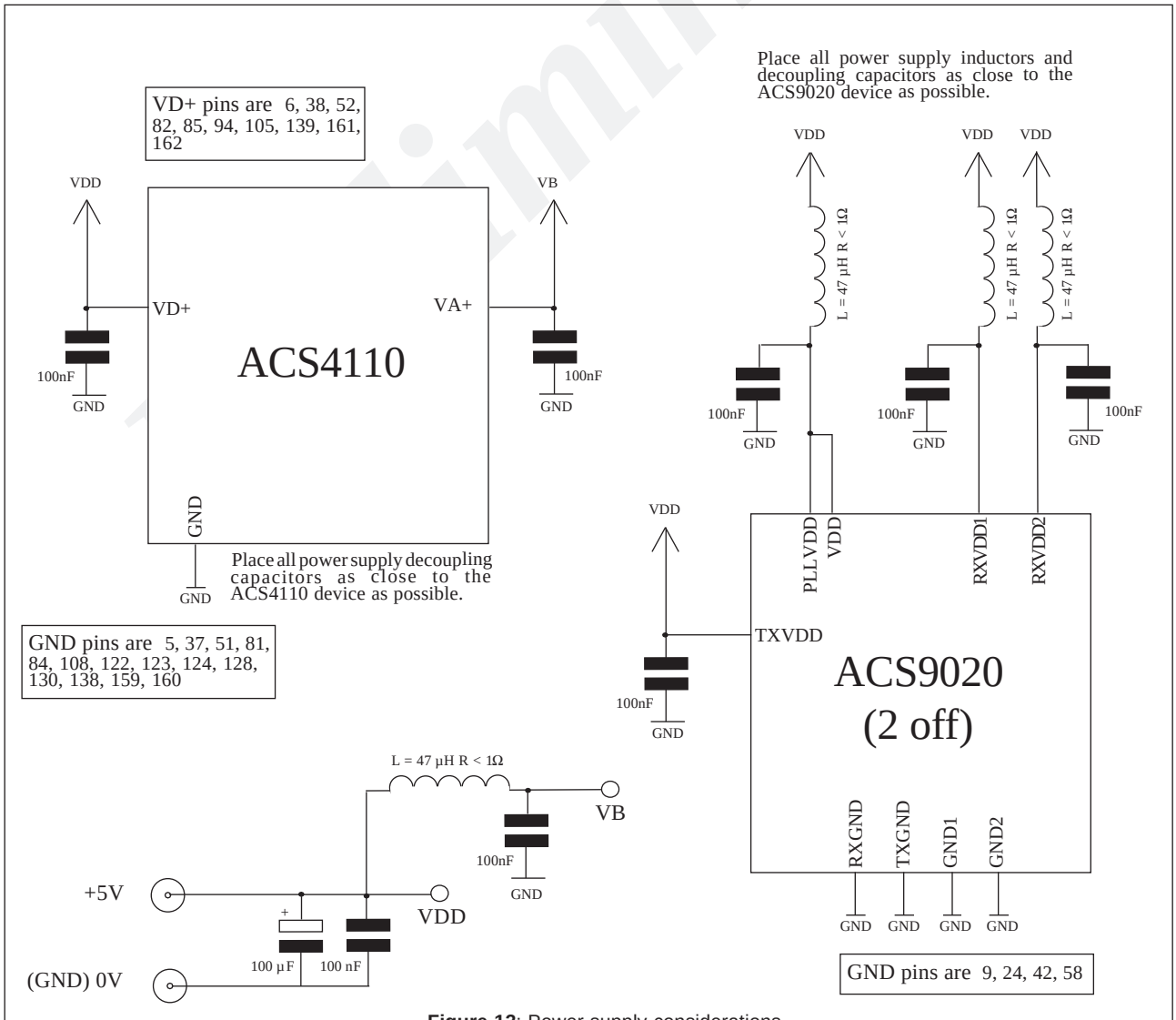


Figure 13: Power supply considerations.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit Laser/LED and the power required to realise the minimum input-amplifier current via the receive PIN/LED. The link budget is normally specified in dB, and represents the maximum attenuation allowed between communicating Lasers/LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LASER/LED performance. The power coupled to the cable is a function of the efficiency of the Laser/LED, the current applied to the Laser/LED and the type of the fiber optic cable employed.

Twin Fiber LED link (880nm LED + PIN)

Link Budget Example (Rtset set so LED launch current = 100 mA peak)

Fiber type Glass (multimode)
Fiber size 62.5micron

Minimum transmit couple power to fiber (µW)	100
Minimum PIN responsivity (A/W)	0.1
Minimum ACS9020 sensitivity (nA)	1500
Minimum input power to ACS9020 amplifier (µW)	20
Link budget (dB) (multi mode fiber attenuation = 3 dB/km)	8.24

Twin Fiber LASER link (1310nm Laser and PIN)

Link Budget Example (Rtset set so LASER launch current = 25 mA peak)

Fiber type Glass (single mode)
Fiber size 9 micron

Minimum transmit couple power to fiber (µW)	1000
Minimum PIN responsivity (A/W)	0.8
Minimum ACS9020 sensitivity (nA)	1500
Minimum input power to ACS9020 amplifier (µW)	4
Link budget (dB) (single mode fiber attenuation = 0.3 dB/km)	27

Single Fiber LASER link (1310nm and 1510nm WDM device)

Link Budget Example (Rtset set so LASER launch current = 25 mA peak)

Fiber type Glass (single mode)
Fiber size 9 micron

Minimum transmit couple power to fiber (µW)	1000
Minimum PIN responsivity (A/W)	0.8
Minimum ACS9020 sensitivity (nA)	1500
Minimum input power to ACS9020 amplifier (µW)	4
Link budget (dB) (single mode fiber attenuation = 0.3 dB/km)	27

Figure 14: Link bugdet examples.

Jitter Characteristics

The receive path includes a Phase Locked Loop block, which provides an independent PLL for each transmission channel. The purpose of each PLL is to regenerate the clock signal such that it tracks the transmit clock of the far end modem. The PLL will also attenuate the jitter present in the received data stream. For E1, E2, T1 and T2 modes, the PLL algorithm implemented is entirely digital. For E3, T3 and OC1/ STS1 modes, the PLL block utilised a mixed signal PLL algorithm. The mixed signal PLL does not require the use of external tuning components.

The dynamic range of all PLL algorithms is +/- 500ppm. The dynamic range is used to accommodate oscillator frequency differences between the two communicating modems, as well as any jitter and wander present in the received data stream.

The jitter characteristics for the ACS4110 is independent of the binary content of the transmitted data stream.

T1 Jitter specification

When configured for T1 operation, the Jitter Tolerance and Jitter Transfer performance conforms to that specified in AT&T Publication 62411.

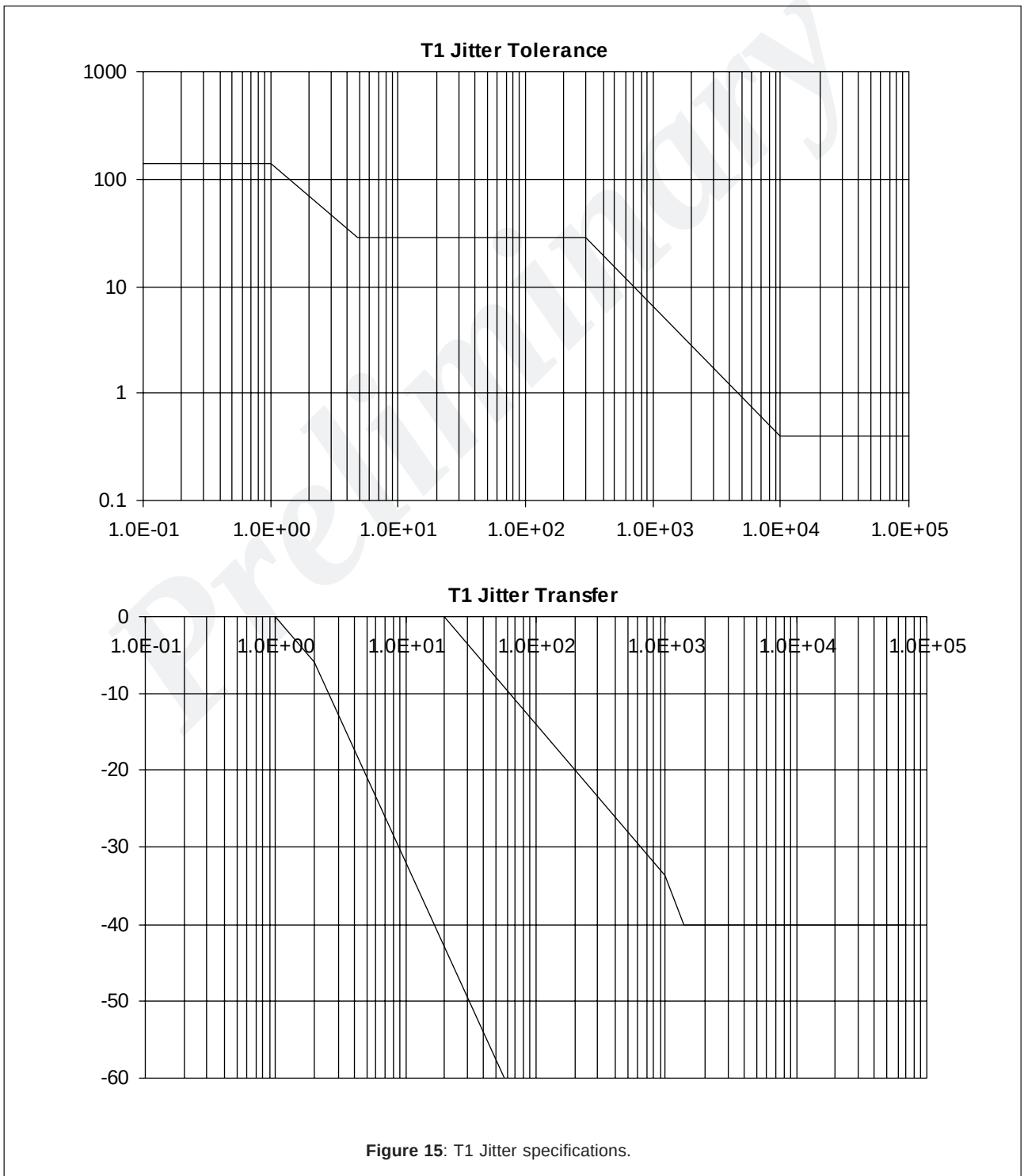


Figure 15: T1 Jitter specifications.

T2 and T3 Jitter specification

When configured for T2 operation, the Jitter Tolerance performance exceeds that specified in both ITU-T G.824 and Bellcore GR-499-CORE.

When configured for T3 operation, the Jitter Tolerance performance exceeds that specified in both ITU-T G.824 and Bellcore GR-499-CORE.

In the absence of input jitter, the output jitter generated from the mixed signal PLL after band pass filtering from 12kHz to 400kHz is 0.07UIpp.

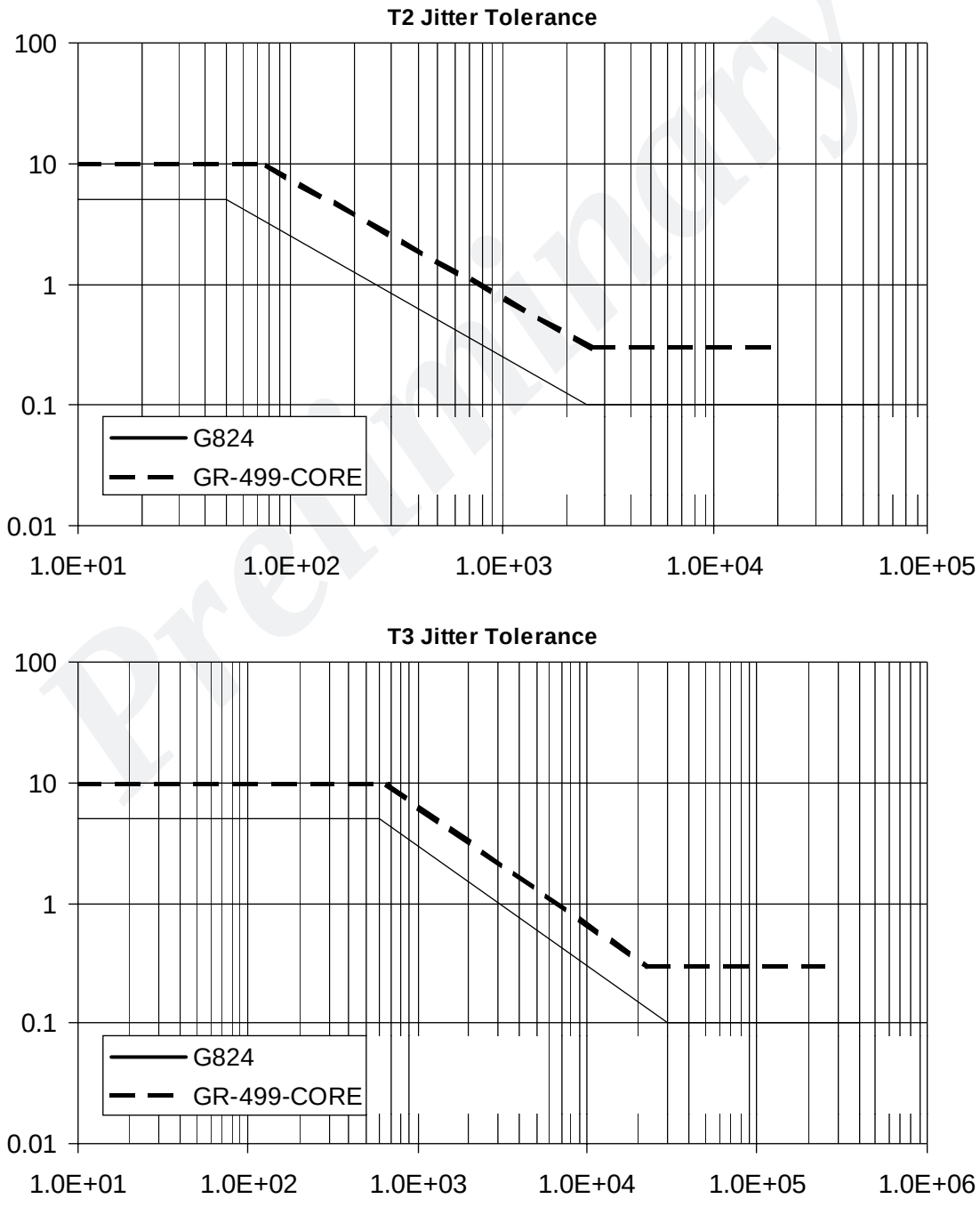


Figure 16: T2 and T3 Jitter specifications.

E1 Jitter specification

When configured for E1 operation, the Jitter Tolerance performances exceeds that specified in ITU-T G.823. The Jitter Transfer performance exceeds that specified in ITU-T G.736.

With reference to ITU-T G.736, section 6.1.3; in the case where the timing signal is derived from an incoming 2048kbit/s signal having no jitter, the output jitter should not exceed 0.10 UIpp when it is measured in the frequency range 20Hz to 100kHz.

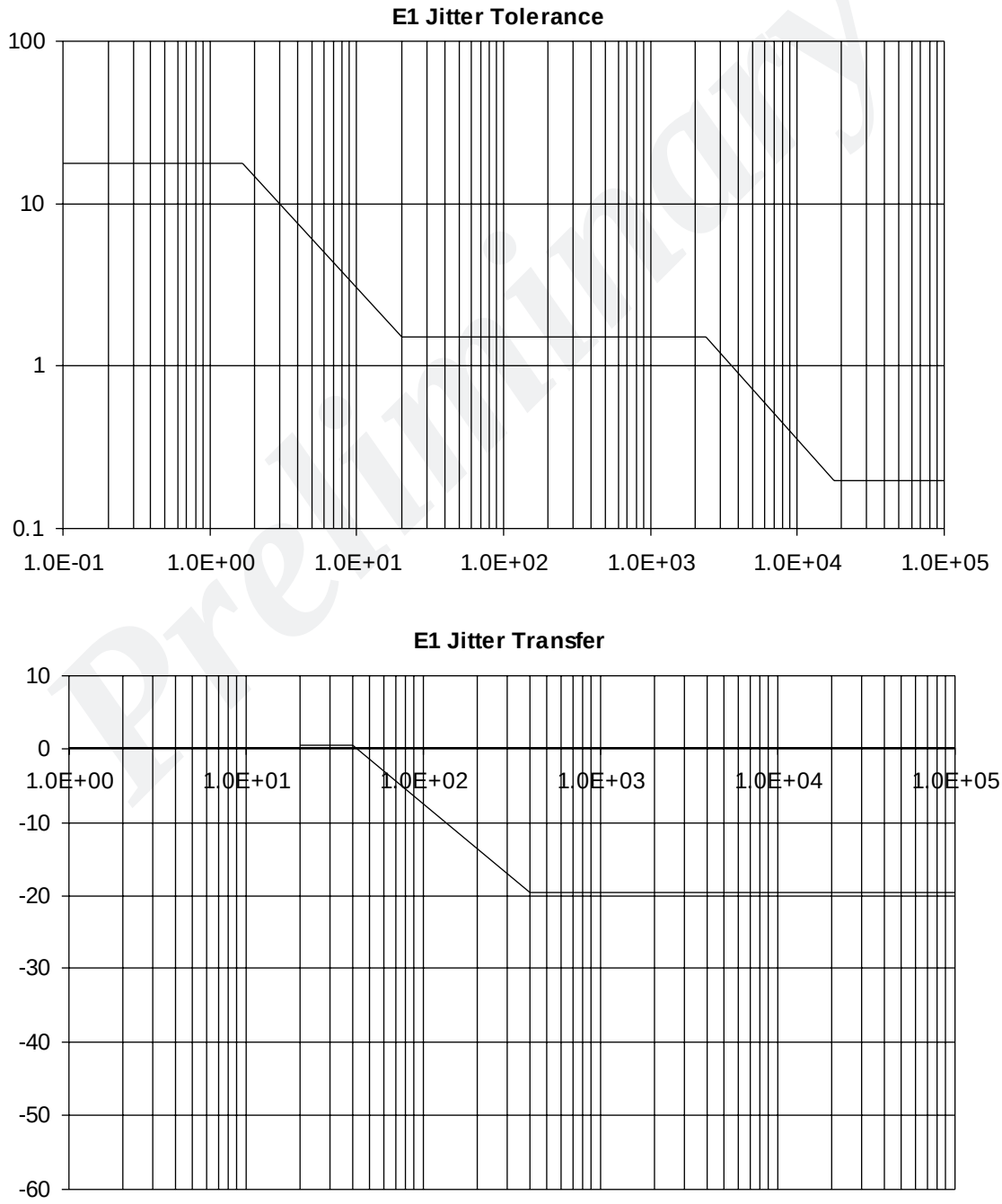


Figure 17: E1 Jitter specifications.

E2 Jitter specification

When configured for E2 operation, the Jitter Tolerance performance exceeds that specified in ITU-T G.823.

In the absence of input jitter, the output jitter generated from the Digital PLL for E2 operation is:

Frequency band	Output Jitter
20Hz to 400kHz	0.7UIpp
80kHz to 400kHz	0.09UIpp

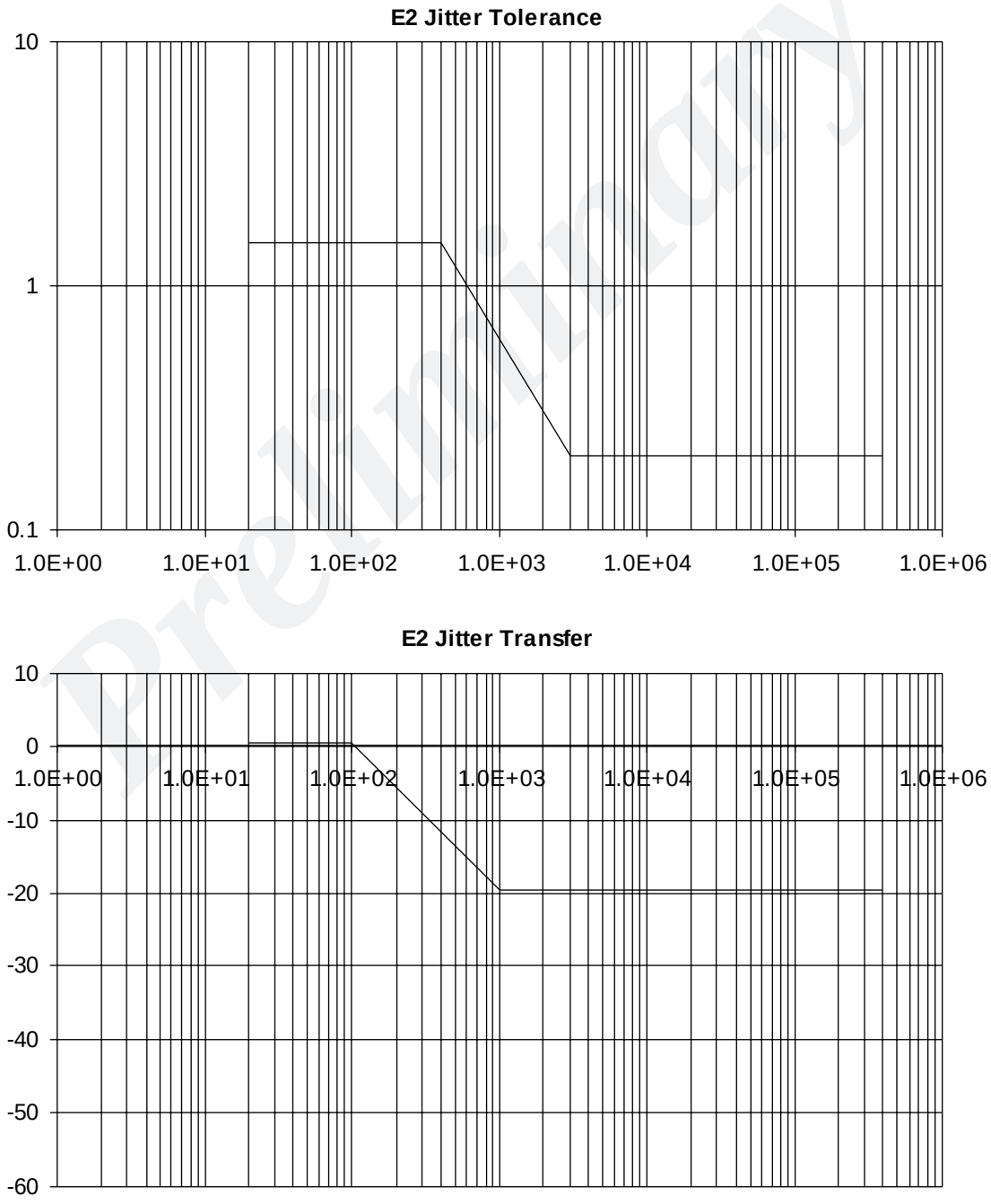


Figure 18: E2 Jitter specifications.

E3 Jitter specification

When configured for E3 operation, the Jitter Tolerance performance exceeds that specified in ITU-T G.823.

Output Jitter Generation after band pass filtering 10 kHz to 800kHz.

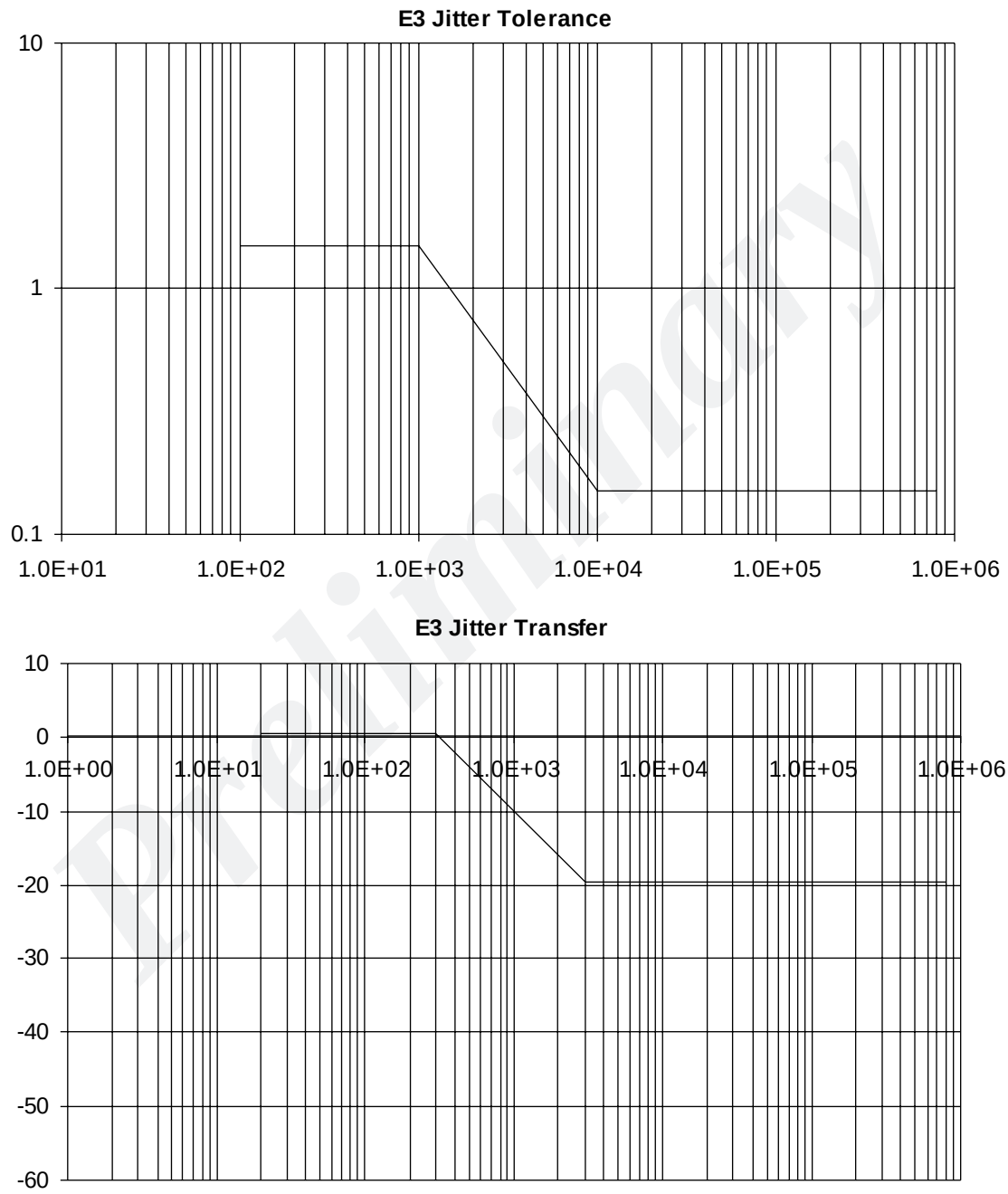


Figure 19: E3 Jitter specifications.

OC1/STS1 Jitter specification

When configured for OC1/STS1 operation, the Jitter Tolerance and Jitter Transfer performance exceeds the requirements specified in Bellcore GR-253-CORE.

In the absence of input jitter, the output jitter generated from the mixed signal PLL after band pass filtering from 12kHz to 400kHz is 0.07UIpp.

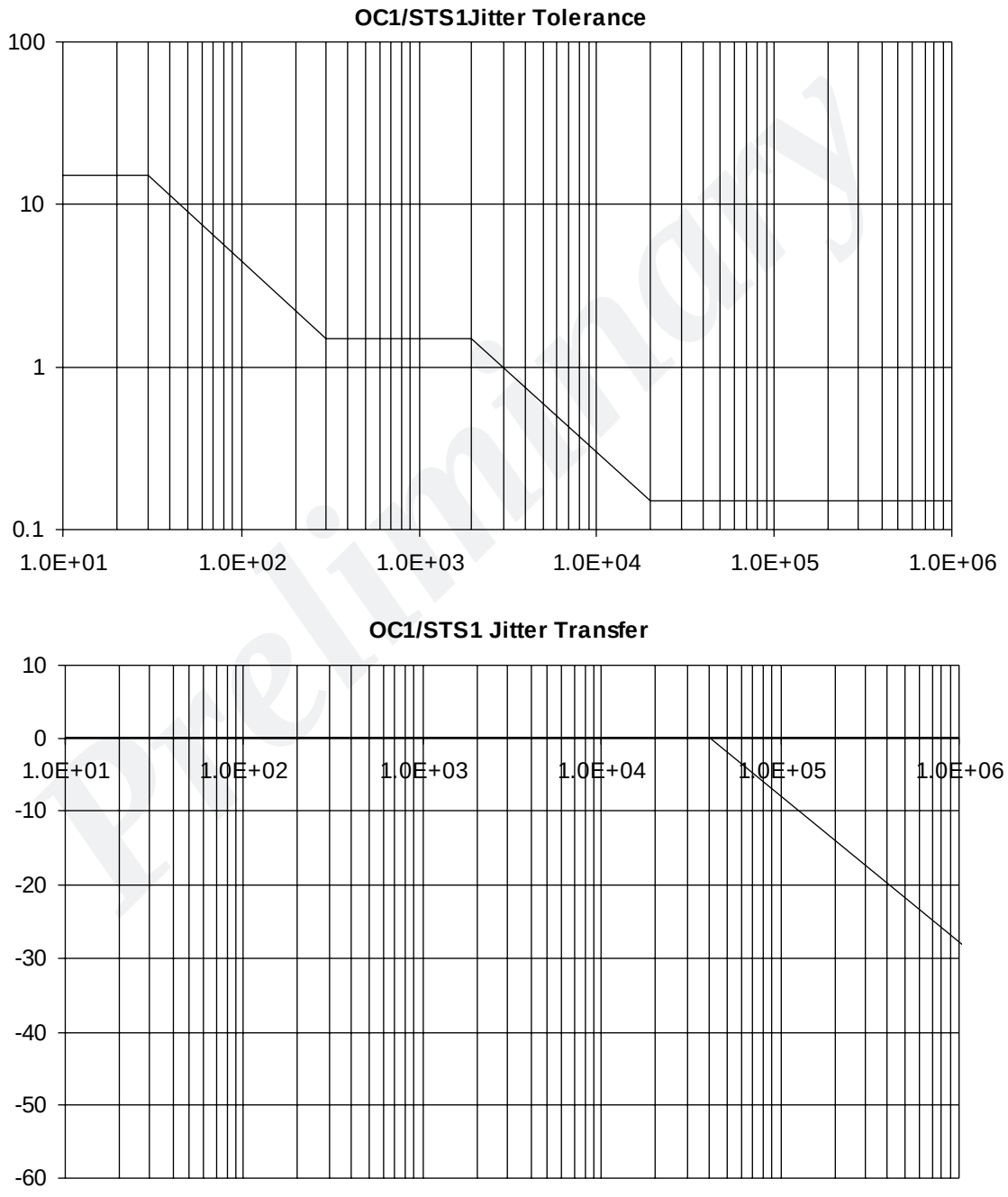
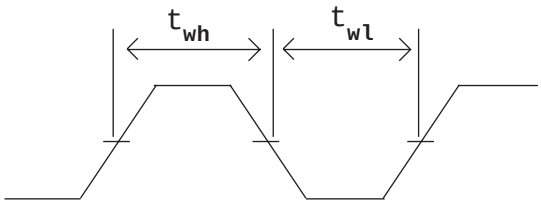
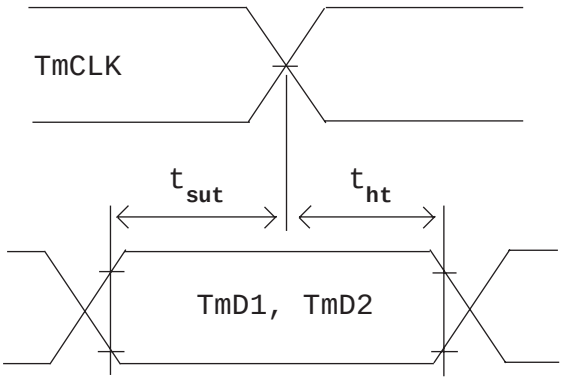


Figure 20: OC1/STS1 Jitter specifications.

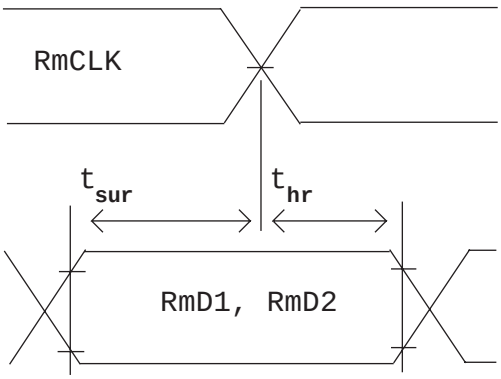


TmCLK and RmCLK clock pulse widths



Transmit set-up and hold times

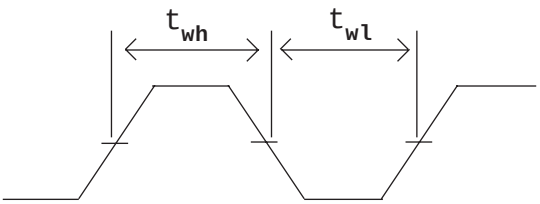
The active TmCLK edge is defined by input TRSEL.



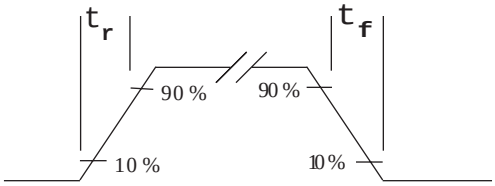
Receive set-up and hold times

The active RmCLK edge is defined by input RESEL.

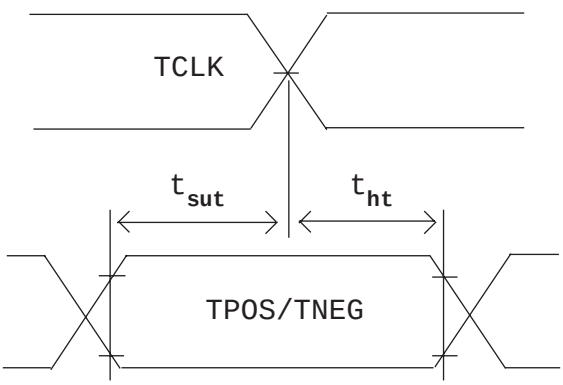
Figure 21: Timing diagrams



TCLK and RCLK clock pulse widths

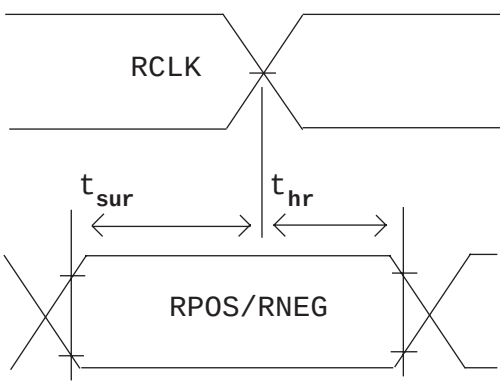


Digital outputs rise and fall times



Transmit set-up and hold times

The active TCLK edge is defined by input TRSEL.



Receive set-up and hold times

The active RCLK edge is defined by input RESEL.

Figure 22: Timing diagrams

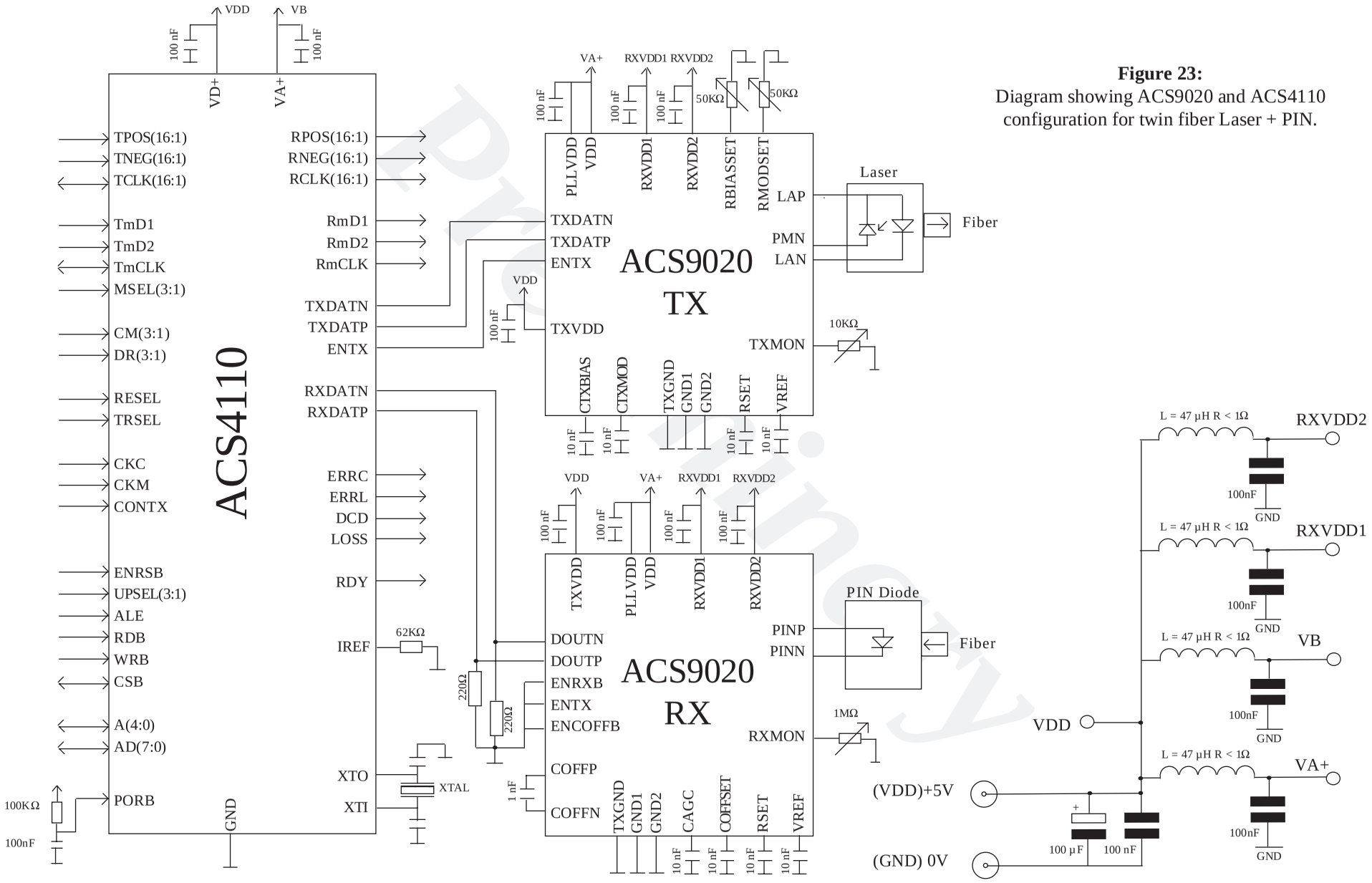
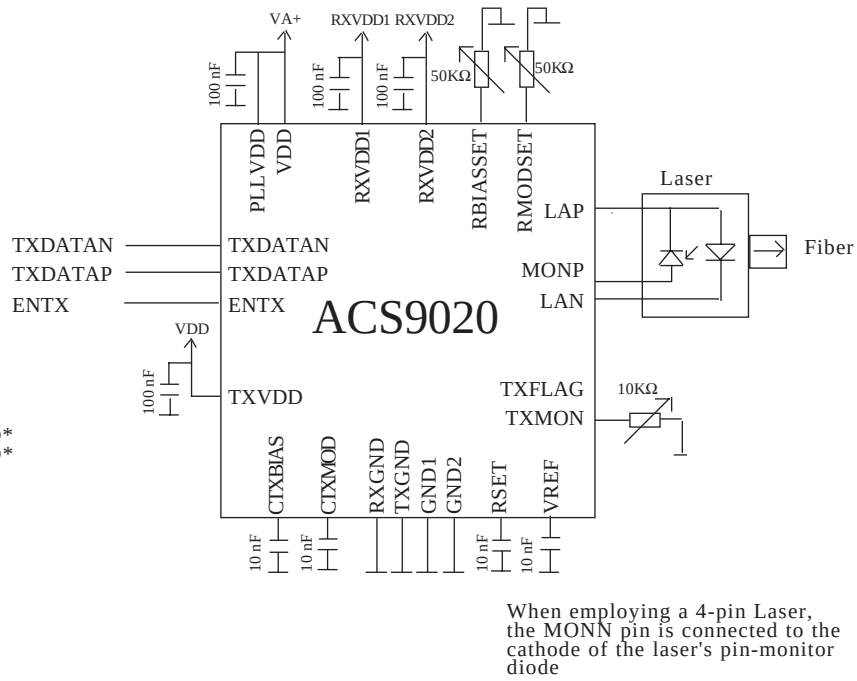


Figure 23:
Diagram showing ACS9020 and ACS4110 configuration for twin fiber Laser + PIN.

LEDRX	=	GND
PINRX	=	GND
XIN	=	GND
XOUT	=	float
F(2:0)	=	GND
RPLL	=	float
ENPLL	=	GND
DINP	=	GND
DINN	=	GND
DOUTP	=	float
DOUTN	=	float
IDOUT	=	GND
ICOFF	=	GND
CBTSTRP	=	GND
COFFWIN	=	float
ENCOFFB	=	GND
ENRXB	=	VDD
RXFLAG	=	float
RXMON	=	float
COFFP	=	float
COFFN	=	float
CAGC	=	float
COFFSET	=	float
VN	=	float
VP	=	float
PINN	=	float
PINP	=	float
MONN	=	float
BIASFIX	=	GND/VDD*
MODFIX	=	GND/VDD*
IBUF	=	GND
SDATAN	=	float
SDATAP	=	float
SCLKN	=	float
SCLKP	=	float
TXEN	=	float
TXSEL	=	GND
QUIETRX	=	GND
MONRX	=	GND

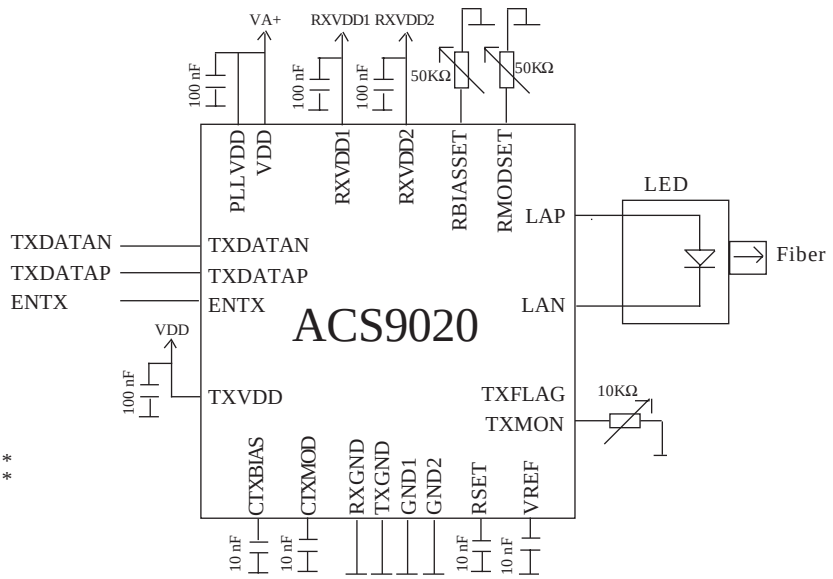


When employing a 4-pin Laser, the MONN pin is connected to the cathode of the laser's pin-monitor diode

* configure with a jumper to enable/disable automatic bias power and modulation power regulation.

Figure 24: Diagram showing ACS9020 configuration for use with a 3-pin laser.

LEDRX	=	GND
PINRX	=	GND
XIN	=	GND
XOUT	=	float
F(2:0)	=	GND
RPLL	=	float
ENPLL	=	GND
DINP	=	GND
DINN	=	GND
DOUTP	=	float
DOUTN	=	float
IDOUT	=	GND
ICOFF	=	GND
CBTSTRP	=	GND
COFFWIN	=	float
ENCOFFB	=	GND
ENRXB	=	VDD
RXFLAG	=	float
RXMON	=	float
COFFP	=	float
COFFN	=	float
CAGC	=	float
COFFSET	=	float
VN	=	float
VP	=	float
PINN	=	float
PINP	=	float
MONN	=	float
MONP	=	float
BIASFIX	=	GND/VDD*
MODFIX	=	GND/VDD*
IBUF	=	GND
SDATAN	=	float
SDATAP	=	float
SCLKN	=	float
SCLKP	=	float
TXEN	=	float
TXSEL	=	GND
QUIETRX	=	GND
MONRX	=	GND



* configure with a jumper to enable/disable automatic bias power and modulation power regulation.

Figure 25: Diagram showing ACS9020 configuration for LED transmission.

LEDRX	=	GND
PINRX	=	VDD
XIN	=	GND
XOUT	=	float
F(2:0)	=	GND
RPLL	=	float
ENPLL	=	GND
DINP	=	GND
DINN	=	GND
ICOFF	=	GND
CBTSTRP	=	GND
COFFWIN	=	float
VN	=	float
VP	=	float
BIASFIX	=	VDD
MODFIX	=	VDD
IBUF	=	GND
SDATAN	=	float
SDATAP	=	float
SCLKN	=	float
SCLKP	=	float
TXEN	=	float
TXSEL	=	GND
QUIETRX	=	VDD
MONRX	=	GND
PMN	=	float
MONN	=	float
LAP	=	float
LAN	=	float
CTXMOD	=	float
CTXBIAS	=	float
RMODSET	=	float
RBIASSET	=	float
TXP	=	GND
TXN	=	GND
TXFLAG	=	float
TXMON	=	float
IDOUT	=	GND

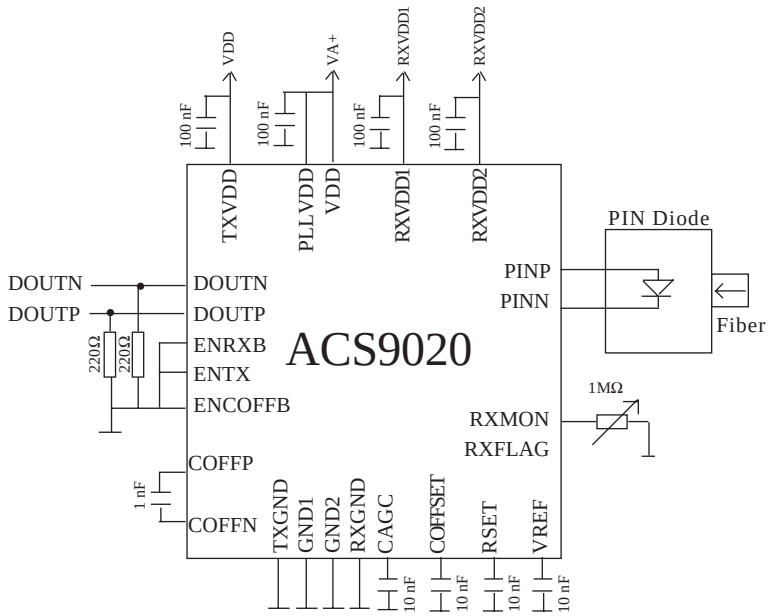


Figure 26: Diagram showing ACS9020 configuration as a trans-impdeance-amplifier/post-amplifier.

LEDRX	=	GND
PINRX	=	GND
XIN	=	GND
XOUT	=	float
F(2:0)	=	GND
RPLL	=	float
ENPLL	=	GND
DINP	=	GND
DINN	=	GND
ICOFF	=	GND
CBTSTRP	=	GND
COFFWIN	=	float
PINN	=	float
PINP	=	float
BIASFIX	=	VDD
MODFIX	=	VDD
IBUF	=	GND
SDATAN	=	float
SDATAP	=	float
SCLKN	=	float
SCLKP	=	float
TXEN	=	float
TXSEL	=	GND
QUIETRX	=	VDD
MONRX	=	GND
PMN	=	float
MONN	=	float
LAP	=	float
LAN	=	float
CTXMOD	=	float
CTXBIAS	=	float
RMODSET	=	float
RBIASSET	=	float
TXP	=	GND
TXN	=	GND
TXFLAG	=	float
TXMON	=	float
IDOUT	=	GND

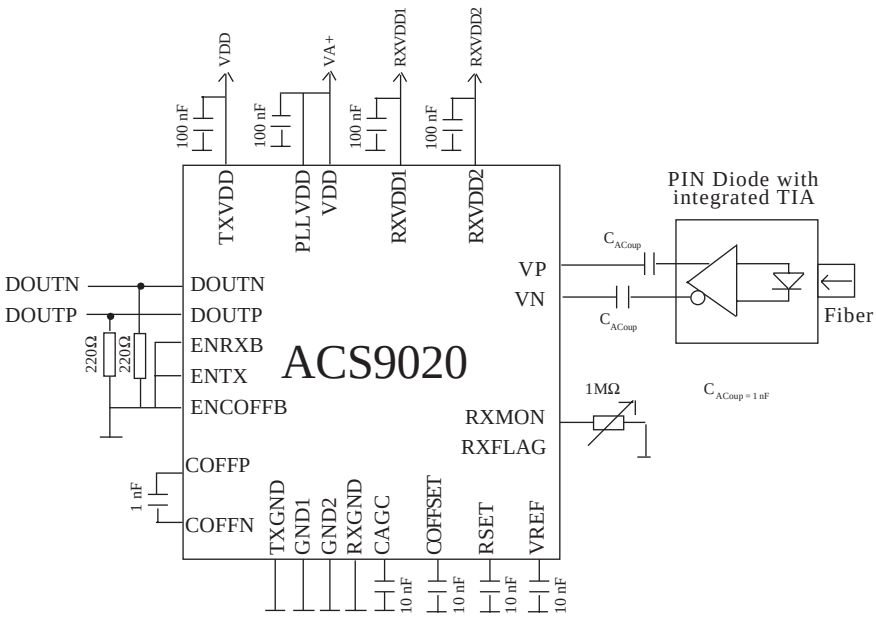
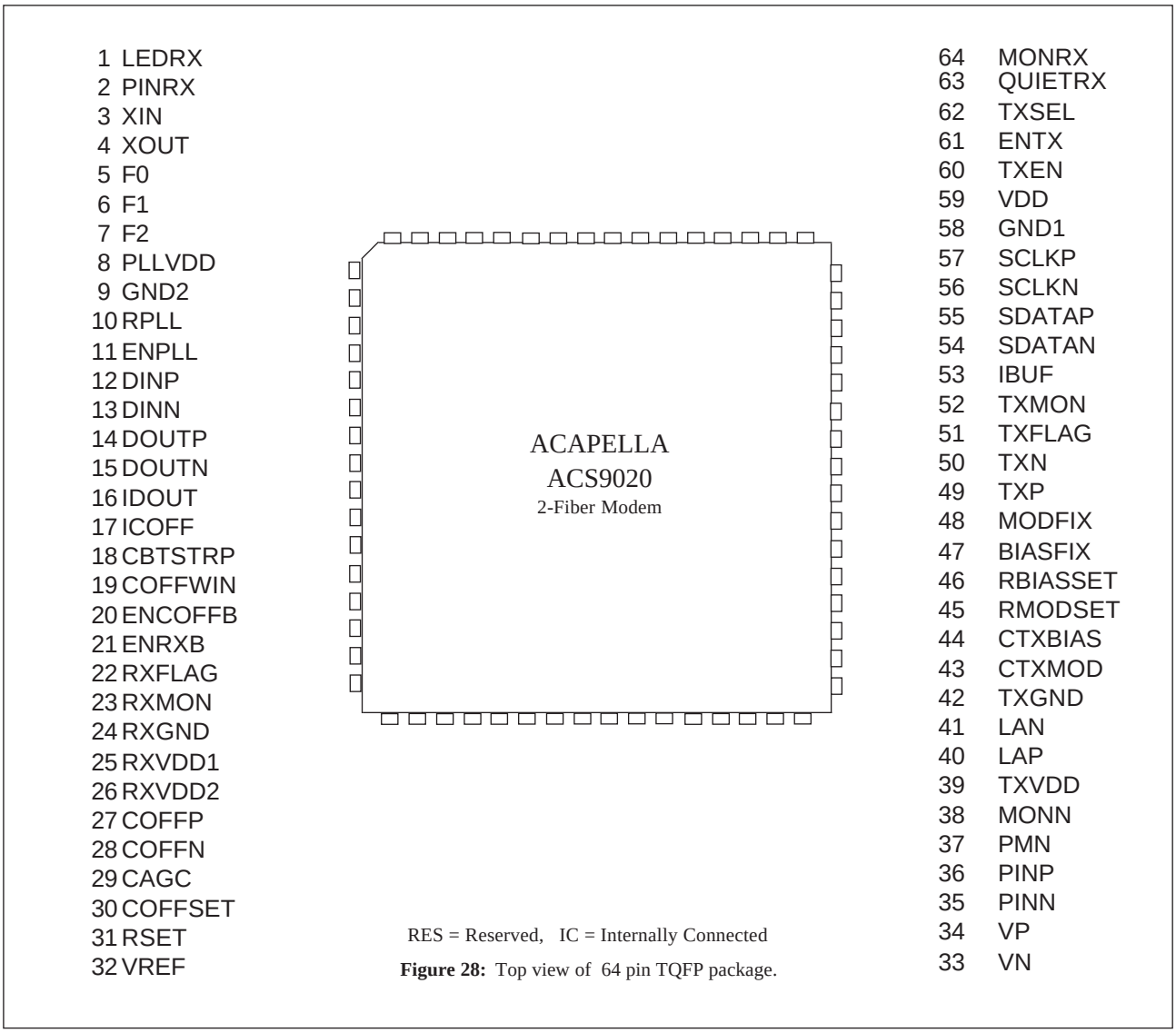


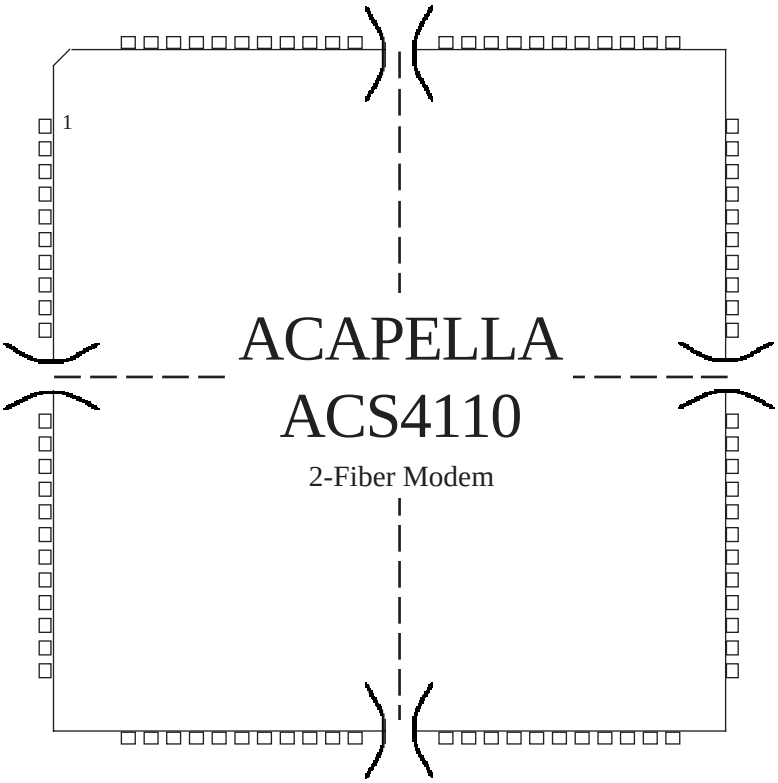
Figure 27: Diagram showing ACS9020 configuration as a post-amplifier.



RES = Reserved, IC = Internally Connected

Figure 28: Top view of 64 pin TQFP package.

1	TPOS7
2	TNEG7
3	RCLK6
4	RPOS6
5	GND
6	VD+
7	RNEG6
8	TCLK6
9	TPOS6
10	TNEG6
11	RCLK5
12	RPOS5
13	RNEG5
14	TCLK5
15	TPOS5
16	TNEG5
17	RCLK4
18	RPOS4
19	RNEG4
20	TCLK4
21	TPOS4
22	TNEG4
23	RCLK3
24	RPOS3
25	RNEG3
26	TCLK3
27	TPOS3
28	TNEG3
29	RCLK2
30	RPOS2
31	RNEG2
32	TCLK2
33	TPOS2
34	TNEG2
35	RCLK1
36	RNEG1
37	GND
38	VD+
39	RPOS1
40	TCLK1
41	TPOS1
42	TNEG1
43	RCLK10
44	RPOS10
45	RNEG10
46	TCLK10
47	TPOS10
48	TNEG10
49	RCLK11
50	RPOS11
51	GND
52	VD+
53	RNEG11
54	TCLK11
55	TPOS11
56	TNEG11
57	RCLK12
58	RPOS12
59	RNEG12
60	TCLK12
61	TPOS12
62	TNEG12
63	RCLK13
64	RPOS13
65	RNEG13
66	TCLK13
67	TPOS13
68	TNEG13
69	RCLK14
70	RPOS14
71	RNEG14
72	TCLK14
73	TPOS14
74	TNEG14
75	RCLK15
76	RPOS15
77	RNEG15
78	TCLK15
79	TPOS15
80	TNEG15
81	GND
82	VD+
83	TCLK16
84	GND
85	VD+
86	RCLK16
87	RPOS16
88	RNEG16



176	TCLK7
175	RNEG7
174	RPOS7
173	RCLK7
172	TNEG8
171	TPOS8
170	TCLK8
169	RNEG8
168	RPOS8
167	RCLK8
166	TNEG9
165	TPOS9
164	TCLK9
163	RNEG9
162	VD+
161	VD+
160	GND
159	GND
158	RPOS9
157	RCLK9
156	TmCLK
155	RmCLK
154	TPOS16
153	TNEG16
152	AD7
151	AD6
150	AD5
149	AD4
148	AD3
147	AD2
146	AD1
145	AD0
144	A4
143	A3
142	A2
141	A1
140	A0
139	VD+
138	GND
137	RDY
136	CSB
135	WRB
134	RDB
133	ALE
132	ENTX
131	DCD
130	GND
129	PORB
128	GND
127	UPSEL1
126	UPSEL2
125	UPSEL3
124	GND
123	GND
122	GND
121	XTO
120	XTI
119	DR1
118	DR2
117	DR3
116	RESEL
115	VA+
114	IREF
113	CM1
112	CM2
111	CM3
110	RXDATN
109	RXDATP
108	GND
107	TXDATN
106	TXDATP
105	VD+
104	TRSEL
103	CKC
102	CKM
101	MSEL1
100	MSEL2
99	MSEL3
98	ENRSB
97	CONTX
96	TmD2
95	TmD1
94	VD+
93	RmD2
92	RmD1
91	LOSS
90	ERRL
89	ERRC

RES = Reserved, IC = Internally Connected

Figure 29: Top view of 176 pin TQFP package.

Pin Description ACS4110 part 1.

Pin	Sym	IO	Name	Description
6,38, 52,82, 85,94, 105,139, 161,162	VD+	-	+ve power supply	Power supply, 4.75 - 5.25 Volts.
115	VA+	-	+ve power supply	Power supply for Clock Recovery PLL, 4.75 - 5.25 Volts.
5, 37, 51,81, 84,108, 122,123, 124,128, 130,138, 159,160	GND	-	Ground	Power Supply
41 TPOS1 33 TPOS2 27 TPOS3 21 TPOS4 15 TPOS5 9 TPOS6 1 TPOS7 171 TPOS8 165 TPOS9 47 TPOS10 55 TPOS11 61 TPOS12 67 TPOS13 73 TPOS14 79 TPOS15 154 TPOS16		I	Transmit Data Positive	Transmit channel 1-16, corresponds to +ve in bipolar signal.
42 TNEG1 34 TNEG2 28 TNEG3 22 TNEG4 16 TNEG5 10 TNEG6 2 TNEG7 172 TNEG8 166 TNEG9 48 TNEG10 56 TNEG11 62 TNEG12 68 TNEG13 74 TNEG14 80 TNEG15 153 TNEG16		I	Transmit Data Negative	Transmit channel 1-16, corresponds to -ve in bipolar signal.
39 RPOS1 30 RPOS2 24 RPOS3 18 RPOS4 12 RPOS5 4 RPOS6 174 RPOS7 168 RPOS8 158 RPOS9 44 RPOS10 50 RPOS11 58 RPOS12 64 RPOS13 70 RPOS14 76 RPOS15 87 RPOS16		O	Receive Data Positive	Receive channel 1-16, corresponds to +ve in bipolar signal.

Pin Description ACS4110 part 2.

Pin	Sym	IO	Name	Description
36 RNEG1 31 RNEG2 25 RNEG3 19 RNEG4 13 RNEG5 7 RNEG6 175 RNEG7 169 RNEG8 163 RNEG9 45 RNEG10 53 RNEG11 59 RNEG12 65 RNEG13 71 RNEG14 77 RNEG15 88 RNEG16		O	Receive Data Negative	Receive channel 1-16, corresponds to -ve in bipolar signal.
131	DCD	O	Data Carrier Detect	When DCD=1, then the communicating modems have synchronised, and are communicating.
120 XTI/ 121 XTO		-	System Clock Crystal	Connect fundamental parallel resonance crystal with appropriate padding capacitor to GND.
129	PORB	I	Power On Reset	Will initialise the device when PORB= 0. PORB is normally connected to an RC circuit so that a POR is automatically invoked on power-up. PORB= 1 for normal operation.
156	TmCLK	I/O	Transmit maintenance CLK	Transmit maintenance Clock. samples TmD on edge selected by TRSEL control.
155	RmCLK	O	Receive maintenance Clock	Receive maintenance Clock. samples RmD on edge selected by RESEL control..
116	RESEL	I	Receive Edge Select	When RESEL = 1, RPOS/RNEG and RmD data is valid on the rising edge of RCLK/RmCLK. When RESEL = 0, the data is valid on the falling edge of RCLK/RmCLK.
104	TRSEL	I	Transmit Edge Select	When TRSEL = 0, TPOS/TNEG and TmD data is latched on the falling edge of TCLK/TmCLK. When TRSEL =1, the data is latched on the rising edge of TCLK/TmCLK.
95	TmD1	I	Transmit maintenance Data	NRZ maintenance channel. TmD is sampled on the TmCLK clock edge defined by TRSEL.
92	RmD2	O	Receive maintenance Data	NRZ maintenance channel. RmD is sampled on the RmCLK clock edge defined by RESEL.

Pin Description ACS4110 part 3.

Pin	Sym	IO	Name	Description
40 32 26 20 14 8 176 170 164 46 54 60 66 72 78 83	TCLK1 TCLK2 TCLK3 TCLK4 TCLK5 TCLK6 TCLK7 TCLK8 TCLK9 TCLK10 TCLK11 TCLK12 TCLK13 TCLK14 TCLK15 TCLK16	I/O	Transmit clocks	Transmit Clock 1-16, samples TPOS/TNEG data on clock edge selected by input TRSEL.
35 29 23 17 11 3 173 167 157 43 49 57 63 69 75 86	RCLK1 RCLK2 RCLK3 RCLK4 RCLK5 RCLK6 RCLK7 RCLK8 RCLK9 RCLK10 RCLK11 RCLK12 RCLK13 RCLK14 RCLK15 RCLK16	O	Receive clocks	Receive Clock, RPOS/RNEG data is valid on edge selected by input RESEL.
113 112 111	CM1 CM2 CM3	I	Configuration Modes	CM(3:1) select the Configuration Modes such as full duplex, master and slave mode.
90	ERRL	O	Error Latch	If errors are detected in the 8B10B coding rules ERRL will be forced high.. ERRL will be reset low if the device is forced out of synchronisation e.g. PORB = 0.
89	ERRC	O	Error count	ERRC will go high coincident with each error detected in the 8B10B coding rules. Errors may be accumulated by means of an external electronic counter.
119 118 117	DR1 DR2 DR3	I	Data Rate Select	The DR(3:1) input select the Data Rates and number of channels. See section headed *Data Rate Selection.*
103	CKC	I	Clock Select	When CKC = 0, TCLK1-16 are configured as an output. When CKC = 1, TCLK1-16 are configured as an input.
102	CKM	I	Clock Select	When CKM = 0, TmCLK is configured as an output. When CKM = 1, TmCLK is configured as an input
97	CONTX	I	Continuous transmit	
114	IREF	I	Current reference	A 51KΩ 1% resistor should be placed between IREF and GND.

Pin Description ACS4110 part 4.

Pin	Sym	IO	Name	Description
91	LOSS	O	LOSS of Signal	When LOSS = 1, receive data is unreliable. When LOSS = 0, receive data is reliable.
96	TmD1	I	Transmit maintenance Data	NRZ maintenance channel. TmD is sampled on the TmCLK clock edge defined by TRSEL.
93	RmD2	O	Receive maintenance Data	NRZ maintenance channel. RmD is sampled on the RmCLK clock edge defined by RESEL.
101 100 99	MSEL1 MSEL2 MSEL3	I	Maintenance channel data rate selection	The MSEL(3:1) input select the Data Rates of channels. See section headed *Maintenance Data Rate Selection.*
98	ENRSB	I	Enable Remote Setup	Remote device setup.

Pin description ACS4110 part 5 - uP interface.

Pin	Sym	IO	Name	Description
127 126 125	UPSEL1 UPSEL2 UPSEL3	I	uP Interface	uP interface mode control.
133	ALE	I	uP Interface	uP bus address latch enable. 1) POL3 in pin control mode UPSEL(3:1) = 0.
134	RDB	I	uP Interface	uP bus read (active low). 2) POL2 in pin control mode UPSEL(3:1) = 0.
135	WRB	I	uP Interface	uP bus write (active low). 3) POL1 in pin control mode UPSEL(3:1) = 0.
136	CSB	IO	uP Interface	uP bus chip select (active low). 4) CKLOCAL in pin control modeUPSEL(3:1) = 0.
137	RDY	O	uP Interface	uP bus ready/data acknowledge.
140 141 142 143 144	A0 A1 A2 A3 A4	IO	uP Interface	uP bus address.
145 146 147 148 149 150 151 152	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	IO	uP Interface	uP bus address/data.

Pin Description of interface signals between ACS9020 and ACS4110.

Pin	Sym	IO	Name	Description
132 61	ENTX	O I	Enable Transmit	Transmit active (ACS4110). Enable transmit (ACS9020).
110	RXDATN	I	Receive data	Negative differential receive data in (or slicing level in for RXDATP).
109	RXDATP	I	Receive data	Positive receive data in.
107	TXDATN	O	Transmit data	Negative differential transmit data in (or slicing level in for TXDATP).
106	TXDATP	O	Transmit data	Positive transmit data out.

Pin Description ACS9020 part 1.

Pin	Sym	IO	Name	Description
1	LEDRX	I	LED receive	Set Logic High or Low.
2	PINRX	I	PINP/PINN Receive	Set Logic High or Low.
3 4	XIN XOUT	-	System Clock Crystal	External crystal with 20pF padding capacitor.
5 6 7	F0 F1 F2	I	Frequency set	PLL rate select.
8	PLLVDD	-	VDD for VCO	Power supply, 4.75 - 5.25 Volts.
9	GND2	-	GND	Power supply.
10	RPLL	-	PLL reference resistor	62KΩ to GND
11	ENPLL	I	PLL Enable	Set Logic High or Low.
12	DINP	I	PLL Positive input data	Connect to DOUTN.
13	DINN	I	PLL Negative input data	Connect to DOUTP.
14	DOUTP	O	Receiver Positive output data	Connect to DINN (220Ω to GND if IDOUT floating).
15	DOUTN	O	Receiver Negative output data	Connect to DINP (220Ω to GND if IDOUT floating).
16	IDOUT	-	Reference current for Data output	1KΩ to VDD (or float if using external differential o/p loads).
17	ICOFF	-	Bias current for automatic offset compensation windowing	100KΩ to RXVDD1 to give COFFWIN delay of 60ns.
18	CBTSTRP	-	Auto offset compensation bootstrap capacitor	10nF to GND to give 2ms bootstrap delay (ICOFF = 100KΩ).
19	COFFWIN	O	Auto output generated window output	Connect to ENCOFFB for auto windowing.
20	ENCOFFB	I	Receiver offset compensation enable	Connect o COFFWIN for auto windowing.
21	ENRXB	I	Receiver enable	Set to Logic High or Low.
22	RXFLAG	O	Receiver signal monitor flag	Use to drive external monitor LED.
23	RXMON	-	Receiver signal monitor	1MΩ potentiometer to GND to adjust RXFLAG threshold.
24	RXGND	-	Ground	Power supply.
25	RXVDD1	-	Receive power supply	Power supply, 4.75 - 5.25 Volts.

Pin Description ACS9020 part 2.

Pin	Sym	IO	Name	Description
26	RXVDD2	-	Pre-amp power supply	Power supply, 4.75 - 5.25 Volts.
27	COFFP	-	Post amp offset capacitor	1nF to COFFN.
28	COFFN	-	Post amp offset capacitor	1nF to COFFP.
29	CAGC	-	Preamp AGC capacitor	10nF to GND.
30	COFFSET	-	Preamp offset capacitor	10nF to GND.
31	RSET	-	Receiver current bias resistor	10nF to GND.
32	VREF	-	Bandgap reference	10nF to GND.
33	VN	-	Postamp negative input	Negative output from external TIA.
34	VP	-	Postamp positive input	Positive output from external TIA.
35	PINN	-	Receiver PIN cathode	Laser/LED PIN cathode.
36	PINP	-	Receiver PIN anode	Laser/LED PIN anode.
37	PMN	-	Monitor PIN anode	Laser monitor PIN anode.
38	MONN	-	Monitor PIN cathode	Laser monitor PIN cathode.
39	TXVDD	-	Power Supply	Power supply, 4.75 - 5.25 Volts.
40 41	LAP LAN	-	Anode Cathode	Laser/LED anode. Laser/LED cathode.
42	TXGND	-	Ground	Power supply.
43	CTXMOD	-	Laser/LED modulation	Laser/LED modulation current set smoothing capacitor 10nF to GND.
44	CTXBIAS	-	Laser/LED bias	Laser/LED bias current set smoothing capacitor 10nF to GND.
45	RMODSET	-	Laser/LED modulation	Laser/LED modulation current set resistor 50KΩ potentiometer to GND.
46	RBIASSET	-	Laser/LED bias	Laser/LED bias current set resistor 50KΩ potentiometer to GND.
47	BIASFIX	I	Laser/LED bias fix	Set Logic High or Low.
48	MODFIX	I	Laser/LED modulation current fix	Set Logic High or Low.

Pin Description ACS9020 part 3.

Pin	Sym	IO	Name	Description
49	TXP	I	Data transmit positive	Positive output of TX data source.
50	TXN	I	Data transmit negative	Negative output of TX data source.
51	TXFLAG	O	Transmit current monitor flag	Used to drive external indicator LED.
52	TXMON	-	Transmit monitor current	10KΩ potentiometer to GND to adjust TXFLAG threshold.
53	IBUF	-	Current reference for SDATA and SCLK drivers	470Ω resistor to VDD (or float if using external differential o/p loads.
54	SDATAN	O	Re-synchronis-ed negative data	Re-synchronised negative data output (120Ω to GND if IBUF floating).
55	SDATAP	O	Re-synchronis-ed positive data	Re-synchronised positive data output (120Ω to GND if IBUF floating).
56	SCLKN	O	PLL recovered clock negative	PLL recovered clock negative (120Ω to GND if IBUF floating).
57	SCLKP	O	PLL recovered clock positive	PLL recovered clock positive (120Ω to GND if IBUF floating).
58	GND1	-	Ground	Power supply.
59	VDD	-	Power supply	Power supply, 4.75 - 5.25 Volts.
60	TXEN	O	Logic transmit window enable	Connect to ENTX if using internal packet data generator.
61	ENTX	I	Enable transmit	Set Logic High or Low or to TXEN.
62	TXSEL	I	Select packet transmit	Set Logic High or Low.
63	QUIETRX	I	Quiet reception	Set Logic High or Low.
64	MONRX	I	Monitor PIN receive select	Set Logic High or Low.

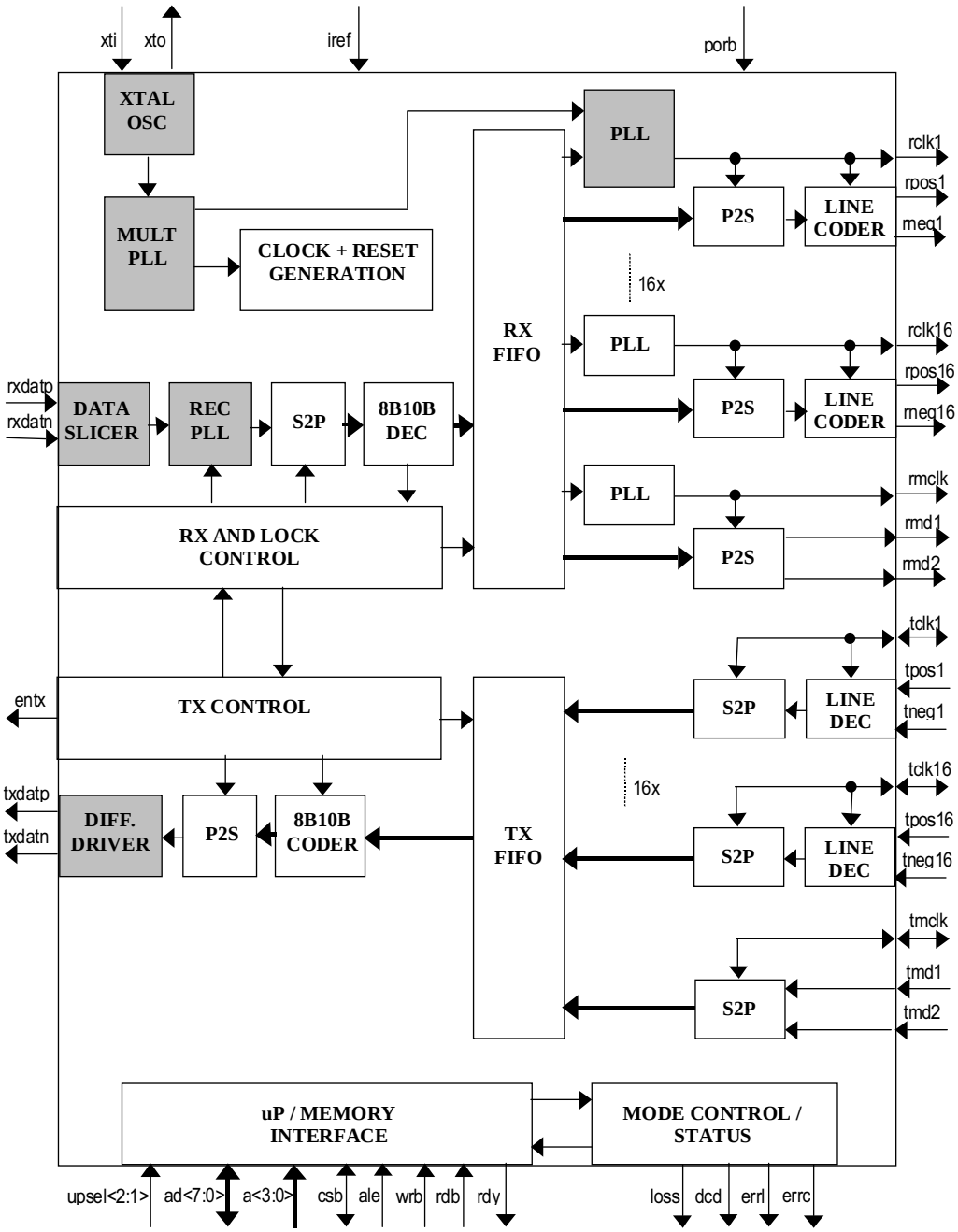
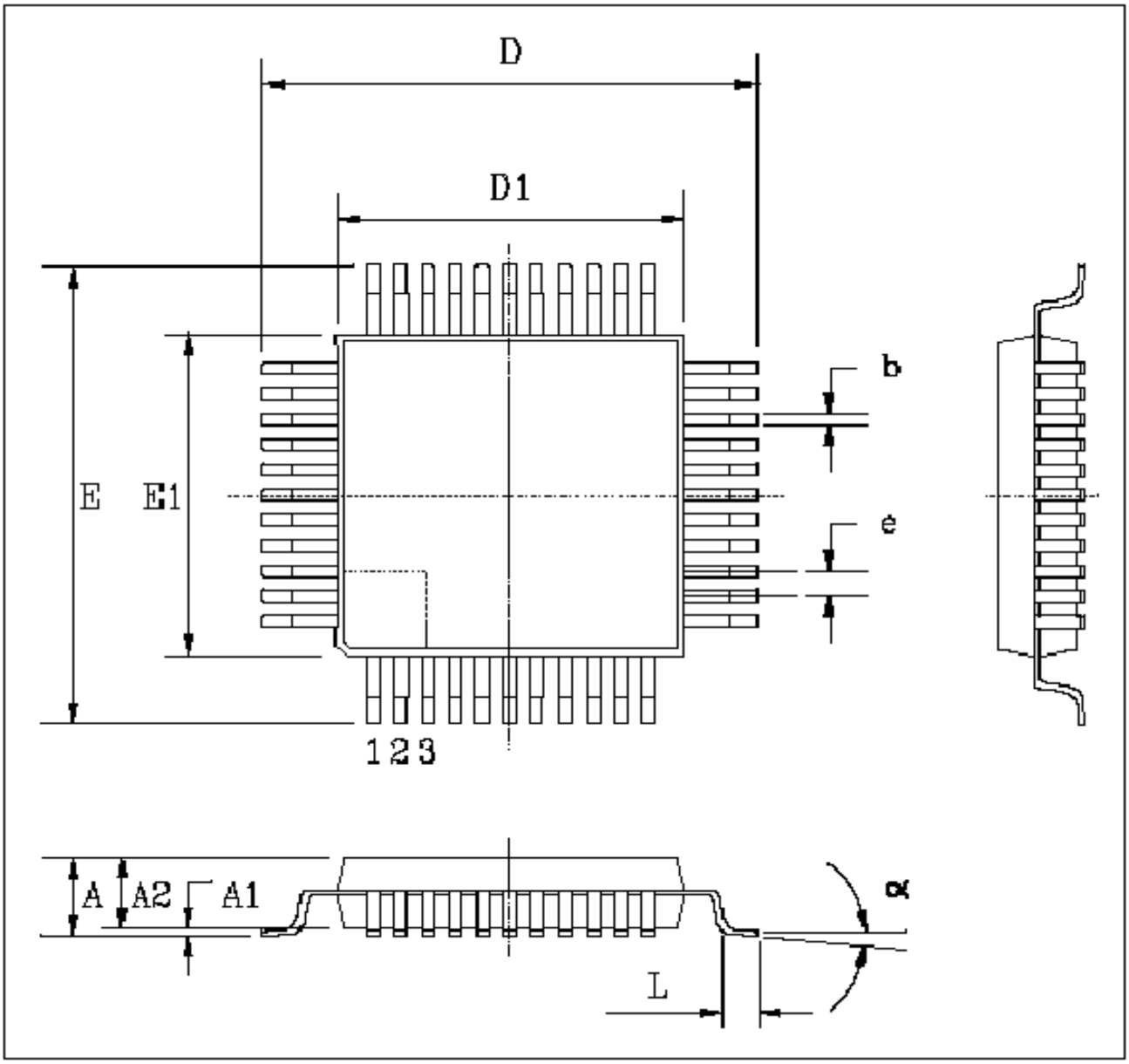
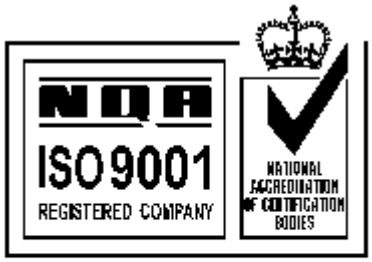


Figure 30: Block diagram for ACS4110.



Thin Quad Flat Pack dimensions in mm	E1/D1	A	A1	A2	e	b	L	α	E/D	Copl.
min			0.05	1.35		0.30	0.45	0°		
TQFP64	14.00				0.80				16.00	
max		1.60	0.15	1.45		0.45	0.75	7°		0.10
min			0.05	1.35		0.17	0.45	0°		
TQFP176	24.00				0.50				26.00	
max		1.60	0.15	1.45		0.27	0.75	7°		0.10

Figure 31: Package information for the 64 and 176 pin TQFP packages.



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