Analog Technology, Inc.

AD16312

1/4- To 1/11-Duty VFD Controller/Driver

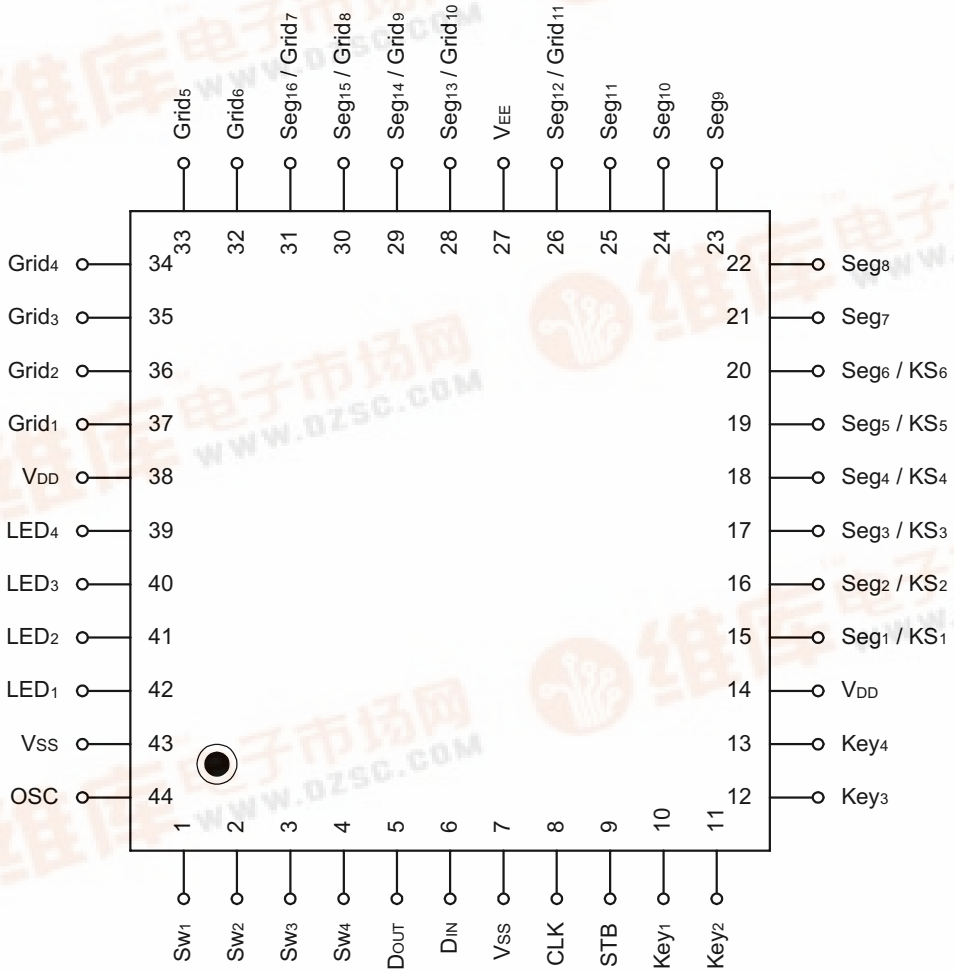
■ Features

- 4-pin serial interface
- Key scanning (6× 4 matrices)
- Programming display modes (11-digit & 11-segment to 16-digit & 4-segment)
- Programming Dimming step
- High-voltage output (V_{DD}-35V max).
- LED ports (4 channels., 20 mA max).
- 4-pin General-purpose input port
- Built in oscillator
- No external resistor necessary for driver outputs

■ General Description

The AD16312 is a VFD (Vacuum Fluorescent Display) controller/driver that is driven on a 1/5- to 1/12 duty factor(include key scan). It consists of 5 segment output lines, 6 segment/key scan output lines, 6 grid output lines, 5 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the AD16312 through a four-line serial interface.

■ Pin Assignment (Top View)



Use all power pins.

■ Pin Descriptions

Data input (D_{IN}) (Pin #6)
Input serial data at rising edge of shift clock, starting from the LSB.

Data output (D_{OUT}) Pin #5
Output serial data at falling edge of shift clock, starting from the LSB. This is an N-ch open-drain output pin.

Strobe (STB) (Pin #9)
Initializes serial interface at the rising or falling edge of the AD16312. It then waits for reception of a command. Data input after STB has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.

Clock input (CLK) (Pin #8)
Reads serial data at the rising edge, and outputs data at the falling edge.

Oscillator pin (OSC) (Pin #44)
Connect resistor to this pin to determine the oscillation frequency to this pin.

High-voltage output (Seg_1/KS_1 to Seg_6/KS_6) (Pin #15 to 20)
Multi-function pins. Segment output pins (Dual function as key scan source)

High-voltage output(Segment) (Seg_7 to Seg_{11}) (Pin #21 to 25)
Segment output pins

High-voltage output(grid) ($Grid_1$ to $Grid_6$) (Pin #37 to 32)
Grid output pins

High-voltage output(segment/grid) ($Seg_{12}/Grid_{11}$ to $Seg_{16}/Grid_7$) (Pin #26,28 to 31)
These pins are selectable for segment or grid driving.

LED output (LED_1 to LED_4) (Pin #42 to 39)
CMOS output.

Key data input (Key_1 to Key_4) (Pin #10 to 13)
Data input to these pins is latched at the end of the display cycle.

Switch input (SW_1 to SW_4) (Pin #1 to 4)
These pins constitute a 4-bit general-purpose input port.

Logic power (V_{DD}) (Pin #14,38)
5V±10%

Logic ground (V_{SS}) (Pin #7,43)
Connect this pin to system GND.

Pull-down level (V_{EE}) (Pin#27)

■ Absolute Maximum Ratings (T_a=25°C,V_{SS}=0V)

PARAMETER	SYMBOL	RATINGS	UNIT
Logic Supply Voltage	V_{DD}	-0.5 to +7.0	V
Driver Supply Voltage	V_{EE}	V_{DD} +0.5 to V_{DD} -40	V
Logic Input Voltage	V_{I1}	-0.5 to V_{DD} +0.5	V
VFD Driver Output Voltage	V_{O2}	V_{EE}-0.5 to V_{DD} +0.5	V
LED Driver Output Current	I_{O1}	+25	mA
VFD Driver Output Current	I_{O2}	-40(grid) -15(segment)	mA
Operating Ambient Temperature	T_{opt}	0 to +85	°C
Storage Temperature	T_{stg}	-20 to +125	°C

■ Operating Conditions (T_a=0 TO +70 °C,V_{SS}=0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V	
High-Level Input Voltage	V_{IH}	0.7·V_{DD}		V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0		0.3·V_{DD}	V	
Driver Supply Voltage	V_{EE}	0		V_{DD}-35	V	

■ DC Characteristics (T_a=0 to 70 °C, V_{DD}=4.5 to 5.5V, V_{SS}=0V, V_{EE}=V_{DD}-35V)

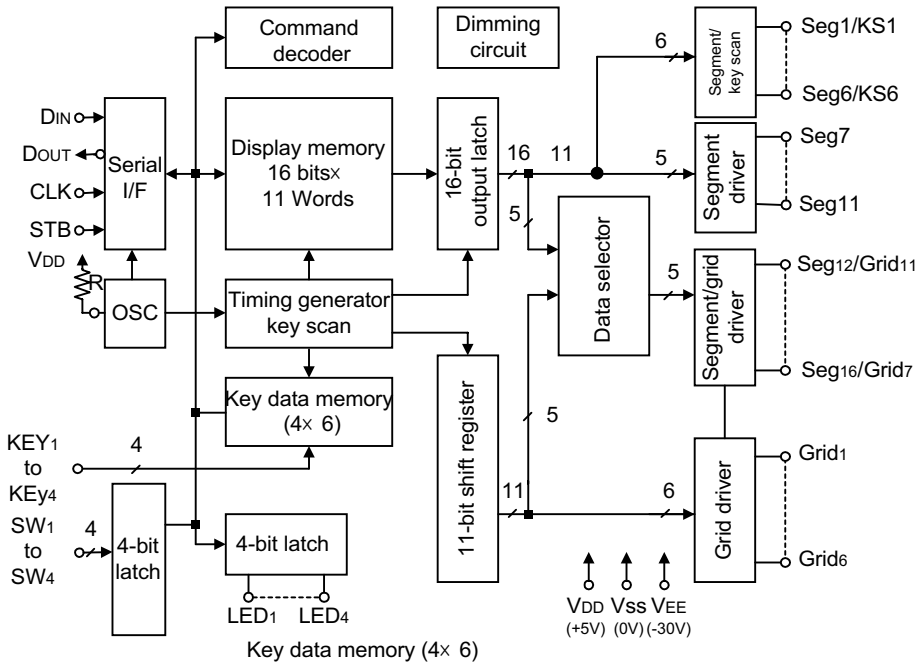
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-Level Output Voltage	V_{OH1}	0.9V_{DD}			V	LED_1-LED_4,I_{OH1}=-1mA
Low-Level Output Voltage	V_{OL1}			1	V	LED_1-LED_4,I_{OL1}=20mA
Low-Level Output Voltage	V_{OL2}			0.4	V	D_{OUT},I_{OL2}=4mA
High-Level Output Current	I_{OH21}	-3			mA	V_O=V_{DD}-2V,Seg_1 to Seg_{11}
High-Level Output Current	I_{OH22}	-15			mA	V_O=V_{DD}-2V,$Grid_1$ to $Grid_6$ Seg_{12}/$Grid_{11}$ to Seg_{16}/$Grid_7$
Driver Leakage Current	I_{OLEAK}			-10	μA	V_O=V_{DD}-35V, driver off
Output Pull-Down Resistor	R_L	50	100	150	kΩ	Driver output
High-Level Input Voltage	V_{IH}	0.7V_{DD}			V	
Low-Level Input Voltage	V_{IL}			0.3V_{DD}	V	

■ AC Characteristics (T_a=0 to +70 °C,V_{DD}=4.5 to 5.5 V, V_{EE}=-30V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Oscillation Frequency	f_{OSC}	350	500	650	KH_Z	R=51 kΩ
Maximum Clock Frequency	$f_{max.}$			1	MH_Z	Duty=50%
Clock Pulse Width	PW_{CLK}	500			ns	
Strobe Pulse Width	PW_{STB}	1			μs	
Data Setup Time	t_{SETUP}	100			ns	
Data Hold Time	t_{HOLD}	100			ns	
Clock-Strobe Time	$t_{CLK-STB}$	1			μs	CLK ↑ →STB ↑
Wait Time	t_{WAIT}	1			μs	CLK ↑ →CLK ↓ *(2)

*(2):Refer to page 8.

■ Block Diagram



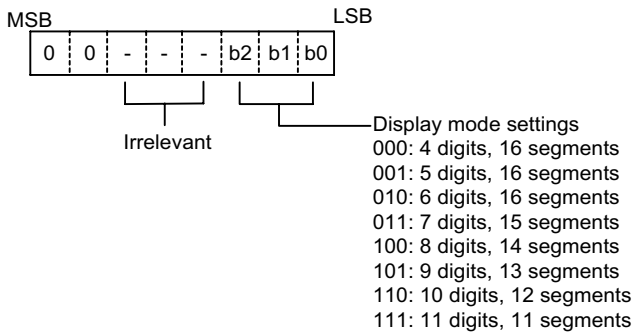
■ Function Description

1.0 Commands

Commands set the display mode and status of the VFD driver.
The first 1 byte input to the AD16312 through the D_{IN} pin after the STB pin has fallen is regarded as a command.
If STB is set high while a commands/data are transmitted, serial communication is Initialized , and the commands/data being transmitted are invalid (however, the commands/data previously transmitted remain valid).

1.1 Display mode setting commands

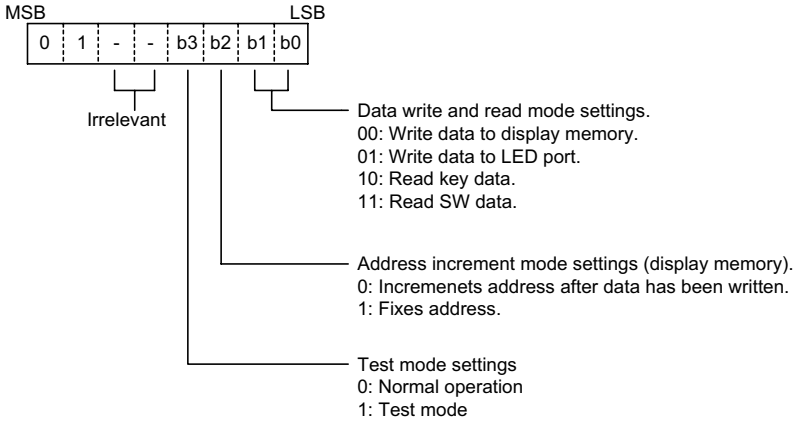
These commands initialize the AD16312 and select the number of segments and the number of grids (4 grids & 16 segments to 11 grids & 11 segments to). When these commands are executed, the display is forcibly turned off, and key scanning is also stopped. To resume display, the display command “ON” must be executed. If the same mode is selected, however, nothing happens.



On power application, the 11-digit, 11-segment mode is selected.

1.2 Data setting commands

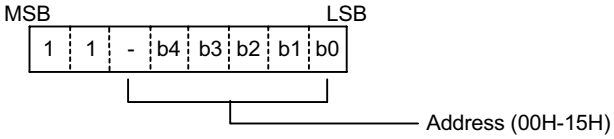
These commands set data write and data read modes.



On power application, the normal operation and address increment modes are set.

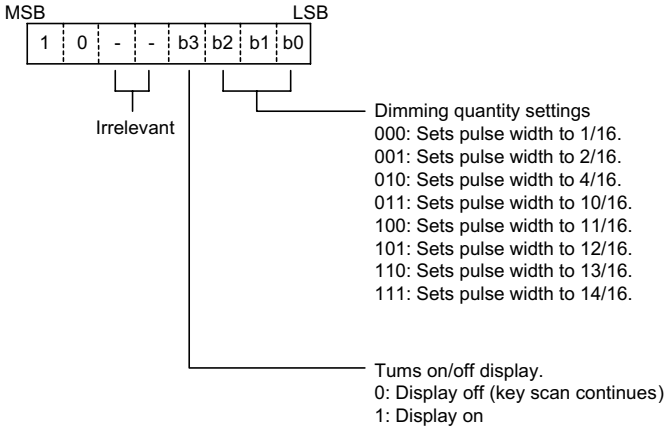
1.3 Address setting commands

These commands set an address of the display memory.



If address 16H or higher is set, data is ignored, until a valid address is set.
On power application, the address is set to 00H.

1.4 Display control commands



On power application, the 1/16-pulse width is set, the display is turned off and key scanning is stopped.

2.0 Display RAM Address and Display Mode

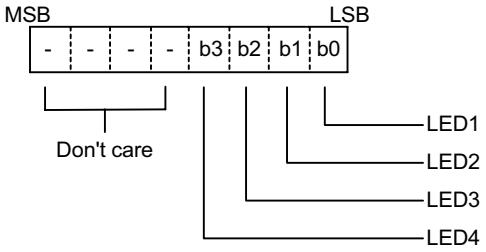
The display RAM stores the data transmitted from an external device to the AD16312 through the serial interface, and is assigned addresses as follows, in 8 bits unit:

Seg_1	Seg_4	Seg_8	Seg_{12}	Seg_{16}	
00 H_L	00 H_U	01 H_L	01 H_U	DIG_1
02 H_L	02 H_U	03 H_L	03 H_U	DIG_2
04 H_L	04 H_U	05 H_L	05 H_U	DIG_3
06 H_L	06 H_U	07 H_L	07 H_U	DIG_4
08 H_L	08 H_U	09 H_L	09 H_U	DIG_5
0 AH_L	0 AH_U	0 BH_L	0 BH_U	DIG_6
0 CH_L	0 CH_U	0 DH_L	0 DH_U	DIG_7
0 EH_L	0 EH_U	0 FH_L	0 FH_U	DIG_8
10 H_L	10 H_U	11 H_L	11 H_U	DIG_9
12 H_L	12 H_U	13 H_L	13 H_U	DIG_{10}
14 H_L	14 H_U	15 H_L	15 H_U	DIG_{11}

b0 b3	b4 b7
XX H_L	XXH_U
Lower 4 bits	Higher 4 bits

3.0 LED Port

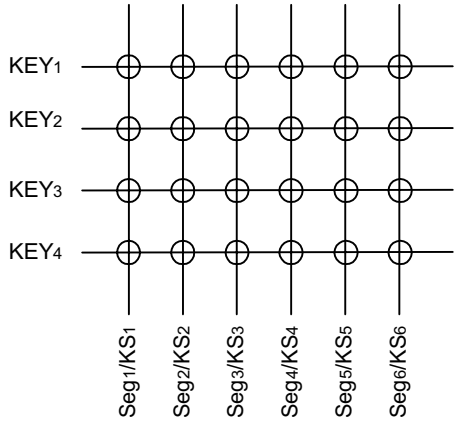
Data is written to the LED port with the write command , starting from the least port's least significant bit. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED turns off . The data of bits 5 through 8 are ignored.



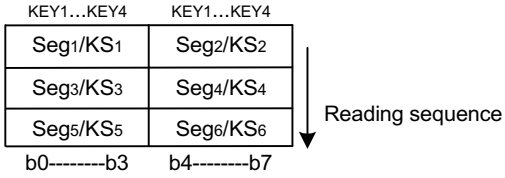
On power application, all LEDs are unlit.

4.0 Key Matrix and Key-Input data Storage RAM

The key matrix is made up of a 6× 4 matrix, as shown below.

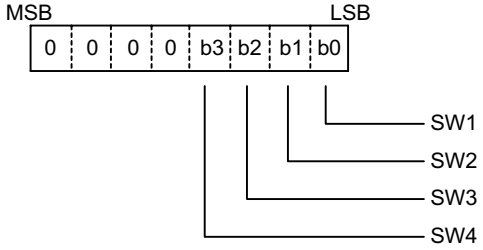


The data of each key is stored as illustrated below, and is read with the read command, starting from the least significant bit.



5.0 SW Data

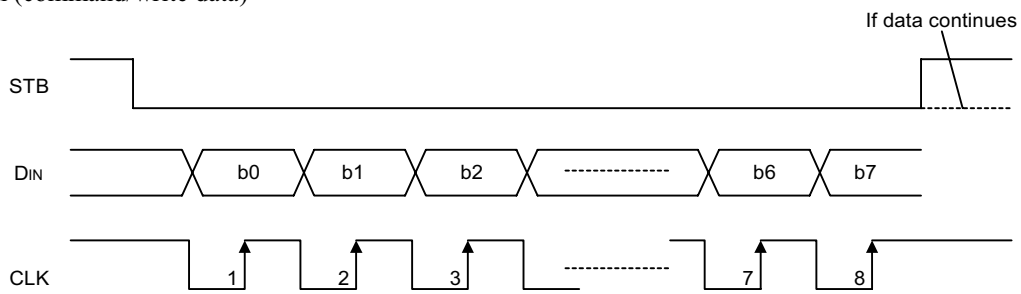
SW data is read with the read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



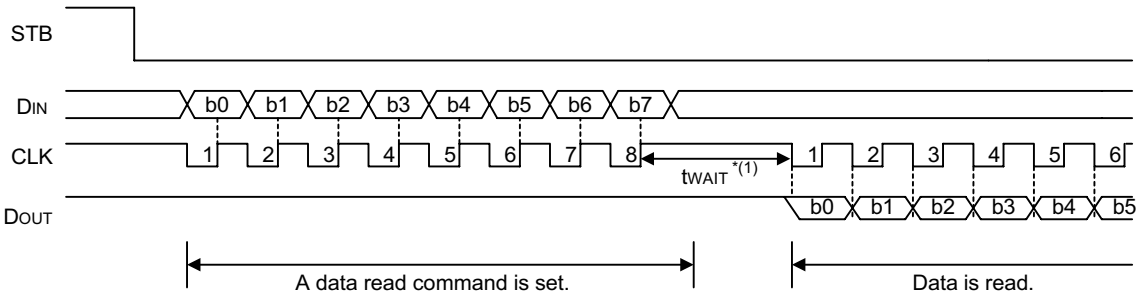
■ Timing Diagram

(1) Serial Communication Format

Reception (command/write data)



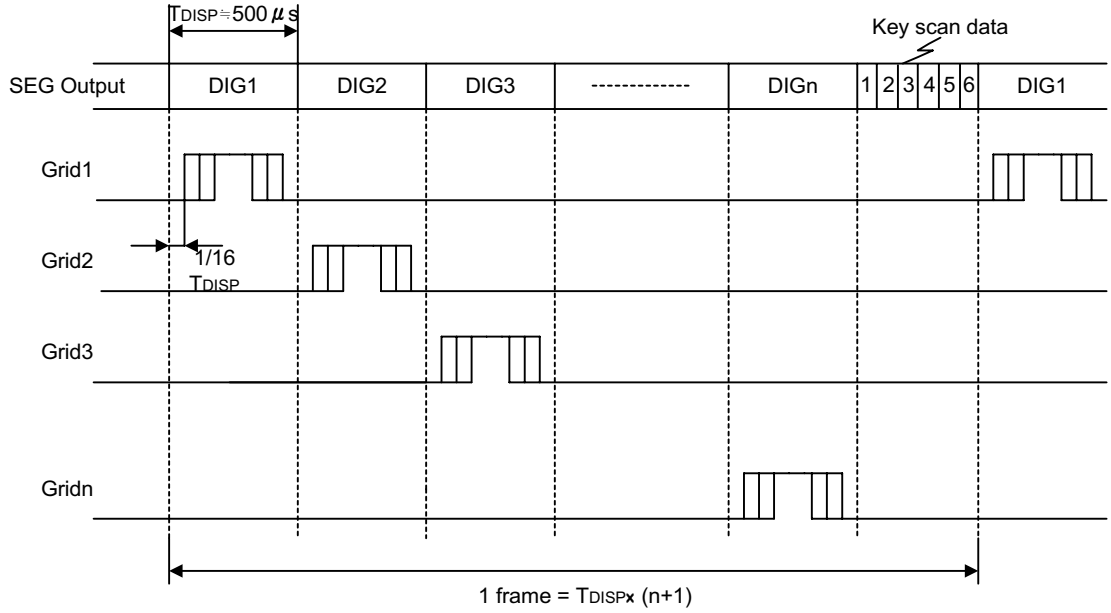
Transmission (read data)



Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

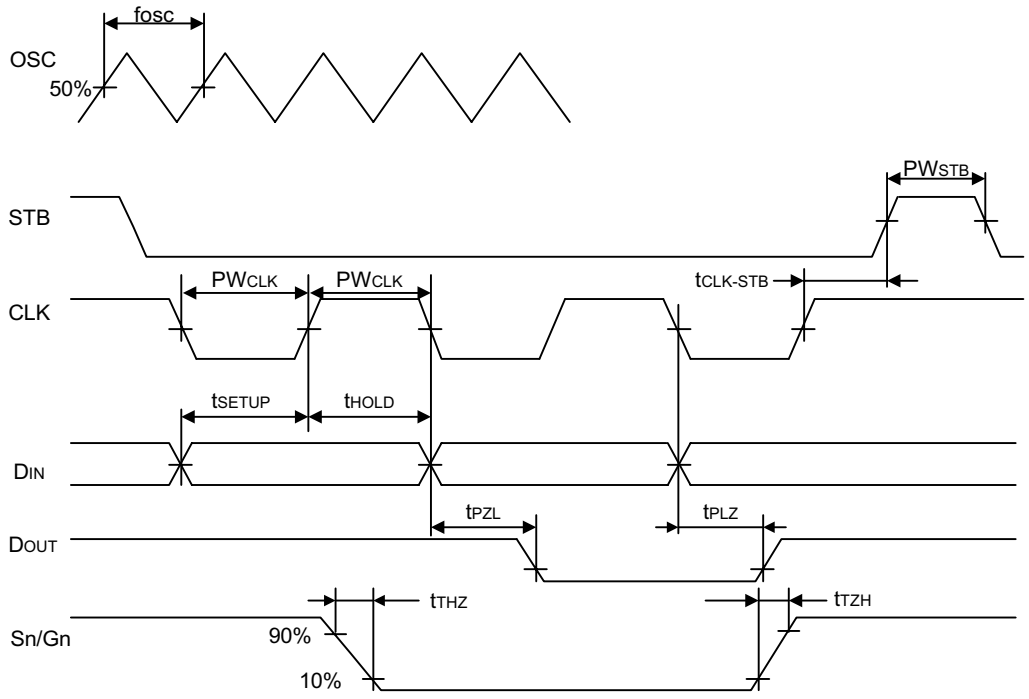
*(1): When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

(2) Key Scanning and Display Timing



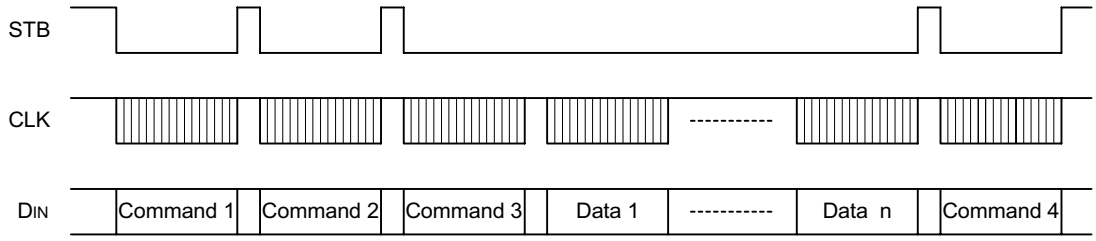
On cycle of key scanning consists of one frame, and data in a 6× 4 matrix is stored in RAM.

Switching Characteristic Waveforms



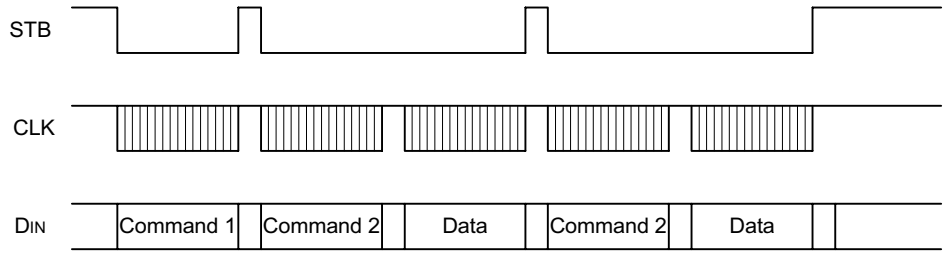
■ Applications

Updating display memory by incrementing address



Command 1: sets display mode
Command 2: sets data(write data to display memory)
Command 3: sets address
Data 1 to n: transfers display data (22bytes max.)
Command 4: controls display

Updating specific display memory



Command 1: sets data
Command 2: sets address
Data: display data

■ Package Dimension

(1) Package Type : QFP-44L