10-Bit, 100 MSPS A/D Converter

AD9071

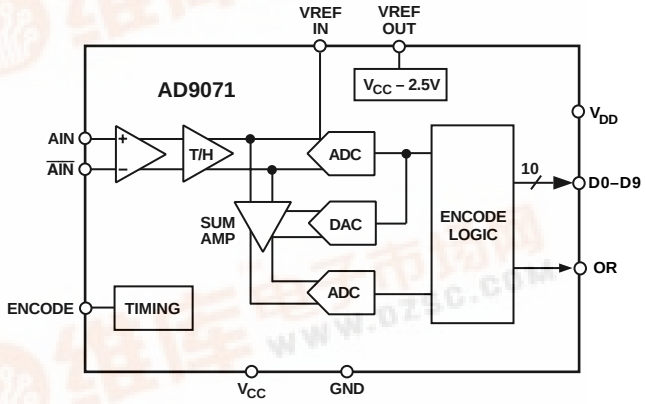
FEATURES

10-Bit, 100 MSPS ADC
Low Power: 450 mW at 100 MSPS
On-Chip Track/Hold
280 MHz Analog Bandwidth
SINAD = 54 dB @ 41 MHz
On-Chip Reference
1 V p-p Analog Input Range
Single +5 V Supply Operation
+5 V/+3.3 V Outputs

APPLICATIONS

Digital Communications
Signal Intelligence
Digital Oscilloscopes
Spectrum Analyzers
Medical Imaging
Sonar
HDTV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9071 is a monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and TTL/CMOS digital interfaces. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range.

The ADC requires only a single 5 V supply and an encode clock for full performance operation. The digital outputs are TTL compatible. Separate output power supply pins support interfacing with 3.3 V or 5 V logic. An out-of-range output (OR) is available that indicates a conversion result is outside the operating range. The output data are held at saturation levels during an out-of-range condition.

The input amplifier supports differential or single-ended interfaces. An internal reference is included.

Fabricated on an advanced BiCMOS process, the AD9071 is available in a plastic SOIC package specified over the industrial temperature range (–40°C to +85°C).

REV. B

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AD9071–SPECIFICATIONS (V_{CC} = +5 V, V_{DD} = +3.3 V, Differential Analog Input, ENCODE = 100 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9071BR Min	Typ	Max	Units
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity[1]	+25°C	I		±0.8	+1.5/–1.0	LSB
	Full	VI		±1.0	+1.75/–1.0	LSB
Integral Nonlinearity[1]	+25°C	I		±0.8	±1.5	LSB
	Full	VI		±1.25	±1.75	LSB
No Missing Codes[1]	+25°C	I		Guaranteed		
Gain Error[2]	+25°C	I		±1	±4	% FS
	Full	VI		±2	±8	% FS
Gain Tempco[2]	Full	V		150		ppm/°C
ANALOG INPUT						
Input Voltage Range (With Respect to $\overline{AIN}$)	Full	V		±512		mV p-p
Common-Mode Voltage	Full	V		–2.5 ± 0.2		V
Input Offset Voltage	+25°C	I		±4	±18	mV
	Full	VI		±5	±20	mV
Input Resistance	Full	VI	15	35		kΩ
Input Capacitance	+25°C	V		3		pF
Input Bias Current	+25°C	I		55	90	µA
	Full	VI		65	115	µA
Analog Bandwidth, Full Power	+25°C	V		280		MHz
REFERENCE OUTPUT						
Output Voltage	Full	VI	V_{CC} – 2.6	V_{CC} – 2.5	V_{CC} – 2.4	V
Temperature Coefficient	Full	V		130		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	100			MSPS
Minimum Conversion Rate	Full	IV			40	MSPS
Encode Pulsewidth High (t_{EH})	+25°C	IV	4.5		13	ns
Encode Pulsewidth Low (t_{EL})	+25°C	IV	4.5		13	ns
Aperture Delay (t_A)	+25°C	V		1.1		ns
Aperture Uncertainty (Jitter)	+25°C	V		3.0		ps, rms
Output Valid Time (t_V)[3]	Full	VI	2.0	4.0		ns
Output Propagation Delay (t_{PD})[3]	Full	VI		5.0	7.0	ns
Output Rise Time (t_R)	Full	V		1.4		ns
Output Fall Time (t_F)	Full	V		1.0		ns
DIGITAL INPUT						
Logic "1" Voltage	Full	VI	2.0			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			±10	µA
Logic "0" Current	Full	VI	–500			µA
Input Capacitance	+25°C	V		3		pF
DIGITAL OUTPUTS						
Logic "1" Voltage	Full	VI	V_{DD} – 0.5			V
Logic "0" Voltage	Full	VI			0.05	V
Output Coding				Offset Binary		
POWER SUPPLY						
V_{CC} Supply Current (V_{CC} = 5 V)[4]	Full	VI		85	115	mA
V_{DD} Supply Current (V_{DD} = 3.3 V)[4]	Full	VI		7.5	14	mA
Power Dissipation[4]	Full	VI		450	620	mW
Power Supply Sensitivity[5]	+25°C	I		0.002	0.010	V/V

Parameter	Temp	Test Level	AD9071BR Min	Typ	Max	Units
DYNAMIC PERFORMANCE[6]						
Transient Response	+25°C	V		4		ns
Overvoltage Recovery Time	+25°C	V		5		ns
Signal-to-Noise Ratio (SNR) (Without Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	54	56		dB
	Full	V		55		dB
f_{IN} = 41 MHz	+25°C	I	53	55		dB
	Full	V		54		dB
Signal-to-Noise Ratio (SINAD) (With Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	54	56		dB
	Full	V		55		dB
f_{IN} = 41 MHz	+25°C	I	52	54		dB
	Full	V		53		dB
Effective Number of Bits						
f_{IN} = 10.3 MHz	+25°C	I	8.8	9.2		Bits
f_{IN} = 41 MHz	+25°C	I	8.5	8.8		Bits
2nd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I	63	75		dBc
f_{IN} = 41 MHz	+25°C	I	60	66		dBc
3rd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I	65	75		dBc
f_{IN} = 41 MHz	+25°C	I	57	65		dBc
Two-Tone Intermodulation (IMD)						
f_{IN} = 10.3 MHz	+25°C	V		70		dBc
f_{IN} = 41 MHz	+25°C	V		60		dBc

NOTES

[1]Differential and integral nonlinearity based on F_S = 80 MSPS.

[2]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference).

[3]t_V and t_{PD} are measured from the threshold crossing of the ENCODE input to the 50% levels of the digital outputs. The output ac load during test is 5 pF.

[4]Power dissipation is measured under the following conditions: F_S @ 100 MSPS, analog input is –1 dBFS at 10.3 MHz.

[5]A change in input offset voltage with respect to a change in V_{CC}.

[6]SNR/harmonics based on an analog input voltage of –1.0 dBFS referenced to a 1.024 V full-scale input range.

Typical thermal impedance for the R style (SOIC) 28-lead package: θ_{JC} = 23°C/W, θ_{CA} = 48°C/W, θ_{JA} = 71°C/W.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} . . . . . +6 V
Analog Inputs . . . . . V_{CC} to 0.0 V
Digital Inputs . . . . . V_{CC} to 0.0 V
VREF IN, VREF OUT . . . . . V_{CC} to 0.0 V
Digital Output Current . . . . . 10 mA
Operating Temperature . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Case Temperature . . . . . +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at +25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9071 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9071BR	–40°C to +85°C	28-Lead Wide Body (SOIC)	R-28
AD9071/PCB	+25°C	Evaluation Board	

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 7, 12, 21, 23	GND	Ground.
2, 8, 11	V_{CC}	Analog Power Supply. Nominally 5.0 V. (Tie together to prevent a possible latch-up condition.)
3	VREF OUT	Internal Reference Output (V_{CC} – 2.5 V typical); Bypass with 0.1 µF to V_{CC}.
4	VREF IN	Reference Input for ADC (V_{CC} – 2.5 V typical).
5, 6	DNC	Do Not Connect.
9	$\overline{AIN}$	Analog Input – Complementary.
10	AIN	Analog Input – True.
13	ENCODE	Encode clock for ADC. (ADC Samples on Rising Edge of ENCODE.)
14	OR	Out-of-Range Output. Goes HIGH when the converted sample is more positive than $3FF_H$ or more negative than 000_H (offset binary coding).
15–19, 24–28	D9–D0	Digital outputs of ADC. D9 is the MSB. Data is offset binary.
20, 22	V_{DD}	Digital Output Power Supply. User selectable range from 3 V to 5 V.

PIN CONFIGURATION

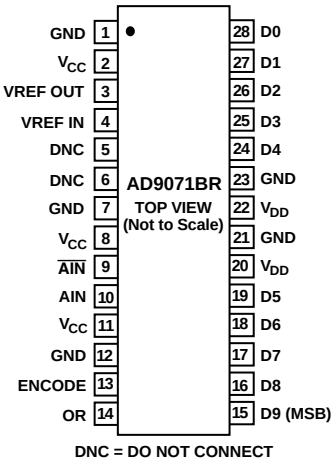


Table I. Output Coding

Code	AIN–$\overline{AIN}$	Offset Binary	OR
1023	≥ 0.512 V	11 1111 1111	1
1023	0.511 V	11 1111 1111	0
1022	0.510 V	11 1111 1110	0
•	•	•	•
•	•	•	•
•	•	•	•
513	0.001 V	10 0000 0001	0
512	0.000 V	10 0000 0000	0
511	–0.001 V	01 1111 1111	0
•	•	•	•
•	•	•	•
•	•	•	•
1	–0.511 V	00 0000 0001	0
0	–0.512 V	00 0000 0000	0
0	≤–0.513 V	00 0000 0000	1

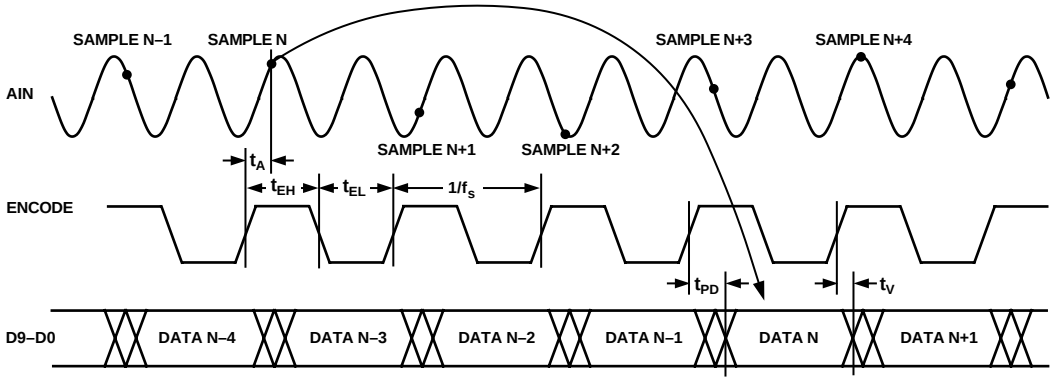


Figure 1. Timing Diagram

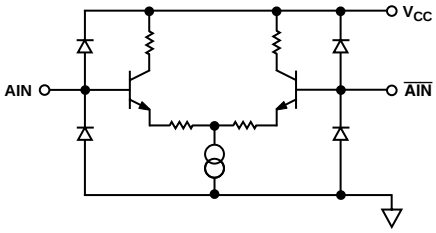


Figure 2. Equivalent Analog Input Circuit

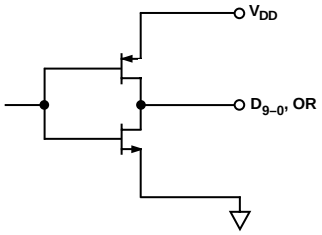


Figure 5. Equivalent Digital Output Circuit

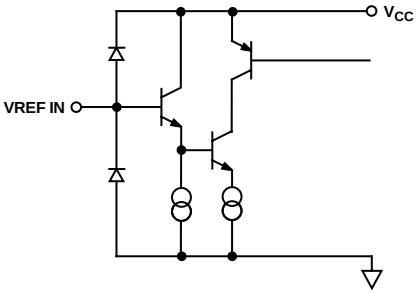


Figure 3. Equivalent Reference Input Circuit

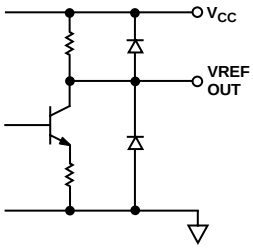


Figure 6. Equivalent Reference Output Circuit

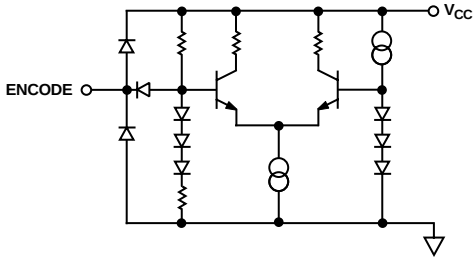


Figure 4. Equivalent Encode Input Circuit

AD9071–Typical Performance Characteristics

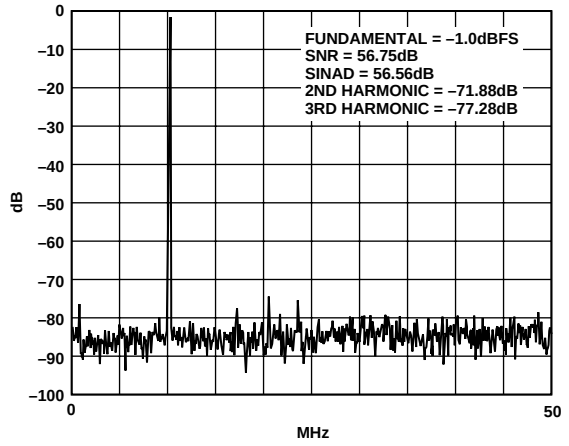


Figure 7. Spectrum: F_S = 100 MSPS, f_{IN} = 10.3 MHz

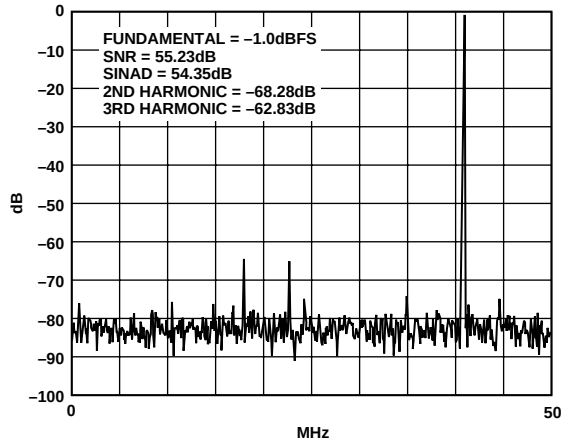


Figure 8. Spectrum: F_S = 100 MSPS, f_{IN} = 41 MHz

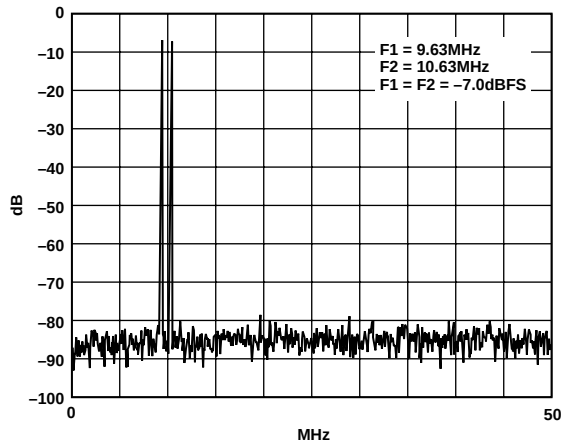


Figure 9. Two-Tone Intermodulation Distortion

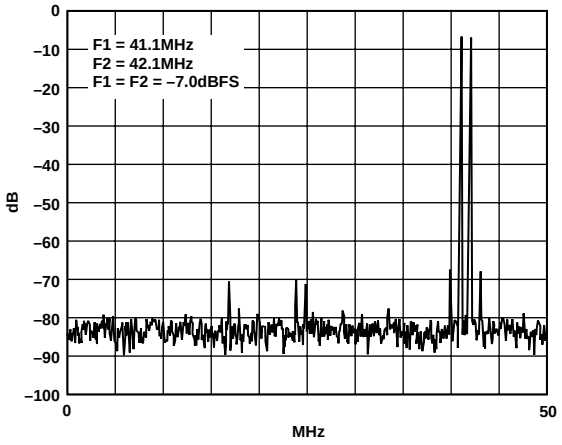


Figure 10. Two-Tone Intermodulation Distortion

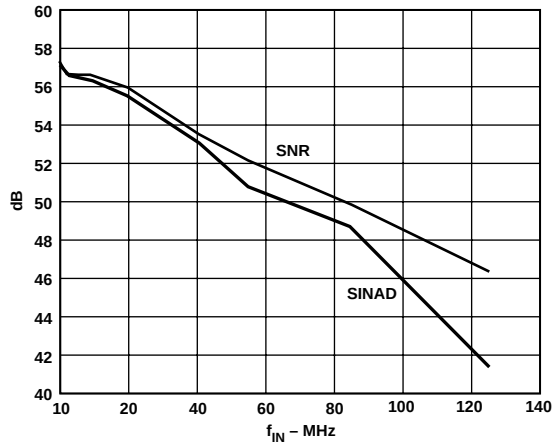


Figure 11. SINAD/SNR vs. f_{IN}: F_S = 100 MSPS

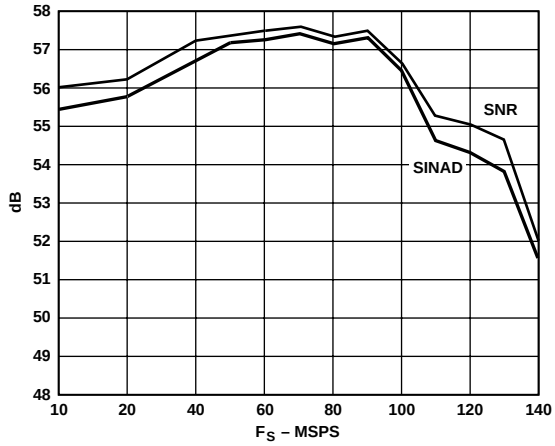


Figure 12. SINAD/SNR vs. F_S: f_{IN} = 10.3 MHz

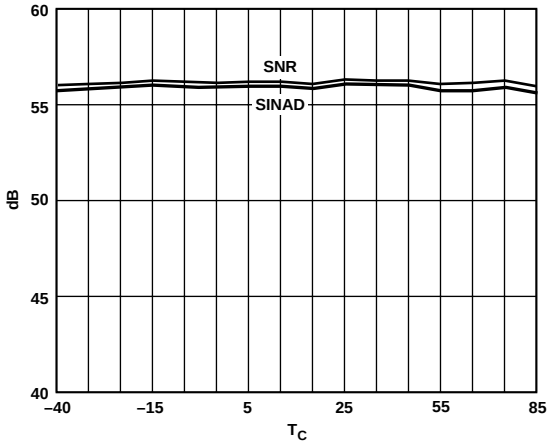


Figure 13. Differential SNR vs. T_C: f_{IN} = 10.3 MHz

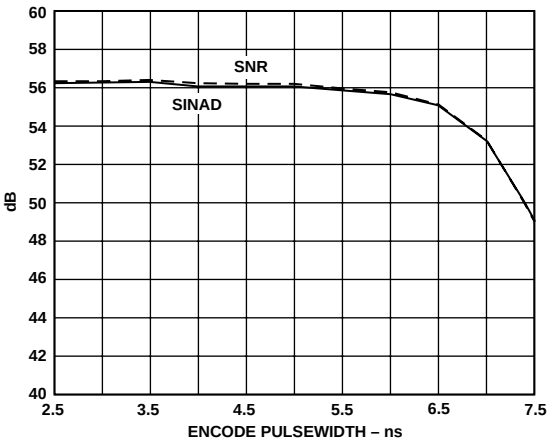


Figure 15. SNR vs. Clock Pulsewidth (t_{EH}): f_{IN} = 10.3 MHz

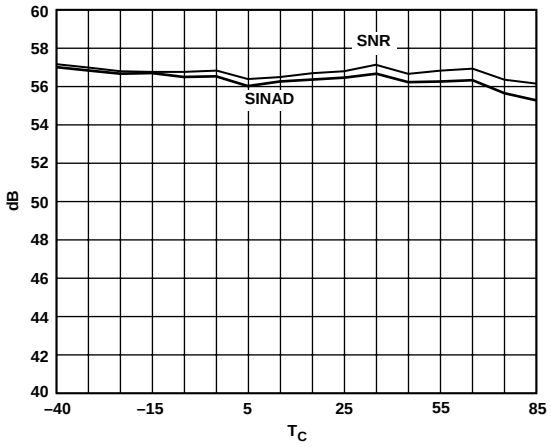


Figure 14. Single-Ended SNR vs. T_C: f_{IN} = 10.3 MHz

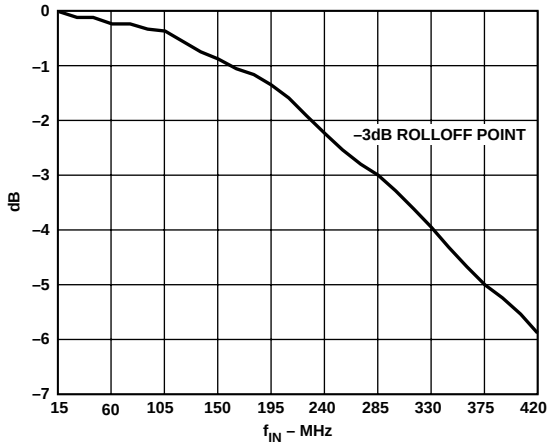


Figure 16. Frequency Response

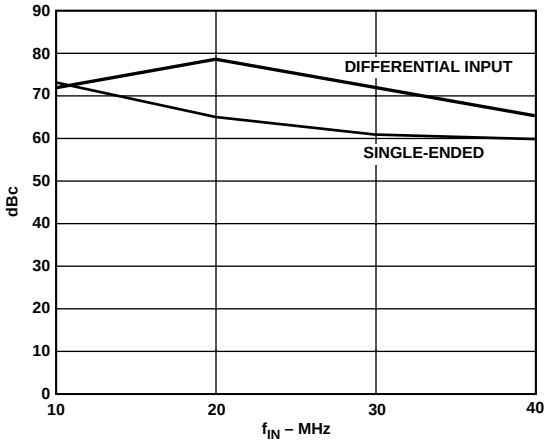


Figure 17. Second Harmonic Performance: Single-Ended vs. Differential Input

APPLICATION NOTES

THEORY OF OPERATION

The AD9071 employs a two-step subranging architecture with digital error correction.

The sampling and conversion process is initiated by a rising edge at the ENCODE input. The analog input signal is buffered by a high speed differential amplifier and applied to a track-and-hold (T/H) circuit, which captures the value of the input at the sampling instant and maintains it for the duration of the conversion.

The coarse quantizer (ADC) produces a 5-bit estimate of the input value. Its digital output is reconverted to analog form by the reconstruction DAC and subtracted from the input signal in the SUM AMP. The second stage quantizer generates a 6-bit representation of the difference signal. The eleven bits are presented to the ENCODE LOGIC, which corrects for range overlap errors and produces an accurate 10-bit result.

Data are strobed to the output on the rising edge of the ENCODE input, with the data from sample N appearing on the output following ENCODE rising edge N+3.

USING THE AD9071

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9071, and the user is advised to give commensurate thought to the clock source. The lowest jitter clock source is a crystal oscillator producing a pure sine wave.

The ENCODE input is fully TTL/CMOS compatible.

Digital Outputs

The digital outputs are CMOS compatible for lower power consumption. 200 Ω series resistors are recommended between the AD9071 and the receiving logic to reduce transients and improve SNR.

Analog Input

The analog input has been optimized for differential signal input.

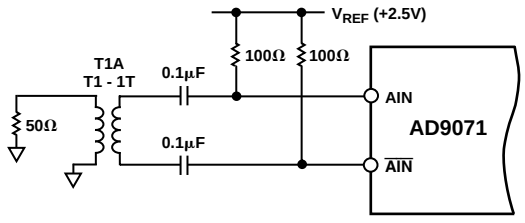


Figure 18. Differential Analog Input Configuration

If driven single-endedly, the $\overline{\text{AIN}}$ should be connected to a clean reference and bypassed to ground. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match.

Special care was taken in the design of the analog input section of the AD9071 to prevent damage and corruption of data when the input is overdriven. The nominal input range is +1.988 V to +3.012 V (1.024 V p-p centered at +2.5 V). Out-of-range comparators detect when the analog input signal is out of this range, and set the OR output signal HIGH. The digital outputs are locked at plus or minus full scale ($3FF_H$ or 200_H) for voltages that are out of range, but between 1 V and 5 V. Input voltages outside of this range may result in invalid codes at the ADC's output.

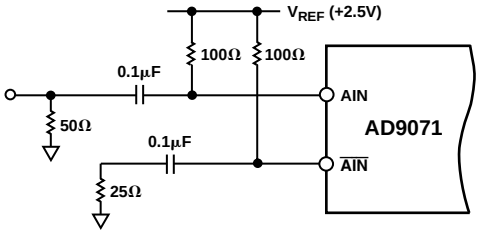


Figure 19. Single-Ended Analog Input Configuration

When the analog input signal returns to the nominal range, the out-of-range comparators return the ADC to its active mode and the device recovers in the overvoltage recovery time.

Voltage Reference

A stable and accurate 2.5 V voltage reference (V_{CC} – 2.5 V) is built into the AD9071 (VREF OUT). In normal operation, the internal reference is used by strapping Pins 3 and 4 of the AD9071 together. The internal reference can provide 100 μA of extra drive current that may be used for other circuits.

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain of the AD9071, which cannot be obtained by using the internal reference. For these applications, an external 2.5 V reference can be connected to VREF IN, which requires 5 μA of drive current (see Figure 20).

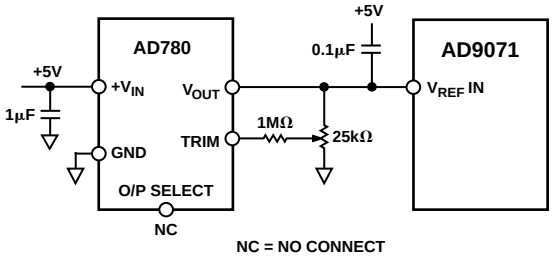


Figure 20. Using the AD780 Voltage Reference

The input range can be adjusted by varying the reference voltage applied to the AD9071. No appreciable degradation in performance occurs when the reference is adjusted ±4%. The full-scale range of the ADC tracks reference voltage changes linearly.

Timing

The performance of the AD9071 is insensitive to the duty cycle of the clock over a wide range of operating conditions (see Figure 15).

The AD9071 provides latched data outputs, with three pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see Figure 1). The length of the output data lines, and loads placed on them, should be minimized to reduce transients within the AD9071; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9071 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade. The AD9070 will operate in bursts, but the user must flush the internal pipeline each time the clock restarts. Valid data will be produced on the fourth rising edge of the ENCODE signal after the clock is restarted.

EVALUATION BOARD

The AD9071 evaluation board is a convenient and easy way to evaluate the performance of the AD9071 in the SOIC package. The board consists of an internal voltage reference or an optional external reference, two 74LCX574 latches for capturing data from the A/D converter, and an AD9760 DAC for viewing reconstructed A/D data. The AD9071 output logic can be driven at 5 V and 3.3 V levels. The latches are set up at 3.3 V but are 5 V tolerant. Test points are provided at Encode, DB9, DB0, Data Ready, and Data Clock. All are clearly labeled.

Analog Input

The evaluation board can be driven single-ended or differentially. Differential input requires using a 1:1 transformer. For single-ended operation (J2), Jumper S5 is connected to S8 and S6 is connected to S7. For differential input operation (J3), S5 is connected to S3 and S4 is connected to S6. The board is shipped in the differential configuration.

Encode

The AD9071 encode inputs are driven single-ended into J1 and are at TTL logic levels.

Data Out

The data delivered out of the AD9071 is in offset binary format at TTL levels. The Data Ready signal can be inverted by opening the S1 and S2 connections. An optional series termination resistor on Data Ready (R33), normally 0 ohms, is provided to support various user output impedance configurations. The AD9760 DAC supports viewing reconstructed A/D data at J4.

Voltage Reference

The AD9071 can be operated using its internal voltage reference (connect E2 to E3) or an optional external reference (connect E1 to E2). The board is shipped utilizing the internal voltage reference.

Layout

The AD9071 is not layout sensitive if some important guidelines are met. The evaluation board layout provides an example where these guidelines have been followed to optimize performance.

- Provide a good ground plane connecting the analog and digital sections.
- Excellent bypassing is essential. Chip capacitors with 0.1 µF values and 0803 dimensions are placed flush against the pins. Placing any of the capacitors on the bottom of the board can degrade performance. These techniques reduce the amount of parasitic inductance that can impact the bypassing ability of the caps.
- Separate power planes and supplies for the analog and digital sections are recommended.

The AD9071 evaluation board is provided as a design example for customers of Analog Devices. ADI makes no warranties express, statutory, or implied regarding merchantability or fitness for a particular purpose.

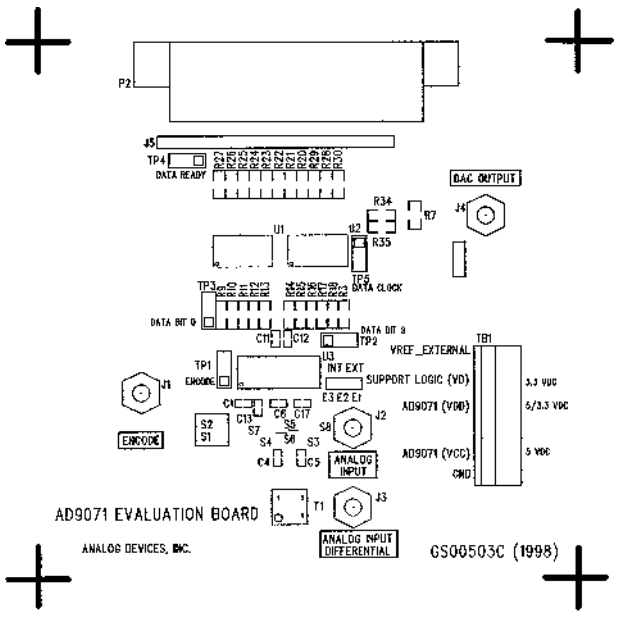


Figure 21. Printed Circuit Board Top Side Silkscreen

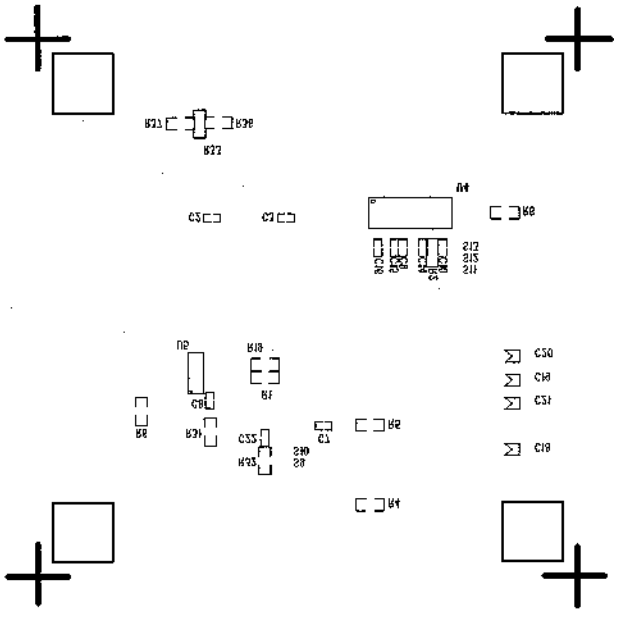


Figure 22. Printed Circuit Board Bottom Side Silkscreen

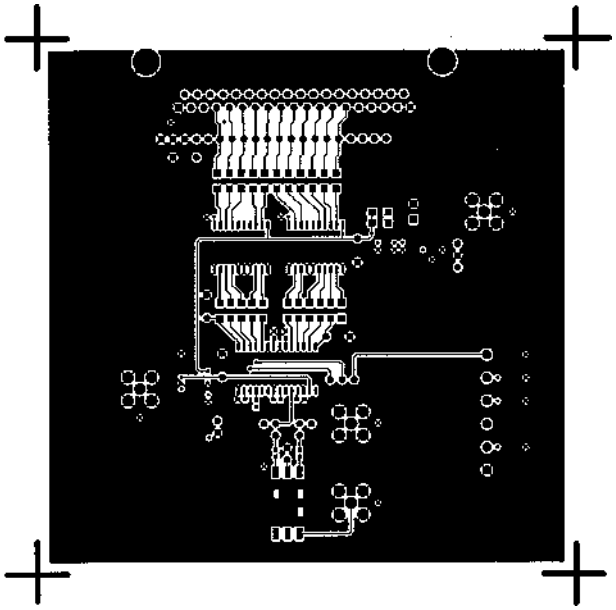


Figure 23. Printed Circuit Board Top Side Copper

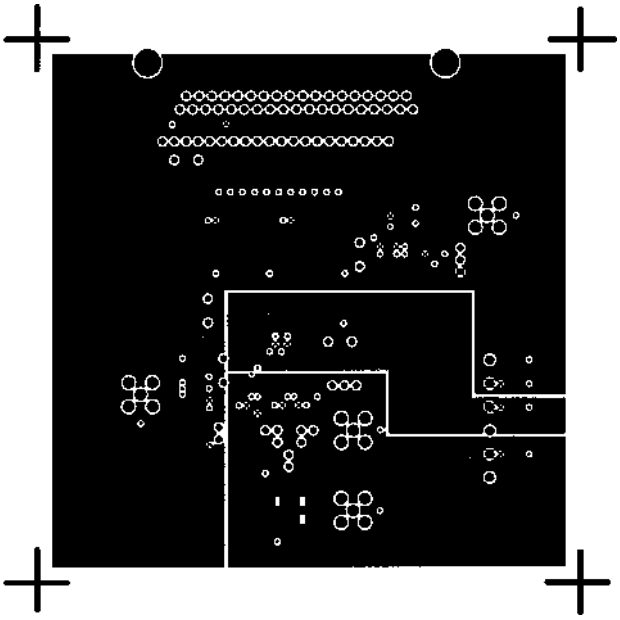


Figure 25. Printed Circuit Board "Split" Power Layer

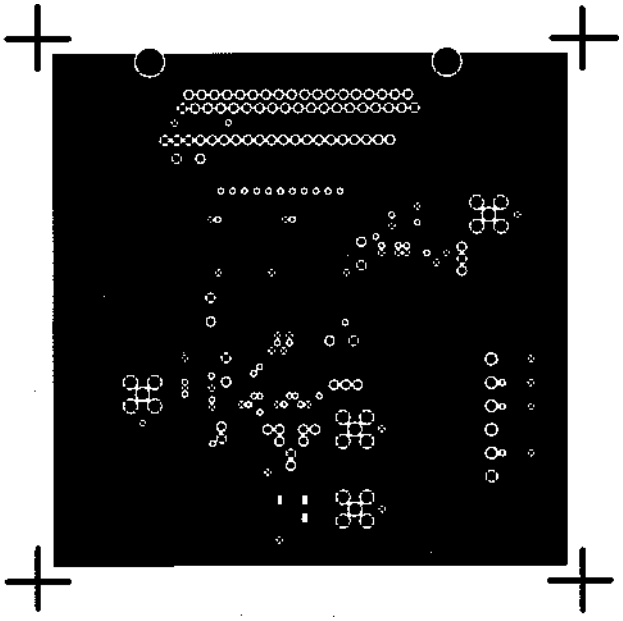


Figure 24. Printed Circuit Board Ground Layer

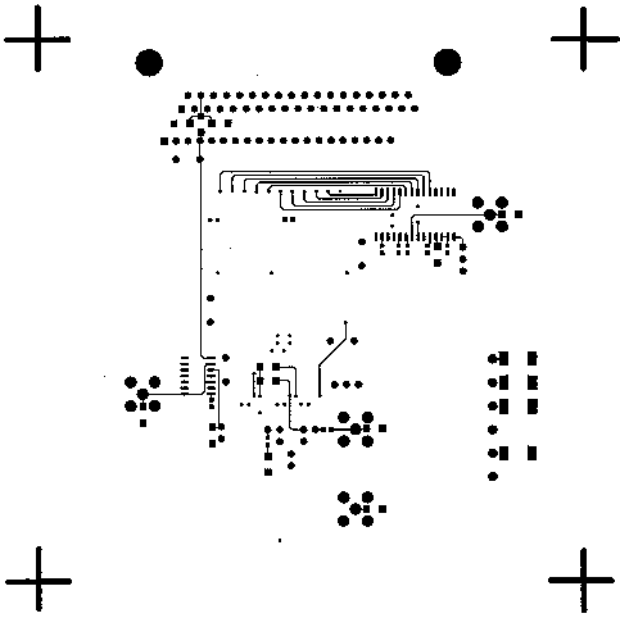


Figure 26. Printed Circuit Board Bottom Side Copper

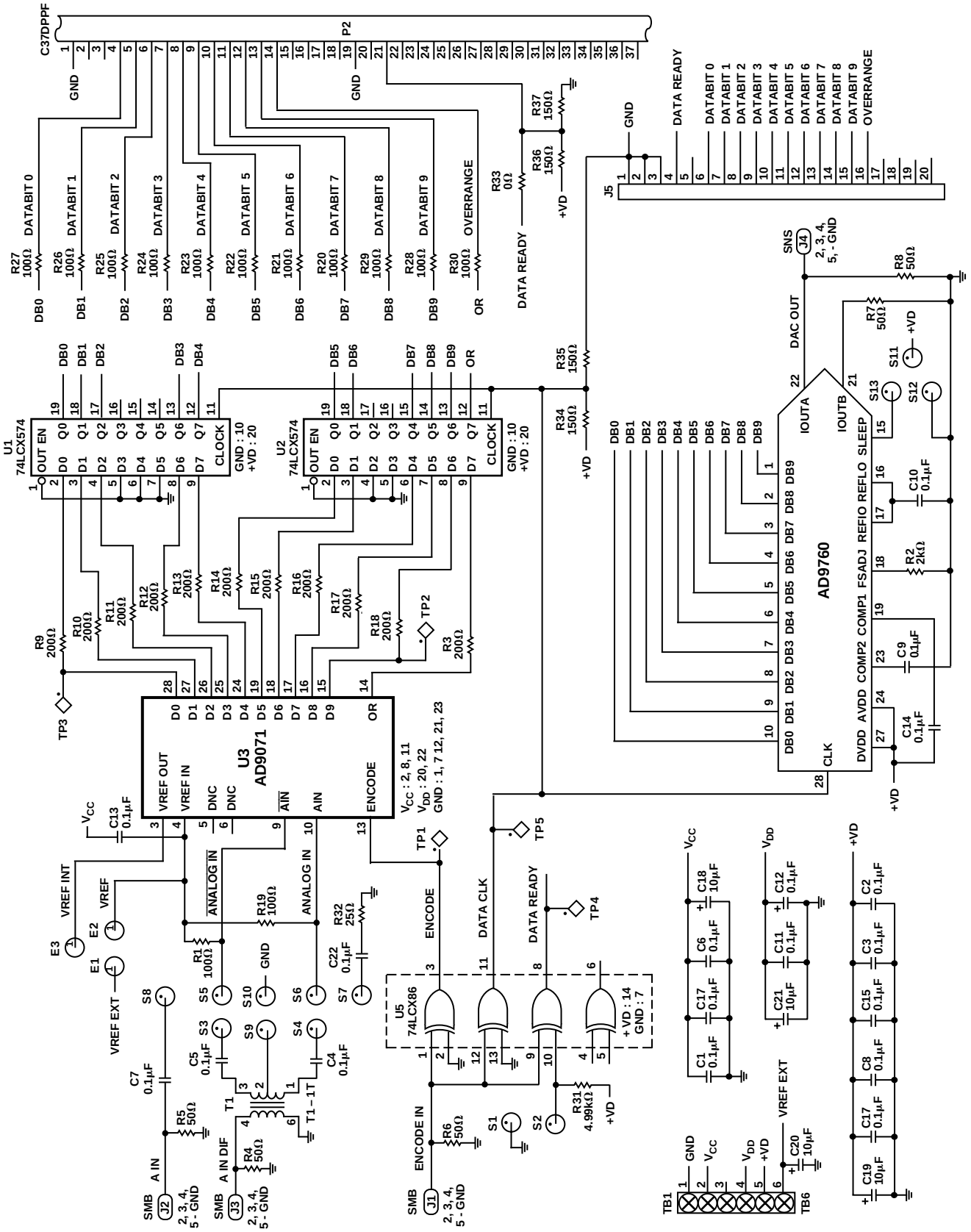


Figure 27. Printed Circuit Board Schematic

Table II. Printed Circuit Board Bill of Materials

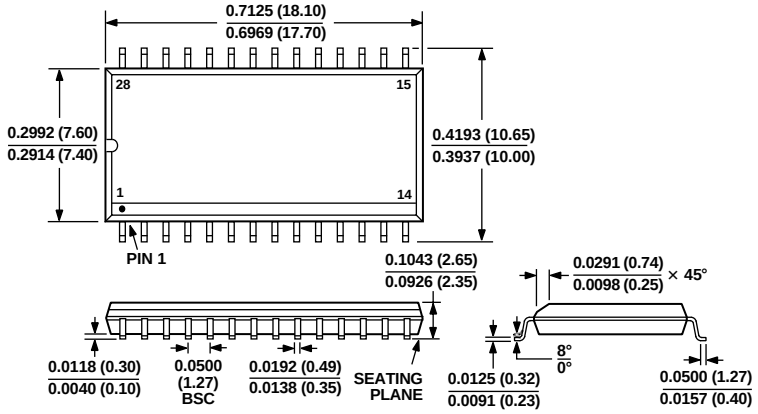
Item #	Quantity	Reference	Description
1	18	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C22	Ceramic Chip Capacitor, 0603, 0.1 µF
2	4	C18, C19, C20, C21	Tantalum Chip Capacitor, 10 µF
3	3	E1, E2, E3	Jumpers
4	4	J1, J2, J3, J4	SMB-P Connector
5	1	J5	20-Pin Male Header
6	1	P2	37-Pin Connector (Amp 747462-4)
7	13	R1, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30	Surface Mount Resistor, 1206, 100 Ω
8	1	R2	Surface Mount Resistor, 1206, 2000 Ω
9	11	R3, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18	Surface Mount Resistor, 1206, 200 Ω
10	5	R4, R5, R6, R7, R8	Surface Mount Resistor, 1206, 50 Ω
11	1	R31	Surface Mount Resistor, 1206, 5000 Ω
12	1	R32	Surface Mount Resistor, 1206, 25 Ω
13	1	R33	Surface Mount Resistor, 1206, 0 Ω
14	4	R34, R35, R36, R37	Surface Mount Resistor, 1206, 150 Ω
15	13	S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13	Jumpers
16	1	T1	Surface Mount Transformer Mini-Circuit T1-T1, 1:1 Ratio
17	1	TB1	6-Pin Wieland Connector (P/N # 25,602, 2653.0; 25.530 3625.0)
18	5	TP1, TP2, TP3, TP4, TP5	Test Points
19	2	U1, U2	74LCX574 Octal Latch
20	1	U3	AD9071BR, 10-Bit, 100 MSPS, ADC
21	1	U4	AD9760AR, 10-Bit, 125 MSPS, DAC
22	1	U5	74LCX86, XOR

C3331b–0–5/99

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Wide Body SOIC
(R-28)



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