



# High Speed, 3.3 V/5 V Quad 2:1 Mux/Demux (4-Bit, 1 of 2) Bus Switch

## ADG3257

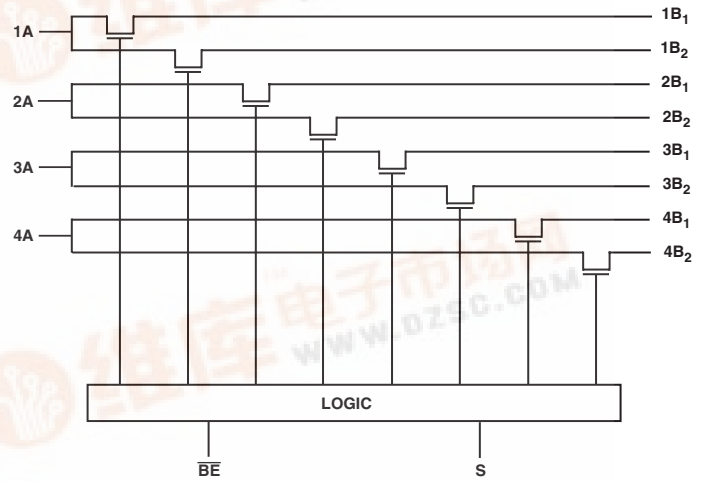
### FEATURES

- 100 ps Propagation Delay through the Switch
- 2 Ω Switches Connect Inputs to Outputs
- Data Rates up to 933 Mbps
- Single 3.3 V/5 V Supply Operation
- Level Translation Operation
- Ultralow Quiescent Supply Current (1 nA Typical)
- 3.5 ns Switching
- Standard '3257 Type Pinout

### APPLICATIONS

- Bus Switching
- Bus Isolation
- Level Translation
- Memory Switching/Interleaving

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The ADG3257 is a CMOS bus switch comprised of four 2:1 multiplexers/demultiplexers with high impedance outputs. The device is manufactured on a CMOS process. This provides low power dissipation yet high switching speed and very low ON resistance, allowing the inputs to be connected to the outputs without adding propagation delay or generating additional ground bounce noise.

The ADG3257 operates from a single 3.3 V/5 V supply. The control logic for each switch is shown in Table I. These switches are bidirectional when ON. In the OFF condition, signal levels are blocked up to the supplies.

This bus switch is suited to both switching and level translation applications. It may be used in applications requiring level translation from 3.3 V to 2.5 V when powered from 3.3 V. Additionally, with a diode connected in series with 5 V V<sub>DD</sub>, the ADG3257 may also be used in applications requiring 5 V to 3.3 V level translation.

### PRODUCT HIGHLIGHTS

1. 0.1 ns propagation delay through switch
2. 2 Ω switches connect inputs to outputs
3. Bidirectional operation
4. Ultralow power dissipation
5. 16-lead QSOP package

Table I. Truth Table

$\overline{BE}$	S	Function
H	X	DISABLE
L	L	A = B <sub>1</sub>
L	H	A = B <sub>2</sub>

REV. C

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# ADG3257—SPECIFICATIONS<sup>1</sup> (V<sub>CC</sub> = 5.0 V ± 10%, GND = 0 V. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

Parameter	Symbol	Conditions <sup>2</sup>	B Version			Unit
			Min	Typ <sup>3</sup>	Max	
<b>DC ELECTRICAL CHARACTERISTICS</b>						
Input High Voltage	V <sub>INH</sub>		2.4			V
Input Low Voltage	V <sub>INL</sub>		-0.3		+0.8	V
Input Leakage Current	I <sub>I</sub>	0 ≤ V <sub>IN</sub> ≤ 5.5 V		±0.01	±1	μA
OFF State Leakage Current	I <sub>OZ</sub>	0 ≤ A, B ≤ V <sub>CC</sub>		±0.01	±1	μA
ON State Leakage Current	I <sub>OZ</sub>	0 ≤ A, B ≤ V <sub>CC</sub>		±0.01	±1	μA
Max Pass Voltage <sup>4</sup>	V <sub>P</sub>	V <sub>IN</sub> = V <sub>CC</sub> = 5 V, I <sub>O</sub> = -5 μA	3.9	4.2	4.4	V
<b>CAPACITANCE<sup>4</sup></b>						
A Port OFF Capacitance	C <sub>A OFF</sub>	f = 1 MHz		7		pF
B Port OFF Capacitance	C <sub>B OFF</sub>	f = 1 MHz		5		pF
A, B Port ON Capacitance	C <sub>A</sub> , C <sub>B ON</sub>	f = 1 MHz		11		pF
Control Input Capacitance	C <sub>IN</sub>	f = 1 MHz		4		pF
<b>SWITCHING CHARACTERISTICS<sup>4</sup></b>						
Propagation Delay A to B or B to A t <sub>PD</sub>	t <sub>PHL</sub> , t <sub>PLH</sub> <sup>5</sup>	V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF			0.10	ns
Propagation Delay Matching <sup>6</sup>		V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF		0.0075	0.035	ns
Bus Enable Time $\overline{BE}$ to A or B	t <sub>PZH</sub> , t <sub>PZL</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1	5	7.5	ns
Bus Disable Time $\overline{BE}$ to A or B	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1	3.5	7	ns
Bus Select Time S to A or B						
Enable	t <sub>SEL_EN</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω		8	12	ns
Disable	t <sub>SEL_DIS</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω		5	8	ns
Max Data Rate		V <sub>A</sub> = 2 V p-p		933		Mbps
<b>DIGITAL SWITCH</b>						
ON Resistance	R <sub>ON</sub>	V <sub>A</sub> = 0 V I <sub>O</sub> = 48 mA, 15 mA, 8 mA, T <sub>A</sub> = 25°C I <sub>O</sub> = 48 mA, 15 mA, 8 mA V <sub>A</sub> = 2.4 V		2	3	Ω
		I <sub>O</sub> = 48 mA, 15 mA, 8 mA, T <sub>A</sub> = 25°C			4	Ω
ON Resistance Matching	ΔR <sub>ON</sub>	V <sub>A</sub> = 0 V 48 mA, 15 mA, 8 mA, T <sub>A</sub> = 25°C V <sub>A</sub> = 0 V, 48 mA, 15 mA, 8 mA		3	5	Ω
					6	Ω
				0.15	0.35	Ω
					0.7	Ω
<b>POWER REQUIREMENTS</b>						
V <sub>CC</sub>			3.0		5.5	V
Quiescent Power Supply Current	I <sub>CC</sub>	Digital Inputs = 0 V or V <sub>CC</sub>		0.001	1	μA
Increase in I <sub>CC</sub> per Input <sup>7</sup>	ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, One Input at 3.0 V; Others at V <sub>CC</sub> or GND			200	μA

## NOTES

<sup>1</sup>Temperature range is as follows: B Version: -40°C to +85°C.

<sup>2</sup>See Test Circuits and Waveforms.

<sup>3</sup>All typical values are at T<sub>A</sub> = 25°C, unless otherwise noted.

<sup>4</sup>Guaranteed by design, not subject to production test.

<sup>5</sup>The digital switch contributes no propagation delay other than the RC delay of the typical R<sub>ON</sub> of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

<sup>6</sup>Propagation delay matching between channels is calculated from ON resistance matching of worst-case channel combinations and load capacitance.

<sup>7</sup>This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition. This parameter is guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS<sup>1</sup> ( $V_{CC} = 3.3\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ . All specifications $T_{MIN}$ to $T_{MAX}$ , unless otherwise noted.)

Parameter	Symbol	Conditions <sup>2</sup>	B Version			Unit
			Min	Typ <sup>3</sup>	Max	
<b>DC ELECTRICAL CHARACTERISTICS</b>						
Input High Voltage	$V_{INH}$		2.0			V
Input Low Voltage	$V_{INL}$		-0.3		+0.8	V
Input Leakage Current	$I_I$	$0 \leq V_{IN} \leq 3.6\text{ V}$		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
OFF State Leakage Current	$I_{OZ}$	$0 \leq A, B \leq V_{CC}$		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
ON State Leakage Current	$I_{OZ}$	$0 \leq A, B \leq V_{CC}$		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
Max Pass Voltage <sup>4</sup>	$V_P$	$V_{IN} = V_{CC} = 3.3\text{ V}$ , $I_O = -5\text{ }\mu\text{A}$	2.3	2.6	2.8	V
<b>CAPACITANCE<sup>4</sup></b>						
A Port OFF Capacitance	$C_A\text{ OFF}$	$f = 1\text{ MHz}$		7		pF
B Port OFF Capacitance	$C_B\text{ OFF}$	$f = 1\text{ MHz}$		5		pF
A, B Port ON Capacitance	$C_A, C_B\text{ ON}$	$f = 1\text{ MHz}$		11		pF
Control Input Capacitance	$C_{IN}$	$f = 1\text{ MHz}$		4		pF
<b>SWITCHING CHARACTERISTICS<sup>4</sup></b>						
Propagation Delay A to B or B to A $t_{PD}$	$t_{PHL}, t_{PLH}$ <sup>5</sup>	$V_A = 0\text{ V}$ , $C_L = 50\text{ pF}$			0.10	ns
Propagation Delay Matching <sup>6</sup>		$V_A = 0\text{ V}$ , $C_L = 50\text{ pF}$		0.01	0.04	ns
Bus Enable Time $\overline{BE}$ to A or B	$t_{PZH}, t_{PZL}$	$C_L = 50\text{ pF}$ , $R_L = 500\text{ }\Omega$	1	5.5	9	ns
Bus Disable Time $\overline{BE}$ to A or B	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{ pF}$ , $R_L = 500\text{ }\Omega$	1	4.5	8.5	ns
Bus Select Time S to A or B						
Enable	$t_{SEL\_EN}$	$C_L = 50\text{ pF}$ , $R_L = 500\text{ }\Omega$		8	12	ns
Disable	$t_{SEL\_DIS}$	$C_L = 50\text{ pF}$ , $R_L = 500\text{ }\Omega$		6	9	ns
Max Data Rate		$V_A = 2\text{ Vp-p}$		933		Mbps
<b>DIGITAL SWITCH</b>						
ON Resistance	$R_{ON}$	$V_A = 0\text{ V}$ $I_O = 15\text{ mA}$ , $8\text{ mA}$ , $T_A = 25^\circ\text{C}$		2	4	$\Omega$
		$V_A = 1.7\text{ V}$ , $I_O = 15\text{ mA}$ , $T_A = 25^\circ\text{C}$		8	16.5	$\Omega$
		$V_A = 1.7\text{ V}$ , $I_O = 8\text{ mA}$ , $T_A = 25^\circ\text{C}$		7	14	$\Omega$
					17	$\Omega$
ON Resistance Matching	$\Delta R_{ON}$	$V_A = 0\text{ V}$ , $15\text{ mA}$ , $8\text{ mA}$ , $T_A = 25^\circ\text{C}$ $V_A = 0\text{ V}$ , $15\text{ mA}$ , $8\text{ mA}$		0.2	0.4	$\Omega$
					0.8	$\Omega$
<b>POWER REQUIREMENTS</b>						
$V_{CC}$			3.0		5.5	V
Quiescent Power Supply Current	$I_{CC}$	Digital Inputs = $0\text{ V}$ or $V_{CC}$		0.001	1	$\mu\text{A}$
Increase in $I_{CC}$ per Input <sup>7</sup>	$\Delta I_{CC}$	$V_{CC} = 3.3\text{ V}$ , One Input at $3.0\text{ V}$ ; Others at $V_{CC}$ or $GND$			200	$\mu\text{A}$

**NOTES**

<sup>1</sup>Temperature range is as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>See Test Circuits and Waveforms.

<sup>3</sup>All typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

<sup>4</sup>Guaranteed by design, not subject to production test.

<sup>5</sup>The digital switch contributes no propagation delay other than the RC delay of the typical  $R_{ON}$  of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

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Specifications subject to change without notice.

# ADG3257

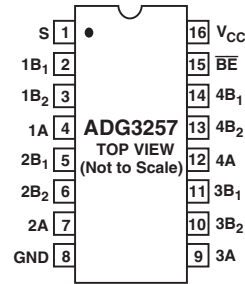
## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>CC</sub> to GND	−0.3 V to +6 V
Digital Inputs to GND	−0.3 V to +6 V
DC Input Voltage	−0.3 V to +6 V
DC Output Current	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QSOP Package	
θ <sub>JA</sub> Thermal Impedance	149.97°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

## PIN CONFIGURATION



## PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
$\overline{BE}$	Output Enable (Active Low)
S	Port Select
A <sub>x</sub>	Port A, Inputs or Outputs
B <sub>x</sub>	Port B, Inputs or Outputs

## ORDERING GUIDE

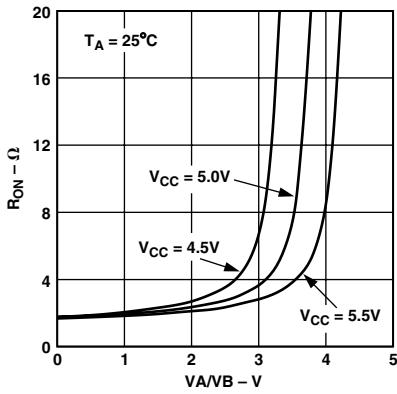
Model	Temperature Range	Package Descriptions	Package Option
ADG3257BRQ	−40°C to +85°C	RQ = 0.15" Quarter Size Outline Package (QSOP)	RQ-16

## CAUTION

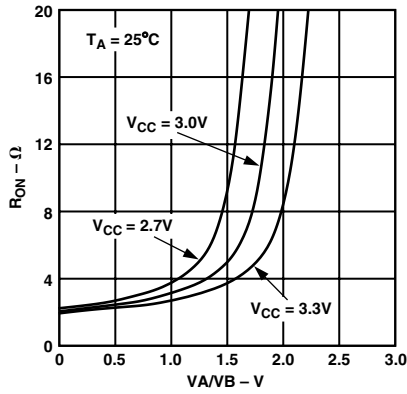
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3257 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



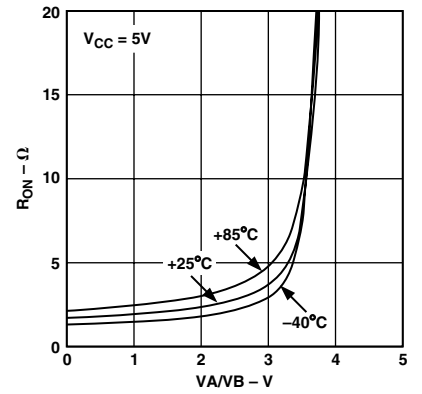
# Typical Performance Characteristics—ADG3257



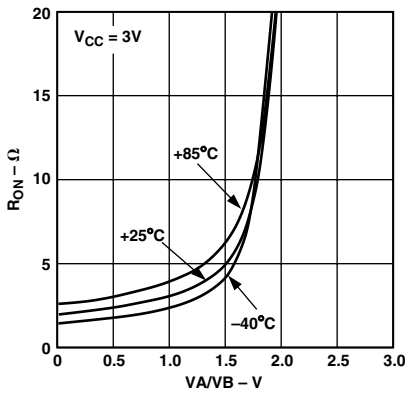
TPC 1. ON Resistance vs. Input Voltage



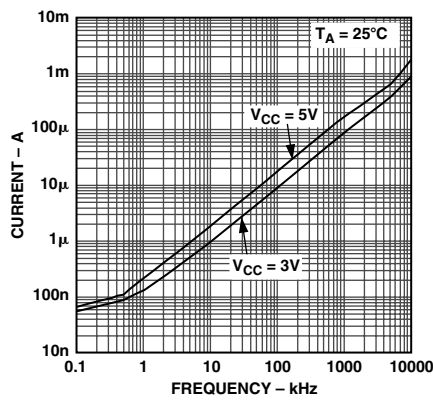
TPC 2. ON Resistance vs. Input Voltage



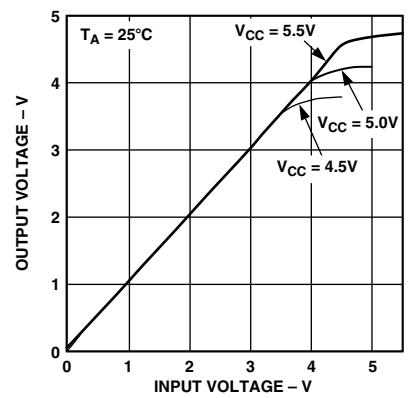
TPC 3. ON Resistance vs. Input Voltage for Different Temperatures



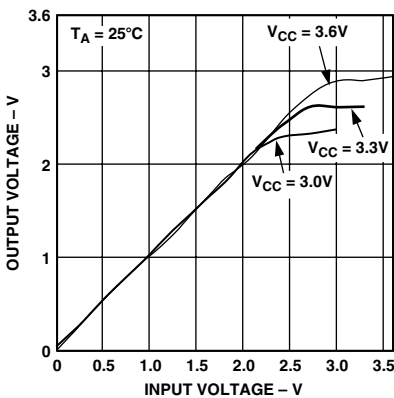
TPC 4. ON Resistance vs. Input Voltage for Different Temperatures



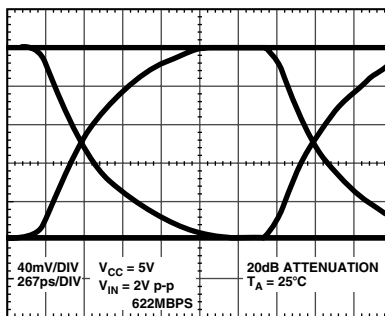
TPC 5.  $I_{CC}$  vs. Enable Frequency



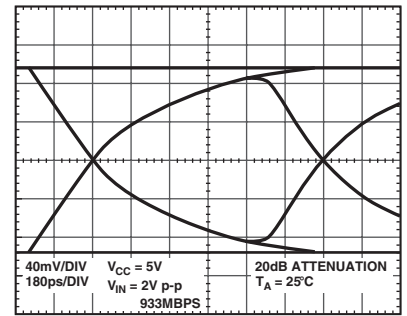
TPC 6. Max Pass Voltage



TPC 7. Max Pass Voltage

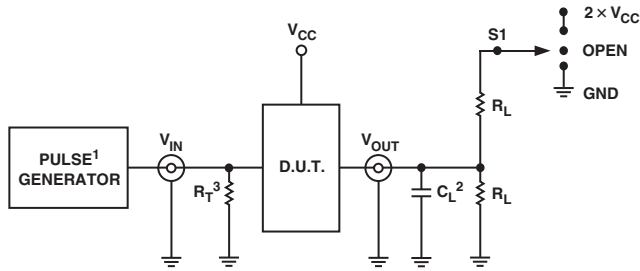


TPC 8. 622 Mbps Eye Diagram



TPC 9. 933 Mbps Eye Diagram

# ADG3257



**NOTES**  
<sup>1</sup>PULSE GENERATOR FOR ALL PULSES:  $t_F < 2.5\text{ns}$ ,  $t_R < 2.5\text{ns}$ .  
<sup>2</sup> $C_L$  = INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES.  
<sup>3</sup> $R_T$  IS THE TERMINATION RESISTOR; SHOULD BE EQUAL TO  $Z_{OUT}$  OF THE PULSE GENERATOR.

Figure 1. Load Circuit

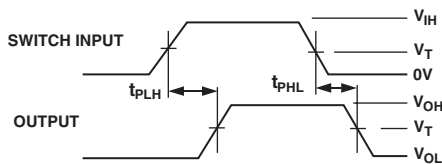


Figure 2. Propagation Delay

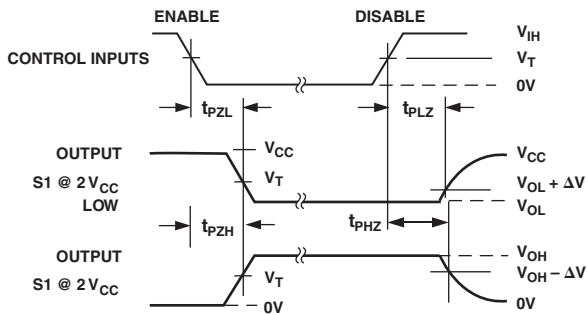


Figure 3. Select, Enable, and Disable Times

Table II. Switch S1 Condition

Test	S1
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}$ , $t_{PZH}$	GND
$t_{SEL}$	OPEN

Table III. Test Conditions

Symbol	$V_{CC} = 5\text{ V} \pm 10\%$	$V_{CC} = 3.3\text{ V} \pm 10\%$	Unit
$R_L$	500	500	$\Omega$
$V_{\Delta}$	300	300	mV
$C_L$	50	50	pF

## APPLICATIONS

### Mixed Voltage Operation, Level Translation

Bus switches can be used to provide a solution for mixed voltage systems where interfacing bidirectionally between 5 V and 3 V devices is required. To interface between 5 V and 3.3 V buses, an external diode is placed in series with the 5 V power supply as shown in Figure 4.

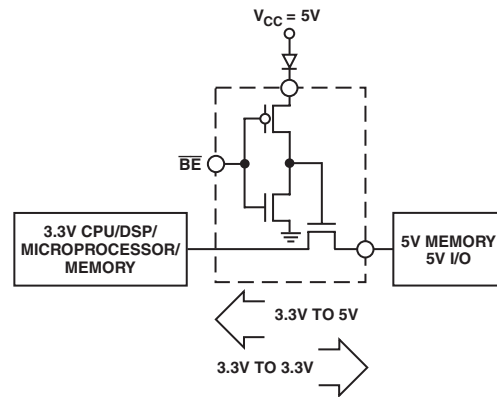


Figure 4. Level Translation Between 5 V and 3.3 V Devices

The diode drops the internal gate voltage down to 4.3 V. The bus switch limits the voltage present on the output to  $V_{CC} - \text{external diode drop} = V_{TH}$ .

Therefore, assuming a diode drop of 0.7 V and a  $V_{TH}$  of 1 V, the output voltage would be limited to 3.3 V with a logic high.

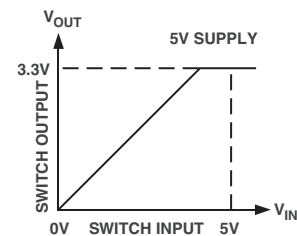


Figure 5. Input Voltage to Output Voltage

Similarly, the device could be used to translate bidirectionally between 3.3 V to 2.5 V systems. In this case, there is no need for an external diode. The internal  $V_{TH}$  drop is 1 V, so with a  $V_{CC} = 3.3\text{ V}$  the bus switch will limit the output voltage to  $V_{CC} - 1\text{ V} = 2.3\text{ V}$ .

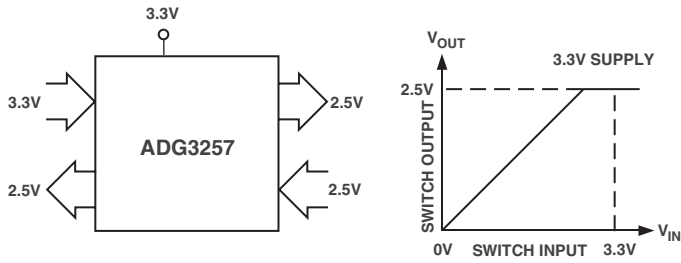


Figure 6. 3.3 V to 2.5 V Level Translation Using the ADG3257 Bus Switch

### Memory Switching

This quad bus switch may be used to allow switching between different memory banks, thus allowing additional memory and decreasing capacitive loading. Figure 7 illustrates the ADG3257 in such an application.

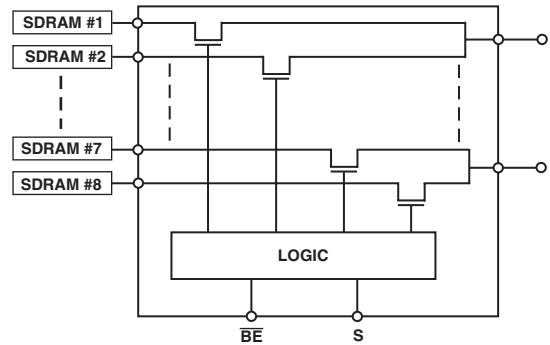
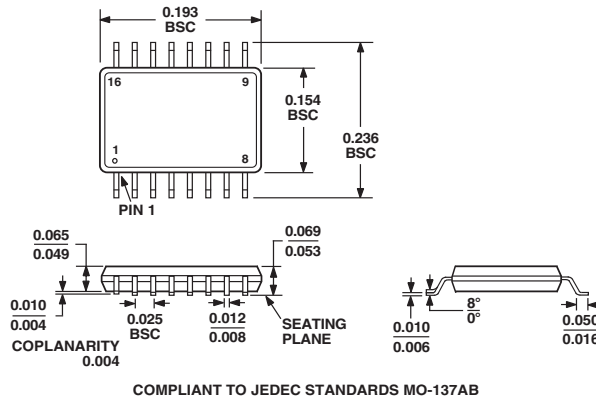


Figure 7. Allows Additional Memory Modules without Added Drive or Delay

OUTLINE DIMENSIONS

16-Lead Shrink Small Outline Package [QSOP]  
(RQ-16)

Dimensions shown in inches



C02914-0-4/03(C)

Revision History

Location	Page
4/03—Data Sheet changed from REV. B to REV. C. Updated Publication Code	8
4/03—Data Sheet changed from REV. A to REV. B. Updated OUTLINE DIMENSIONS	8
06/02—Data Sheet changed from REV. 0 to REV. A. Edits to FEATURES	1