



Quad SPDT Switch

ADG333A

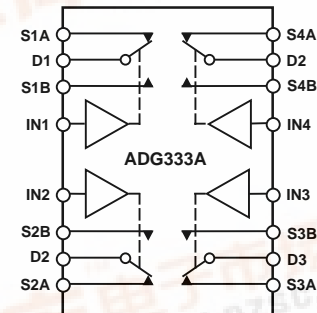
FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (45 Ω max)
- Low ΔR_{ON} (5 Ω max)
- Low R_{ON} Match (4 Ω max)
- Low Power Dissipation
- Fast Switching Times
 - $t_{ON} < 175$ ns
 - $t_{OFF} < 145$ ns
- Low Leakage Currents (5 nA max)
- Low Charge Injection (10 pC max)
- Break-Before-Make Switching Action

APPLICATIONS

- Audio and Video Switching
- Battery Powered Systems
- Test Equipment
- Communication Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG333A is a monolithic CMOS device comprising four independently selectable SPDT switches. It is designed on an LC²MOS process which provides low power dissipation yet achieves a high switching speed and a low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable, battery powered instruments.

When they are ON, each switch conducts equally well in both directions and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
The ADG333A is fabricated on an enhanced LC²MOS process, giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
For applications where the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The part is fully specified with a single +12 V supply.

REV. 0

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ADG333A—SPECIFICATIONS¹

DUAL SUPPLY ($V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	+25°C	-40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analogue Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	20 45	45	Ω typ Ω max	$V_D = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
ΔR_{ON}		5	Ω max	$V_D = \pm 5\text{ V}$, $I_S = -10\text{ mA}$
R_{ON} Match		4	Ω max	$V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.1 ± 0.25	± 3	nA typ nA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$ Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.1 ± 0.4	± 5	nA typ nA max	$V_S = V_D = \pm 15.5\text{ V}$ Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}		± 0.005 ± 0.5	μA typ μA max	$V_{IN} = 0\text{ V}$ or V_{DD}
DYNAMIC CHARACTERISTICS²				
t_{ON}	90	175	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
t_{OFF}	80	145	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 5
Charge Injection	2		pC typ	$V_D = 0\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$;
	10		pC max	$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$; Test Circuit 6
OFF Isolation	72		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				$V_S = 2.3\text{ V rms}$, Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				$V_S = 2.3\text{ V rms}$, Test Circuit 8
C_S (OFF)	5		pF typ	
C_D , C_S (ON)	20		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05 0.25	0.35	mA typ mA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.01 1	5	μA typ μA max	
V_{DD}/V_{SS}		$\pm 3/\pm 20$	V min/V max	$ V_{DD} = V_{SS} $

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY ($V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	+25°C	-40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH Analog Signal Range R_{ON}	35	0 to V_{DD} 75	V Ω typ Ω max	$V_D = +1\text{ V}$, $+10\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS Source OFF Leakage I_S (OFF) Channel ON Leakage I_D , I_S (ON)	± 0.1 ± 0.25 ± 0.1 ± 0.4	± 3 ± 5	nA typ nA max nA typ nA max	$V_{DD} = +13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$ Test Circuit 2 $V_S = V_D = 12.2\text{ V}/1\text{ V}$ Test Circuit 3
DIGITAL INPUTS Input High Voltage, V_{INH} Input Low Voltage, V_{INL} Input Current I_{INL} or I_{INH}		2.4 0.8 ± 0.005 ± 0.5	V min V max μA typ μA max	$V_{IN} = 0\text{ V}$ or V_{DD}
DYNAMIC CHARACTERISTICS ² t_{ON} t_{OFF} Break-Before-Make Delay, t_{OPEN} Charge Injection OFF Isolation Channel-to-Channel Crosstalk C_S (OFF) C_D , C_S (ON)	110 100 10 5 72 85 5 20	200 180	ns typ ns max ns typ ns max ns min ns min pC typ dB typ dB typ pF typ pF typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4 $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4 $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 5 $V_D = 6\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$; $V_{DD} = +12\text{ V}$, $V_{SS} = -0\text{ V}$; Test Circuit 6 $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 1.15\text{ V rms}$, Test Circuit 7 $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 1.15\text{ V rms}$, Test Circuit 8
POWER REQUIREMENTS I_{DD} V_{DD}	0.05 0.25	0.35 +3/+30	mA typ mA max V min/V max	$V_{DD} = +13.5\text{ V}$ Digital Inputs = 0 V or 5 V

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.²Guaranteed by design, not subject to production test.

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ADG333A

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+44 V
V _{DD} to GND	-0.3 V to +30 V
V _{SS} to GND	+0.3 V to -30 V
Analog, Digital Inputs ²	V _{SS} - 2 V to V _{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D	20 mA
Peak Current, S or D	40 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Junction Temperature	+150°C
Plastic Package	
θ _{JA} , Thermal Impedance	103°C/W
Lead Temperature, Soldering (10 sec)	+260°C

SOIC Package

θ _{JA} , Thermal Impedance	74°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

SSOP Package

θ _{JA} , Thermal Impedance	130°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG333A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG333ABN	-40°C to +85°C	N-20
ADG333ABR	-40°C to +85°C	R-20
ADG333ABRS	-40°C to +85°C	RS-20

*N = Plastic DIP, R = Small Outline IC (SOIC). RS = Shrink Small Outline Package (SSOP).

Table I. Truth Table

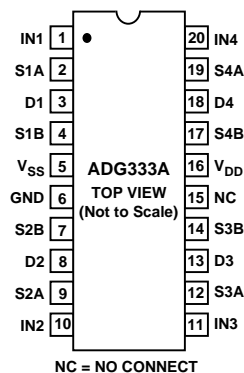
Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

TERMINOLOGY

<p>S Source Terminal. May be an input or output.</p> <p>D Drain Terminal. May be an input or output.</p> <p>IN Logic Control Input.</p> <p>R_{ON} Ohmic resistance between D and S.</p> <p>ΔR_{ON} R_{ON} variation due to a change in the analog input voltage with a constant load current.</p> <p>R_{ON} Match Difference between the R_{ON} of any two channels.</p> <p>I_S (OFF) Source leakage current with the switch “OFF.”</p> <p>I_D (OFF) Drain leakage current with the switch “OFF.”</p> <p>I_D, I_S (ON) Channel leakage current with the switch “ON.”</p> <p>V_D (V_S) Analog voltage on terminals D, S.</p> <p>C_S (OFF) “OFF” Switch Source Capacitance.</p> <p>C_D (OFF) “OFF” Switch Drain Capacitance.</p>	<p>C_D, C_S (ON) “ON” Switch Capacitance.</p> <p>t_{ON} Delay between applying the digital control input and the output switching on.</p> <p>t_{OFF} Delay between applying the digital control input and the output switching off.</p> <p>t_{OPEN} Break Before Make delay when switches are configured as a multiplexer.</p> <p>V_{INL} Maximum input voltage for logic “0.”</p> <p>V_{INH} Minimum input voltage for logic “1.”</p> <p>I_{INL} (I_{INH}) Input current of the digital input.</p> <p>Crosstalk A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.</p> <p>Off Isolation A measure of unwanted signal coupling through an “OFF” switch.</p> <p>Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching.</p>
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PIN CONFIGURATION

DIP/SOIC/SSOP



ADG333A—Typical Performance Graphs

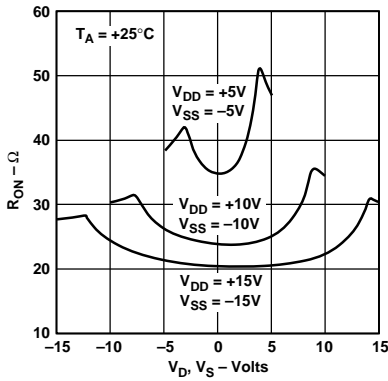


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply

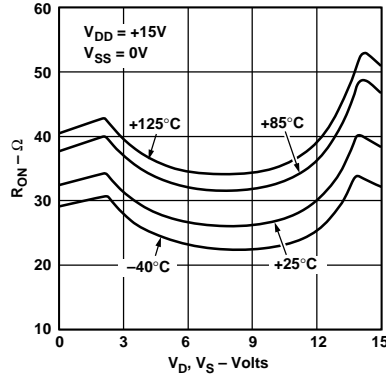


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Single Supply

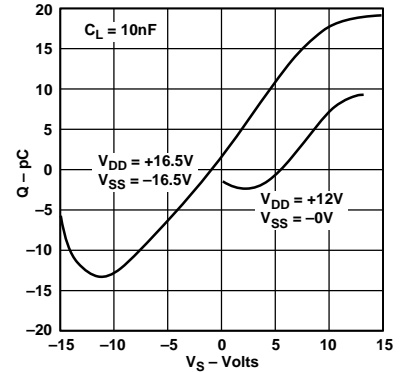


Figure 7. Charge Injection as a Function of V_S

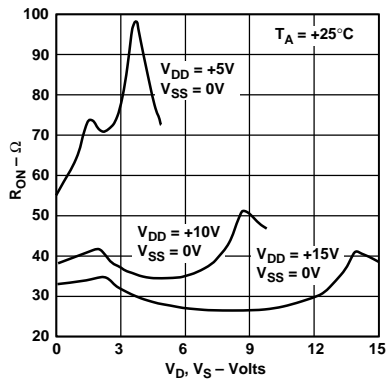


Figure 2. R_{ON} as a Function of V_D (V_S): Single Power Supply

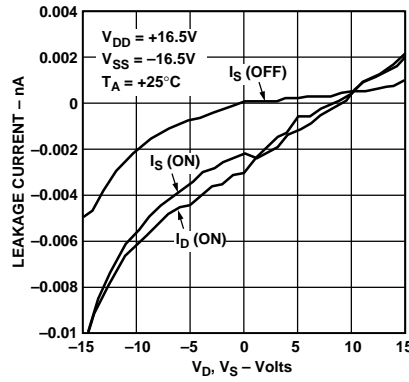


Figure 5. Leakage Currents as a Function of V_D (V_S): Dual Supply

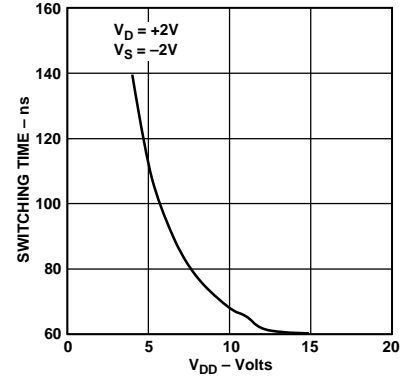


Figure 8. Switching Time as a Function of V_{DD}

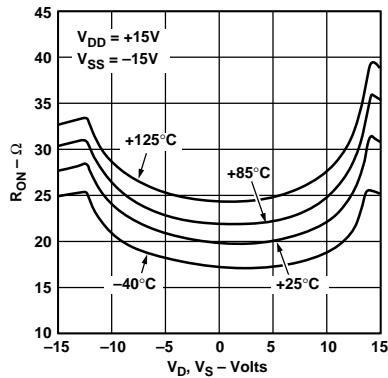


Figure 3. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Dual Supply

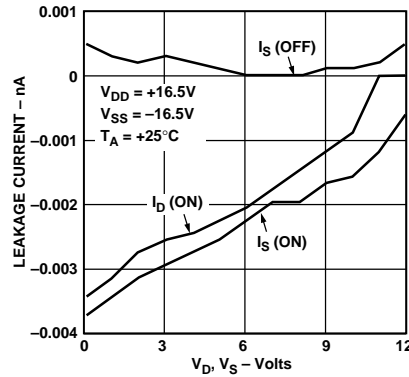


Figure 6. Leakage Currents as a Function of V_D (V_S): Single Supply

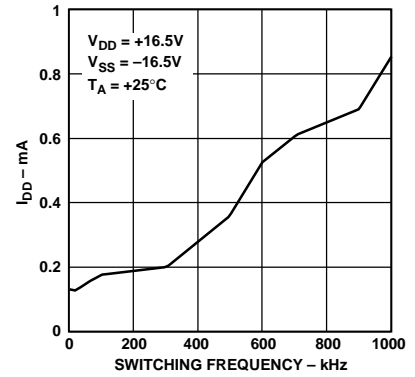
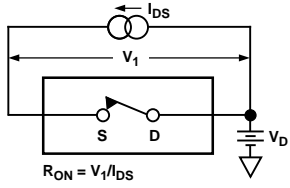
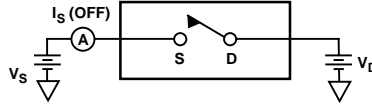


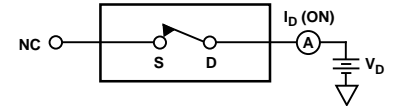
Figure 9. I_{DD} as a Function of Switching Frequency



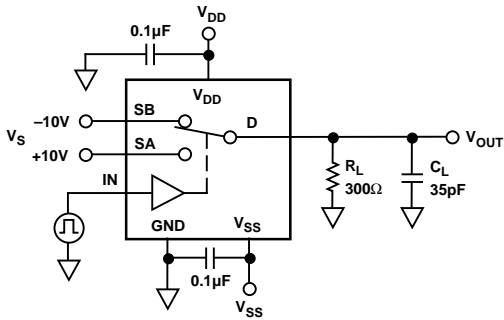
Test Circuit 1. On Resistance



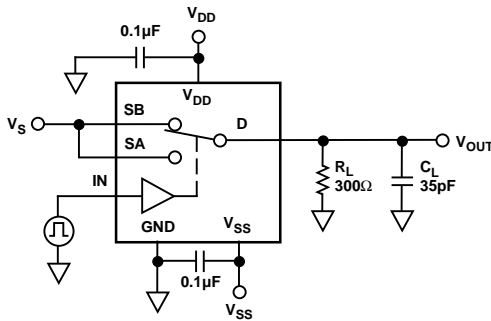
Test Circuit 2. Off Leakage



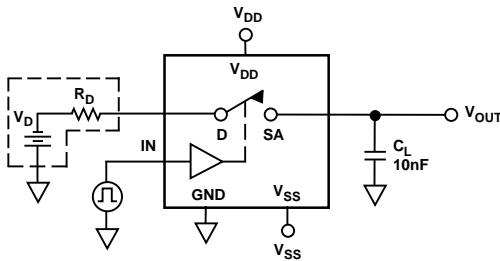
Test Circuit 3. On Leakage



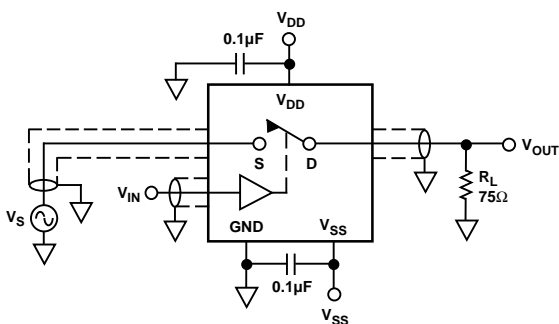
Test Circuit 4. Switching Times



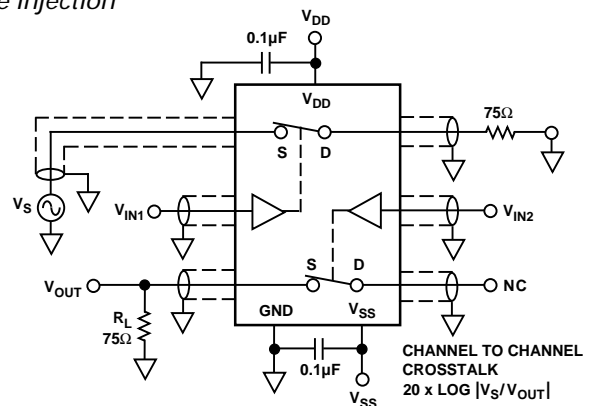
Test Circuit 5. Break-Before-Make Delay, t_{OPEN}



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

