Low Cost µP Supervisory Circuits

ADM705/ADM706/ADM707/ADM708

FEATURES

Guaranteed RESET valid with V_{CC} = 1 V
190 µA quiescent current
Precision supply-voltage monitor
4.65 V (ADM705/ADM707)
4.40 V (ADM706/ADM708)
200 ms reset pulse width
Debounced TTL/CMOS manual reset input ($\overline{MR}$)
Independent watchdog timer
1.6 sec timeout (ADM705/ADM706)
Active-high reset output (ADM707/ADM708)
Voltage monitor for power-fail or low battery warning
Superior upgrade for MAX705–MAX708

APPLICATIONS

Microprocessor systems
Computers
Controllers
Intelligent instruments
Critical µP monitoring
Automotive systems
Critical µP power monitoring

FUNCTIONAL BLOCK DIAGRAMS

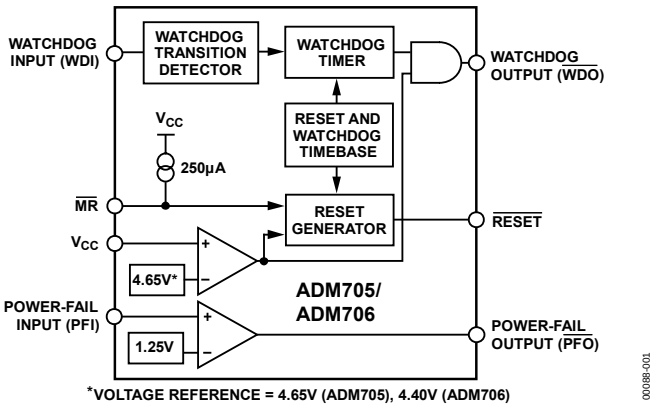

Figure 1.

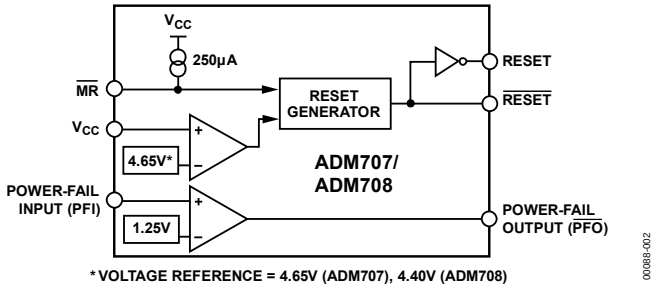

Figure 2.

GENERAL DESCRIPTION

The ADM705/ADM706/ADM707/ADM708 are low cost µP supervisory circuits. They are suitable for monitoring the 5 V power supply/battery and can also monitor microprocessor activity.

The ADM705/ADM706 provide the following functions:

- Power-on reset output during power-up, power-down, and brownout conditions. The $\overline{RESET}$ output remains operational with V_{CC} as low as 1 V.
- Independent watchdog timeout, $\overline{WDO}$, that goes low if the watchdog input has not been toggled within 1.6 seconds.
- A 1.25 V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 5 V.
- An active-low debounced manual reset input ($\overline{MR}$).

The ADM707/ADM708 differ in that:

- A watchdog timer function is not available.
- An active-high reset output in addition to the active-low output is available.

Two supply-voltage monitor levels are available. The ADM705/ADM707 generate a reset when the supply voltage falls below 4.65 V, while the ADM706/ADM708 require that the supply fall below 4.40 V before a reset is issued.

All parts are available in 8-lead DIP and SOIC packages.

Rev. D

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REVISION HISTORY

11/05—Rev. C to Rev. D

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8/02—Rev. B to Rev. C

Removed RM-8 (µSOIC) Package ..... Universal
Updated N-8 and R-8 Packages 8

SPECIFICATIONS

V_{CC} = 4.75 V to 5.5 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		190	250	µA	
Reset Threshold	4.5	4.65	4.75	V	ADM705, ADM707
	4.25	4.40	4.50	V	ADM706, ADM708
Reset Threshold Hysteresis		40		mV	
Reset Pulse Width	160	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA
			0.3	V	V_{CC} = 1 V, I_{SINK} = 50 µA
			0.3	V	V_{CC} = 1.2 V, I_{SINK} = 100 µA
RESET Output Voltage	V_{CC} – 1.5			V	ADM707, ADM708, I_{SOURCE} = 800 µA
			0.4	V	ADM707, ADM708, I_{SINK} = 1.2 mA
Watchdog Timeout Period (t_{WD})	1.00	1.60	2.25	sec	V_{IL} = 0.4 V, $V_{IH} = V_{CC} \times 0.8$ WDI = V_{CC}
WDI Pulse Width (t_{WP})	50			ns	
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		50	150	µA	WDI = 0 V
	–150	–50		µA	WDI = 0 V
$\overline{\text{WDO}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 1.2 mA
$\overline{\text{MR}}$ Pull-Up Current	100	250	600	µA	$\overline{\text{MR}}$ = 0 V
$\overline{\text{MR}}$ Pulse Width	150			ns	
$\overline{\text{MR}}$ Input Threshold			0.8	V	
	2.0			V	
$\overline{\text{MR}}$ to Reset Output Delay			250	ns	
PFI Input Threshold	1.2	1.25	1.3	V	
PFI Input Current	–25	+0.01	+25	nA	
PFO Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
All Other Inputs	−0.3 V to V_{CC} + 0.3 V
Input Current	
V_{CC}	20 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, N-8 PDIP	727 mW
θ_{JA} Thermal Impedance	135°C/W
Power Dissipation, R-8 SOIC	470 mW
θ_{JA} Thermal Impedance	110°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	−65°C to +150°C
ESD Rating	>5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

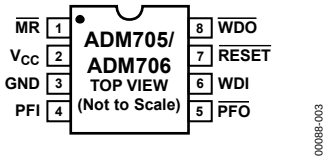


Figure 3.ADM705/ADM706 Pin Configuration

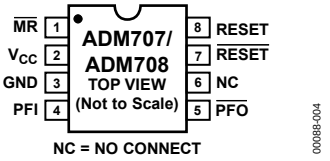


Figure 4.ADM707/ADM708 Pin Configuration

Table 3. Pin Function Descriptions

	Pin Number		
	ADM705 ADM706	ADM707 ADM708	
Mnemonic	PDIP, SOIC	PDIP, SOIC	Function
$\overline{MR}$	1	1	Manual Reset Input. When taken below 0.8 V, a RESET is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch as it is internally debounced. An internal 250 µA pull-up current holds the input high when floating.
V_{CC}	2	2	5 V Power Supply Input.
GND	3	3	0 V Ground Reference for All Signals.
PFI	4	4	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI should be connected to GND or V_{CC}.
$\overline{PFO}$	5	5	Power-Fail Output. $\overline{PFO}$ is the output from the power-fail comparator. It goes low when PFI is less than 1.25 V.
WDI	6	–	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output $\overline{WDO}$ goes low. The timer resets with each transition at the WDI input. Either a high-to-low or a low-to-high transition clears the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	–	6	No Connect.
$\overline{RESET}$	7	7	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It can be triggered either by V_{CC} being below the reset threshold or by a low signal on the manual reset ($\overline{MR}$) input. $\overline{RESET}$ remains low whenever V_{CC} is below the reset threshold (4.65 V in ADM705, 4.4 V in ADM706). It remains low for 200 ms after V_{CC} goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	8	–	Watchdog Output. $\overline{WDO}$ remains low until the watchdog timer is cleared. $\overline{WDO}$ also goes low during low line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ goes low if the internal $\overline{WDO}$ remains low. As soon as V_{CC} goes above the reset threshold, $\overline{WDO}$ goes high immediately.
RESET	–	8	Logic Output. RESET is an active-high output suitable for systems that use active-high RESET logic. It is the inverse of $\overline{RESET}$.

TYPICAL PERFORMANCE CHARACTERISTICS

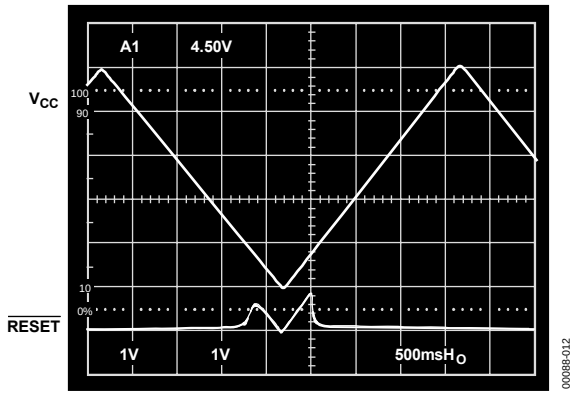


Figure 5. $\overline{RESET}$ Output Voltage vs. Supply Voltage

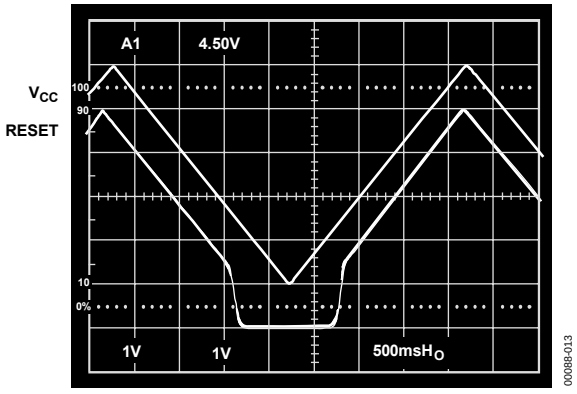


Figure 6. ADM707/ADM708 RESET Output Voltage vs. Supply Voltage

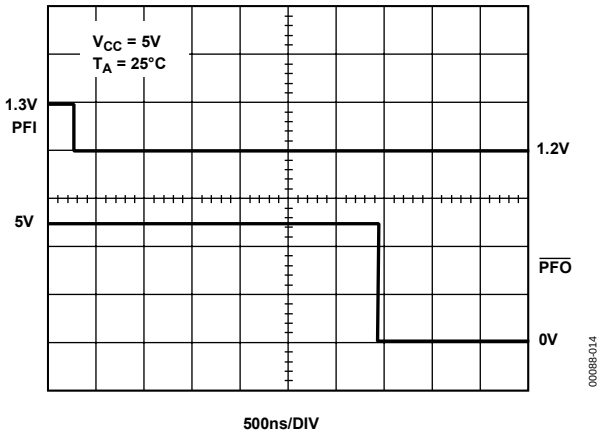


Figure 7. PFI Comparator Assertion Response Time

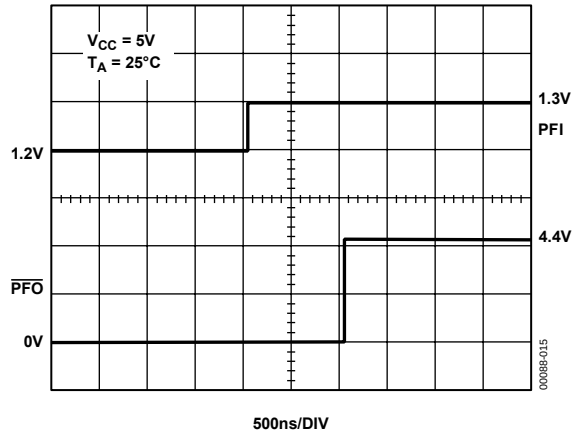


Figure 8. PFI Comparator Deassertion Response Time

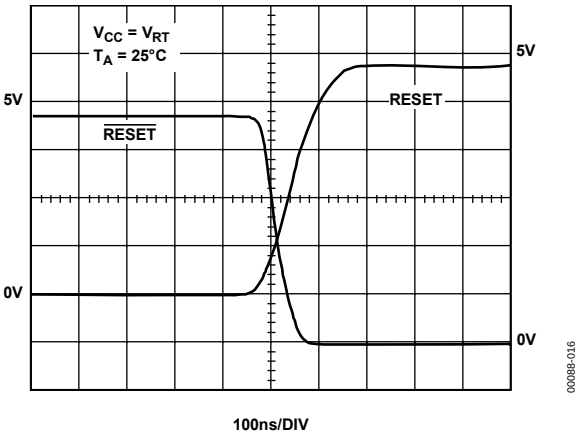


Figure 9. $\overline{RESET}$, RESET Assertion

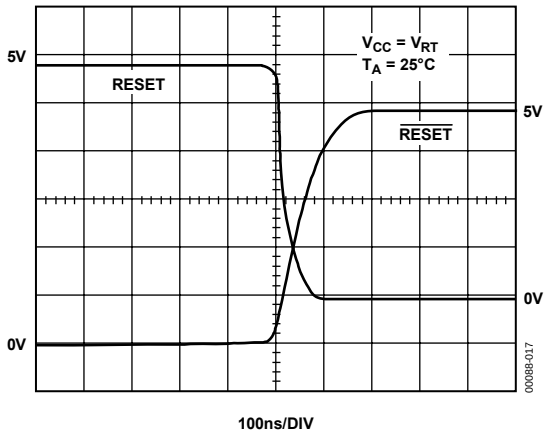


Figure 10. $\overline{RESET}$, RESET Deassertion

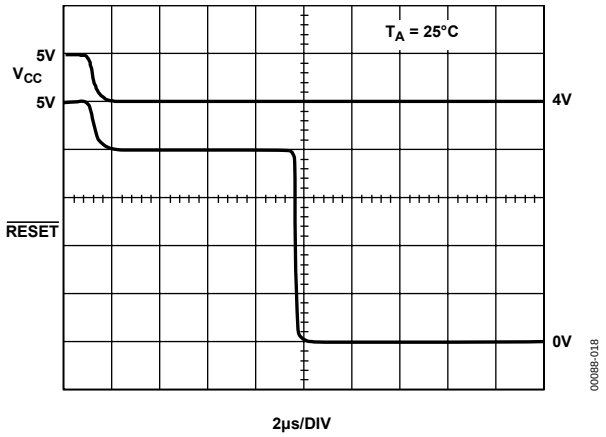


Figure 11. ADM705/ADM707 $\overline{RESET}$ Response Time

CIRCUIT INFORMATION

POWER-FAIL $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active-low output that provides a RESET signal to the microprocessor whenever the V_{CC} input is below the reset threshold. An internal timer holds RESET low for 200 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on RESET signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. The $\overline{\text{RESET}}$ output is guaranteed to remain valid (low) with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply voltage ramps up.

In addition to $\overline{\text{RESET}}$, an active-high RESET output is also available on the ADM707/ADM708. This is the complement of $\overline{\text{RESET}}$ and is useful for processors requiring an active-high RESET signal.

MANUAL RESET (ADM707/ADM708)

The manual reset input ($\overline{\text{MR}}$) allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The $\overline{\text{MR}}$ input is TTL/CMOS compatible, so it may also be driven by any logic reset output.

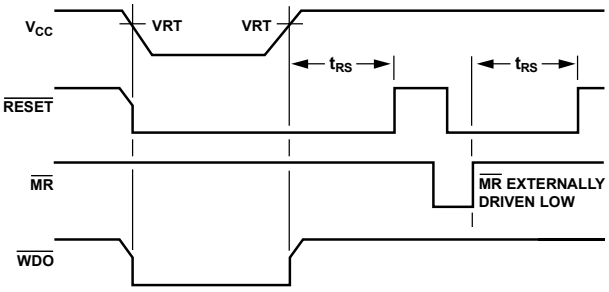


Figure 12. $\overline{\text{RESET}}$, $\overline{\text{MR}}$, and $\overline{\text{WDO}}$ Timing

WATCHDOG TIMER (ADM705/ADM706)

The watchdog timer circuit may be used to monitor the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.6 sec), then the watchdog output ($\overline{\text{WDO}}$) goes low. The $\overline{\text{WDO}}$ may be connected to a nonmaskable interrupt (NMI) on the processor; therefore, if the watchdog timer times out, then an interrupt is generated. The interrupt service routine should then be used to rectify the problem.

If a $\overline{\text{RESET}}$ signal is required when a timeout occurs, then the $\overline{\text{WDO}}$ should be connected to the manual reset input ($\overline{\text{MR}}$).

The watchdog timer is cleared by either a high-to-low or by a low-to-high transition on WDI. It is also cleared by $\overline{\text{RESET}}$ going low; therefore, the watchdog timeout period begins after $\overline{\text{RESET}}$ goes high.

When V_{CC} falls below the reset threshold, $\overline{\text{WDO}}$ is forced low whether or not the watchdog timer has timed out. Normally, this would generate an interrupt, but it is overridden by $\overline{\text{RESET}}$ going low.

The watchdog monitor can be deactivated by floating the watchdog input (WDI). The $\overline{\text{WDO}}$ can now be used as a low line output because it only goes low when V_{CC} falls below the reset threshold.

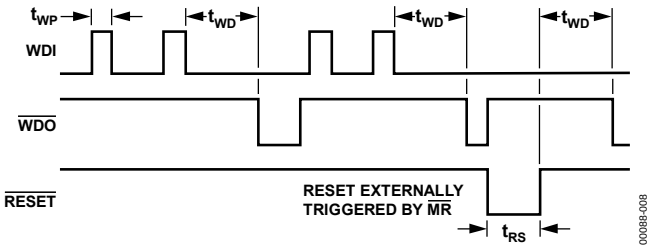


Figure 13. Watchdog Timing

POWER-FAIL COMPARATOR

The power-fail comparator is an independent comparator that may be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ($\overline{\text{PFO}}$) goes low, indicating a power failure. For early warning of power failure, the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The $\overline{\text{PFO}}$ output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

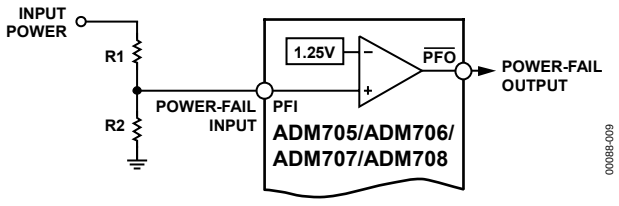


Figure 14. Power-Fail Comparator

Adding Hysteresis to the Power-Fail Comparator

For increased noise immunity, hysteresis may be added to the power-fail comparator. Because the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 15. When $\overline{PFO}$ is low, Resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.

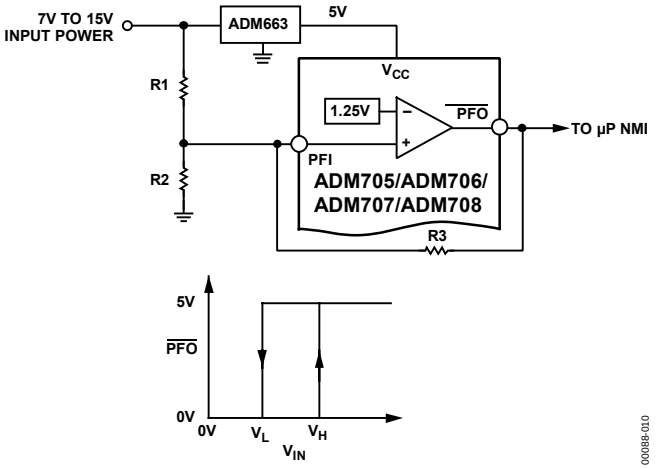


Figure 15. Adding Hysteresis to the Power-Fail Comparator

$$V_H = 1.25\left[1 + \left(\frac{R2 + R3}{R2 \times R3}\right)R1\right]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{RE}\right)$$

$$V_{MID} = 1.25\left(\frac{R1 + R2}{R2}\right)$$

VALID RESET BELOW 1 V V_{CC}

The ADM705/ADM706/ADM707/ADM708 are guaranteed to provide a valid reset level with V_{CC} as low as 1 V; please refer to the Typical Performance Characteristics section. As V_{CC} drops below 1 V, the internal transistor does not have sufficient drive to hold it on so the voltage on $\overline{RESET}$ is no longer held at 0 V. A pull-down resistor as shown in Figure 16 may be connected externally to hold the line low if required.

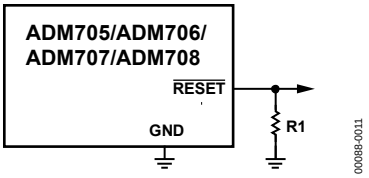


Figure 16. $\overline{RESET}$ Valid Below 1 V

APPLICATIONS

A typical operating circuit is shown in Figure 17. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistors R1 and R2 should be selected so that when the supply voltage drops below the desired level (e.g., 8 V), the voltage on PFI drops below the 1.25 V threshold thereby generating an interrupt to the µP. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

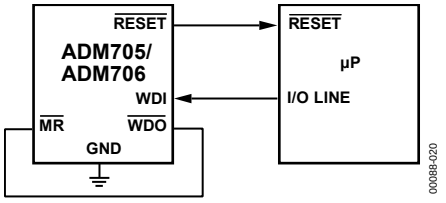


Figure 17. Typical Application Circuit

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines should toggle this line at least once every 1.6 seconds. If a problem occurs and this line is not toggled, $\overline{\text{WDO}}$ goes low and a nonmaskable interrupt is generated. This interrupt routine may be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, the $\overline{\text{WDO}}$ output should be connected to the $\overline{\text{MR}}$ input as shown in Figure 18.

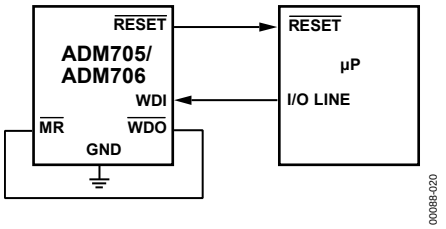


Figure 18. $\overline{\text{RESET}}$ from WDO

MONITORING ADDITIONAL SUPPLY LEVELS

It is possible to use the power-fail comparator to monitor a second supply as shown in Figure 19. The two sensing resistors, R1 and R2, are selected so that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The $\overline{\text{PFO}}$ output may be connected to the $\overline{\text{MR}}$ input so that a RESET is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, then a $\overline{\text{RESET}}$ is generated.

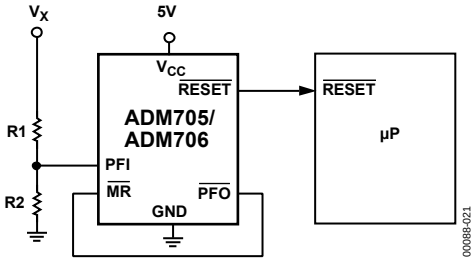


Figure 19. Monitoring 5 V and an Additional Supply, V_X

µPS WITH BIDIRECTIONAL RESET

In order to prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM70x $\overline{\text{RESET}}$ output pin and the µP reset pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, it should be buffered as shown in Figure 20.

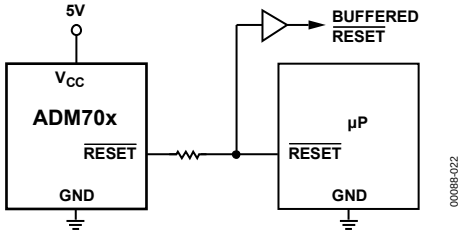
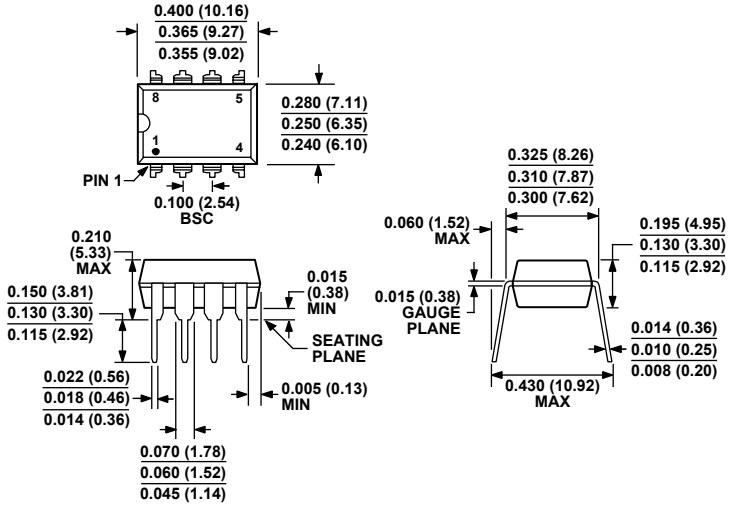


Figure 20. Bidirectional I-O $\overline{\text{RESET}}$

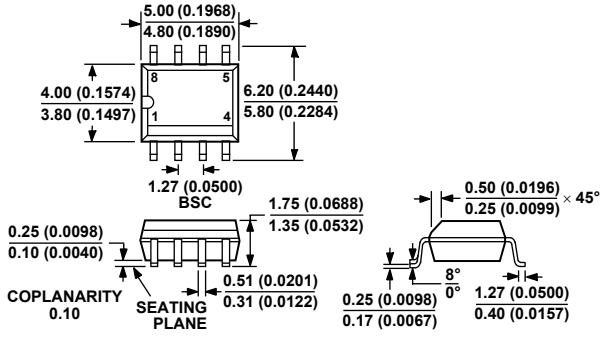
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 21. 8-Lead Plastic Dual-in-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 8-Lead Small Outline Package [SOIC]
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM705AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM705AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM705AR–REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM705AR–REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM705ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM705ARZ–REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM705ARZ–REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM706ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM706AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM706ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM707AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM707ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM707AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM707AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM707ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM707ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM708AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM708ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM708AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM708AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM708ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8
ADM708ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC]	R-8

[1] Z = Pb-free part.