Low-Power, Synchronous Voltage-to-Frequency Converter

FEATURES

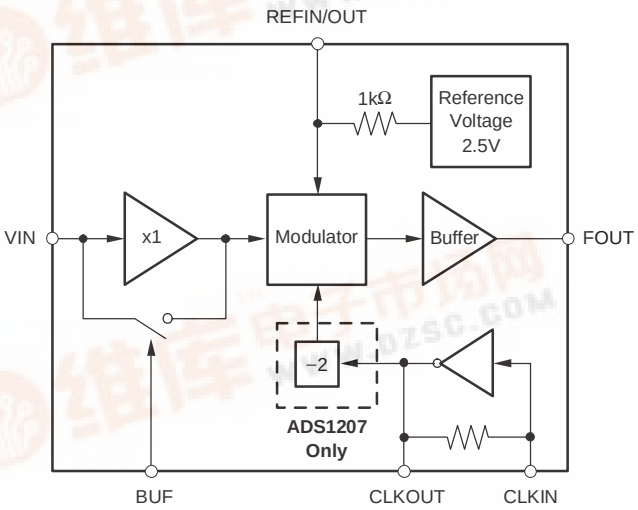
- Syncronous Operation
- Frequency Set By External Clock
- Maximum Input Frequency:
  - 1MHz for ADS1206
  - 4MHz for ADS1207
- Selectable High-Impedance Buffered Input
- 2% Internal, 2.5V Reference Voltage
- High-Current Output Driver
- Power Supply 3.3V or 5V
- Low Power : 3mW (typ)
- Alternate Source for AD7740
- −40°C to +85°C Operating Temperature Range

APPLICATIONS

- Galvanic Isolation Measurement
- High Voltage Measurement
- Low-Cost Analog-to-Digital Conversion
- Motor Control
- Industrial Process Control
- Instrumentation
- Smart Transmitters
- Portable Instruments

DESCRIPTION

The ADS1206 and ADS1207 are a low-cost, high-performance, synchronous voltage-to-frequency converters (VFC). Both devices can operate from a single 3.0V to 3.6V or 4.5V to 5.5V power supply, consuming only 1mA. The output signal is synchronous with the input clock, CLKIN. The clock input is TTL- and CMOS-compatible and the onboard clock generator can also accept an external crystal or resonator. The maximum input clock frequency for the ADS1206 is 1MHz and for the ADS1207 is 4MHz. The clock divider on the ADS1207 scales the input frequency to 2MHZ, which permits the core to operate at the higher rate. The high-impedance input is ideal for direct connection to high-impedance transducers or high-voltage resistive dividers. Counting output pulses over a 4ms period results in an effective 12-bit resolution for the ADS1206 using a 1MHz input clock. For the ADS1207 using a 4MHz input clock, the same result occurs over a 2ms period. Both devices are designed for use in medium-resolution measurements. They are available in an 8-lead VSSOP package.



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (%FS)	MAXIMUM GAIN ERROR (%)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1206	±0.012	±0.7	VSSOP-8	DGK	−40°C to +85°C	TBD	ADS1206IDGKT	Tape and Reel, 250
						TBD	ADS1206IDGKR	Tape and Reel, 2000
ADS1207	±0.012	±0.7	VSSOP-8	DGK	−40°C to +85°C	TBD	ADS1207IDGKT	Tape and Reel, 250
						TBD	ADS1207IDGKR	Tape and Reel, 2000

(1) For the most current package and ordering information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1204	UNIT
Supply Voltage, GND to V_{DD}	−0.3 to 7	V
Analog Input Voltage with Respect to GND	GND − 0.3 to V_{DD} + 0.3	V
Reference Input Voltage with Respect to GND	GND − 0.3 to V_{DD} + 0.3	V
Digital Input Voltage with Respect to GND	GND − 0.3 to V_{DD} + 0.3	V
Input Current to Any Pin Except Supply	−20 to 20	mA
Power Dissipation	See Dissipation Rating Table	
Operating Virtual Junction Temperature Range, T_J	−40 to +150	°C
Operating Free-Air Temperature Range, T_A	−40 to +85	°C
Storage Temperature Range, T_{STG}	−65 to +150	°C
Lead Temperature (1.6mm or 1/16-inch from case for 10s)	+260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply Voltage, GND to V_{DD}	Low-Voltage Levels	3.0		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Reference Input Voltage		TBD	2.5	V_{DD}	V
Analog Inputs	BUF = 0	0		V_{REF}	V
	BUF = 1	0.1		V_{DD} − 0.2	V
External Clock	ADS1206	TBD		1	MHz
	ADS1207	TBD		4	MHz
Operating Junction Temperature Range, T_J		−40		105	°C

(1) with reduced accuracy, minimum clock can go up to 500kHz.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
Low-K(2)	DGK	469.6mW	3.756mW/°C	300.5mW	244.2mW
High-K(3)	DGK	691.4mW	5.531mW/°C	442.5mW	359.5mW

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at −40°C to +85°C, V_{DD} = 5V or V_{DD} = 3V, V_{REF} = internal +2.5V, CLKIN = 1MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1206I, ADS1207I MIN	TYP(1)	MAX	UNITS
DC Accuracy						
INL	Integral linearity error(2)	BUF = 1			±0.012	% FSR
		BUF = 0			±0.018	% FSR
DNL	Differential nonlinearity(3)				TBD	% FSR
V_{OS}	Offset error	BUF = 0, VIN = 0V		±7	±35	mV
		BUF = 1, VIN = 0.1V		±7	±35	mV
TCV_{OS}	Offset error drift			5	20	µV/°C
G_{ERR}	Gain error(4)	Referenced to V_{REF}		±0.1	±0.7	% FSR
TCG_{ERR}	Gain error drift			20		ppm/°C
	Noise			TBD		µVrms
PSRR	Power-supply rejection ratio	4.5V < V_{DD} < 5.5V		55		dB
		3.0V < V_{DD} < 3.6V		65		dB
Analog Input						
FSR	Full-scale range	BUF = 0	0		V_{REF}	V
		BUF = 1	0.1		V_{DD} − 0.2	V
	Input capacitance	BUF = 0		3		pF
		BUF = 1		3		pF
	Input current	BUF = 0		8	10	µA
		BUF = 1		5	100	nA
	Differential input resistance			100		kΩ
	Differential input capacitance			1		pF
BW	Bandwidth	FS sinewave, −3dB, BUF = 0		TBD		MHz
		FS sinewave, −3dB, BUF = 1		TBD		MHz
Output Signal						
FOUT	Output frequency span	ADS1206I	0.1		0.9	CLKIN
		ADS1207I	0.05		0.45	CLKIN
Voltage Reference Output						
V_{OUT}	Reference voltage output		2.3	2.5	2.7	V
	Initial accuracy				±8	%
dV_{OUT}/dT	Output voltage temperature drift			±50		ppm/°C
	Output voltage noise	f = 0.1Hz to 10Hz, C_L = 10µF		100		$µV_{PP}$
		f =10Hz to 10kHz, C_L = 10µF		TBD		µVrms
PSRR	Power-supply rejection ratio	V_{DD} = 4.5V to 5.5V		−70		dB
		V_{DD} = 3.0V to 3.6V		−60		dB
	Reference output resistance			1		kΩ
	Turn-on settling time	to 0.1% at C_L = 0		30		µs
Voltage Reference Input						
V_{REF}	Reference voltage input		TBD	2.5	V_{DD}	V
	Reference input capacitance			5		pF
	Reference input current			±200		µA

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the transfer curve for V_{IN} = 0V to V_{REF} or 0.1V to V_{DD} − 0.2V, expressed either as the number of LSBs or as a percent of measured input range.
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) Applicable for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.
(6) Applicable for 3.0V nominal supply: V_{DD} (min) = 3.0V and V_{DD} (max) = 3.6V.

ELECTRICAL CHARACTERISTICS (continued)

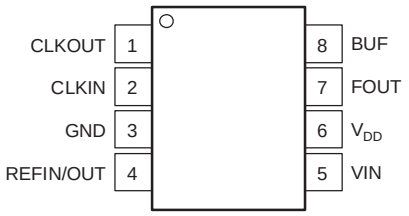
Over recommended operating free-air temperature range at −40°C to +85°C, V_{DD} = 5V or V_{DD} = 3V, V_{REF} = internal +2.5V, CLKIN = 1MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1206I, ADS1207I MIN	TYP(1)	MAX	UNITS
Digital Inputs(5)						
	Logic family			CMOS		
V_{IH}	High-level input voltage		0.7×V_{DD}		V_{DD}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.3×V_{DD}	V
I_{IN}	Input current	V_I = V_{DD} or GND			±1	µA
C_I	Input capacitance			5		pF
Digital Outputs(5)						
	Logic family			CMOS		
V_{OH}	High-level output voltage	V_{DD} = 4.5V, I_{OH} = −100µA	4.44			V
		V_{DD} = 4.5V, I_{OH} = −2mA	2.5			V
V_{OL}	Low-level output voltage	V_{DD} = 4.5V, I_{OH} = 2mA			0.5	V
I_O	Output sink current	1.5V < V_{OL} < V_{DD}		10		mA
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
Digital Inputs(6)						
	Logic family			LVCMOS and LVTTL		
V_{IH}	High-level input Voltage	V_{DD} = 3.6V	2		V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.0V	−0.3		0.8	V
I_{IN}	Input current	V_I = V_{DD} or GND			±1	nA
C_I	Input capacitance			5		pF
Digital Outputs(6)						
	Logic family			LVCMOS and LVTTL		
V_{OH}	High-level output voltage	V_{DD} = 3V, I_{OH} = −100µA	V_{DD}−0.2			V
		V_{DD} = 3V, I_{OH} = −2mA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 3V, I_{OH} = 100µA			0.2	V
		V_{DD} = 3V, I_{OH} = 2mA			0.4	V
I_O	Output sink current			10		mA
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
Power Supply						
V_{DD}	Power-supply voltage	Low-voltage levels	3.0		3.6	V
		5V logic levels	4.5		5.5	V
I_{DD}	Supply current	BUF = GND		0.9	1.25	mA
		BUF = V_{DD}		1.1	1.5	mA
	Power dissipation	V_{DD} = 3.3V		3.63	4.95	mW
		V_{DD} = 5V		5.5	7.5	mW

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the transfer curve for V_{IN} = 0V to V_{REF} or 0.1V to V_{DD} − 0.2V, expressed either as the number of LSBs or as a percent of measured input range.
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) Applicable for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.
(6) Applicable for 3.0V nominal supply: V_{DD} (min) = 3.0V and V_{DD} (max) = 3.6V.

PIN ASSIGNMENTS

VSSOP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	NO.	DESCRIPTION
CLKOUT	1	Clock output
CLKIN	2	Master clock input
GND	3	Ground
REFIN/OUT	4	Reference voltage input or output
VIN	5	Analog input
V_{DD}	6	Power supply, +3.3V or +5V nominal
FOUT	7	Modulator output
BUF	8	Buffered mode select

PARAMETER MEASUREMENT INFORMATION

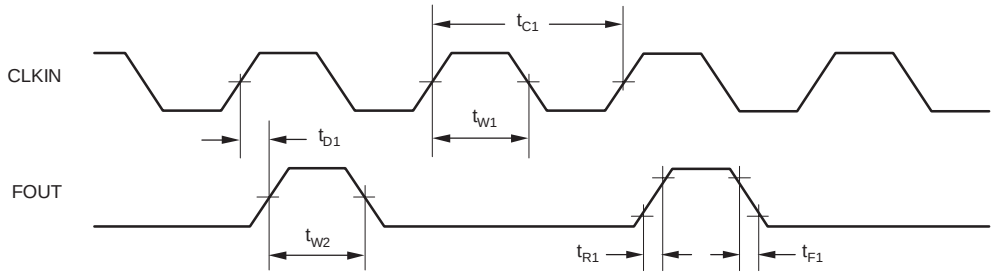


Figure 1. Timing Diagram

TIMING REQUIREMENTS: 5.0V

over recommended operating free-air temperature range at −40°C to +85°C,, and V_{DD} = 5V, unless otherwise noted.

PARAMETER			MIN	MAX	UNITS
t_{C1}	Input clock period	ADS1206	1000	TBD	ns
		ADS1207	250	TBD	ns
t_{W1}	Input clock high time		(t_{C1}/2) − 100	(t_{C1}/2) + 100	ns
t_{D1}	FOUT rising edge delay after input clock rising edge		TBD	TBD	ns
t_{W2}	FOUT high time		t_{C1} − 20	t_{C1} + 20	ns
t_{R1}	FOUT rise time		TBD	TBD	ns
t_{F1}	FOUT fall time		TBD	TBD	ns

NOTE: Applicable for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V. All input signals are specified with t_R = t_F = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See timing diagram.

TIMING REQUIREMENTS: 3.3V

over recommended operating free-air temperature range at −40°C to +85°C,, and V_{DD} = 3.3V, unless otherwise noted.

PARAMETER			MIN	MAX	UNITS
t_{C1}	Input clock period	ADS1206	1000	TBD	ns
		ADS1207	250	TBD	ns
t_{W1}	Input clock high time		(t_{C1}/2) − 100	(t_{C1}/2) + 100	ns
t_{D1}	FOUT rising edge delay after input clock rising edge		TBD	TBD	ns
t_{W2}	FOUT high time		t_{C1} − 8	t_{C1} + 8	ns
t_{R1}	FOUT rise time		TBD	TBD	ns
t_{F1}	FOUT fall time		TBD	TBD	ns

NOTE: Applicable for 3.3V nominal supply: V_{DD} (min) = 3.0V and V_{DD} (max) = 3.6V. All input signals are specified with t_R = t_F = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See timing diagram.

PRODUCT PREVIEW

PACKAGE OPTION ADDENDUM

25-Feb-2005

PACKAGING INFORMATION

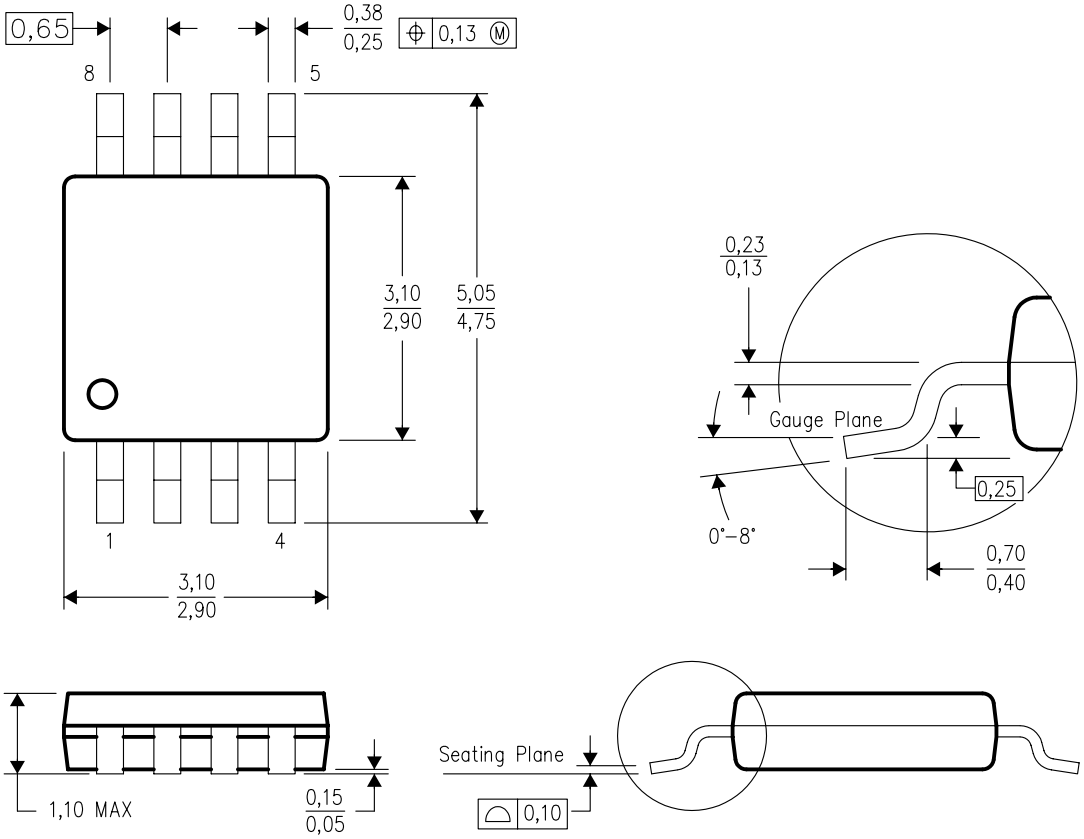
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1206IDGKR	PREVIEW	MSOP	DGK	8	2500	None	Call TI	Call TI
ADS1206IDGKT	PREVIEW	MSOP	DGK	8	250	None	Call TI	Call TI
ADS1207IDGKR	PREVIEW	MSOP	DGK	8		None	Call TI	Call TI
ADS1207IDGKT	PREVIEW	MSOP	DGK	8		None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

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