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AF4811P

P-Channel 30-V (D-S) MOSFET

■ Features

-Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
-Miniature SO-8 Surface Mount Package Saves Board Space
-High power and current handling capability
-Extended V_{GS} range (±25) for battery pack applications

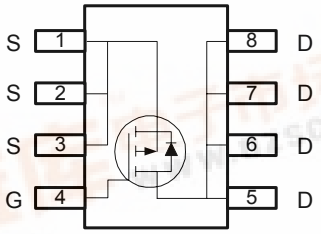
■ General Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWM DC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

■ Product Summary

V_{DS} (V)	$r_{DS(on)}$ (mΩ)	I_D (A)
-30	30@V_{GS}=-10V	9.5
	52@V_{GS}=-4.5V	7.5

■ Pin Assignments



SOP-8

■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

■ Ordering information

A X 4811P X X X

Feature	PN	Package	Lead Free	Packing
F :MOSFET		S: SOP-8	Blank : Normal L : Lead Free Package	Blank : Tube or Bulk A : Tape & Reel

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■ Absolute Maximum Ratings (T_A=25ºC unless otherwise noted)

Symbol	Parameter		Rating	Units
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current **(Note 1)**	T_A=25ºC	9.5	A
		T_A=70ºC	8.3	
I_{DM}	Pulsed Drain Current **(Note 2)**		±50	A
I_S	Continuous Source Current (Diode Conduction) **(Note 1)**		-2.1	A
P_D	Power Dissipation **(Note 1)**	T_A=25ºC	3.1	W
		T_A=70ºC	2.6	
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	ºC

■ Thermal Resistance Ratings

Symbol	Parameter		Maximum	Units
$R_{\theta JC}$	Maximum Junction-to-Case **(Note 1)**	t ≤ 5 sec	25	ºC/W
$R_{\theta JA}$	Maximum Junction-to-Ambient **(Note 1)**	t ≤ 10 sec	50	ºC/W

Note 1: surface Mounted on 1"x 1" FR4 Board.
Note 2: Pulse width limited by maximum junction temperature

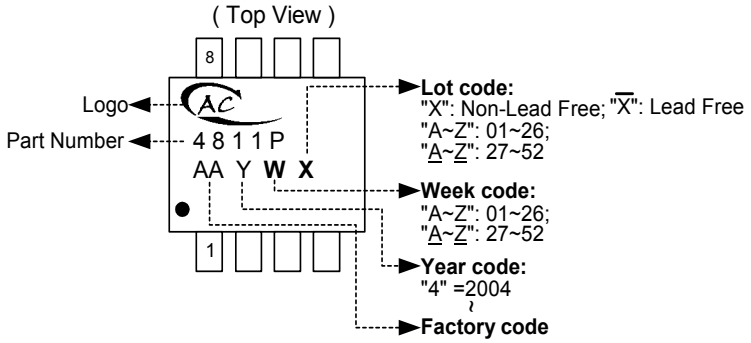
■ Specifications (T_A=25ºC unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
$V_{(BR)DSS}$	Drain-Source breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$V_{GS(th)}$	Gate-Threshold Voltage	V_{DS}= V_{GS}, I_D=-250uA	-1	-1.6	-3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±25V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V	-	-	-1	uA
		V_{DS}=-24V, V_{GS}=0V, T_J=55ºC	-	-	-5	
$I_{D(on)}$	On-State Drain Current **(Note 3)**	V_{DS}=-5V, V_{GS}=-10V	-50	-	-	A
$r_{DS(on)}$	Drain-Source On-Resistance **(Note 3)**	V_{GS}=-10V, I_D=-9.5A	-	24	30	mΩ
		V_{GS}=-4.5V, I_D=-7.5A	-	44	52	
		V_{GS}=-10V, I_D=-9.5A, T_J=55ºC	-	29	36	
g_{fs}	Forward Tranconductance **(Note 3)**	V_{GS}=-15V, I_D=-9.5A	-	31	-	S
V_{SD}	Diode Forward Voltage	I_S=-2.1A, V_{GS}=0V	-	-0.7	-1.2	V
Dynamic **(Note 4)**						
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-9.5A	-	15	26	nC
Q_{gs}	Gate-Source Charge		-	5.8	-	
Q_{gd}	Gate-Drain Charge		-	12	-	
Switching						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15, R_L=15Ω, ID=-1A, VGEN=-10V, RG=6Ω	-	15	26	nS
t_r	Rise Time		-	12	21	
$t_{d(off)}$	Turn-Off Delay Time		-	62	108	
t_f	Fall-Time		-	46	71	

Note 3: Pulse test: PW ≤ 300us duty cycle ≤ 2%.
Note 4: Guaranteed by design, not subject to production testing.

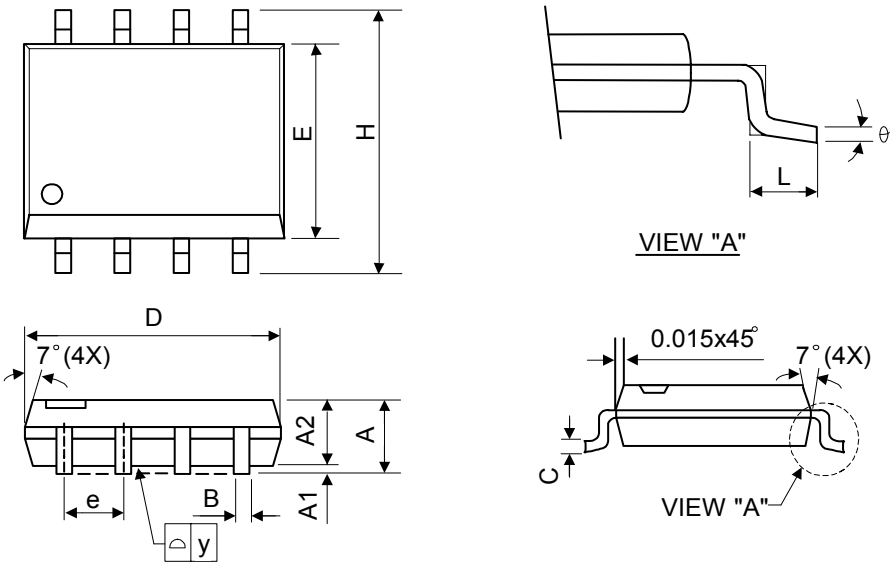
■ Marking Information

SOP-8L



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°