



## AIC1573

# 5-bit DAC, Synchronous PWM Power Regulator with Simple PWM Power Regulator, LDO And Linear Controller

### FEATURES

- Compatible with HIP6020.
- Provides 4 Regulated Voltages for Microprocessor Core, AGP Bus, Memory and GTL Bus Power.
- TTL Compatible 5-bit Digital-to-Analog Core Output Voltage Selection. Range from 1.3V to 3.5V.
  - 0.1V Steps from 2.1V to 3.5V.
  - 0.05V Steps from 1.3V to 2.05V.
- $\pm 1.0\%$  PWM Output Voltage for VCORE.
- $\pm 3\%$  PWM Output Voltage for AGP Bus.
- $\pm 3.0\%$  Reference Voltage for Chipset and/or Cache Memory and VGTL.
- Simple Voltage-Mode PWM Control with Built in Internal Compensation Networks.
- N-Channel MOSFET Driver for PWM buck converters.
- Linear Controller Drives Compatible with both N-Channel MOSFET and NPN Bipolar Series Pass Transistor.
- Operates from +3.3V, +5V and +12V Inputs.
- Fast Transient Response.
- Full 0% to 100% Duty Ratios.
- Adjustable Current Limit without External Sense Resistor.
- Microprocessor Core Voltage Protection against Upper MOSFET shorted to +5V.
- Power Good Output Voltage Monitor.
- Over-Voltage and Over-Current Fault Monitors.
- 200KHz Free-Running Oscillator Programmable up to 700KHz.

### APPLICATIONS

- Full Motherboard Power Regulation for Computers.

### DESCRIPTION

The AIC1573 combines two PWM voltage mode controllers and two linear controllers as well as the monitoring and protection functions in this chip. One PWM controller regulates the microprocessor core voltage with a synchronous rectified buck converter. The second PWM controller provides AGP bus 1.5V or 3.3V power with a standard buck converter. Two linear controllers regulate power for the 1.5V GTL bus and 1.8V power for the chip set core voltage and/or cache memory circuits.

An integrated 5 bit D/A converter that adjusts the microprocessor core voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V increments. The second PWM controller for AGP bus power is selectable by means of SELECT pin status for 1.5V or 3.3V with 3% accuracy. Two linear controllers drive with external N-channel MOSFETs to provide  $1.5V \pm 3\%$  and fixed output voltage  $1.8V \pm 3\%$ .

This chip monitors all the output voltages. Power Good signal is issued when the core voltage is within  $\pm 10\%$  of the DAC setting and the other levels are above their under-voltage levels. Over-voltage protection for the core output uses the lower N-channel MOSFET to prevent output voltage above 116% of the DAC setting.

The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's  $R_{DS(ON)}$ , eliminating the need for a current sensing resistor.






## ORDERING INFORMATION

AIC1573-CX

PACKAGING TYPE  
S: SMALL OUTLINE

ORDER NUMBER	PIN CONFIGURATION	
AIC1573CS (SO28)	UGATE2 <span style="border: 1px solid black; padding: 0 2px;">1</span> PHASE2 <span style="border: 1px solid black; padding: 0 2px;">2</span> VID4 <span style="border: 1px solid black; padding: 0 2px;">3</span> VID3 <span style="border: 1px solid black; padding: 0 2px;">4</span> VID2 <span style="border: 1px solid black; padding: 0 2px;">5</span> VID1 <span style="border: 1px solid black; padding: 0 2px;">6</span> VID0 <span style="border: 1px solid black; padding: 0 2px;">7</span> PGOOD <span style="border: 1px solid black; padding: 0 2px;">8</span> OCSET2 <span style="border: 1px solid black; padding: 0 2px;">9</span> VSEN2 <span style="border: 1px solid black; padding: 0 2px;">10</span> SELECT <span style="border: 1px solid black; padding: 0 2px;">11</span> SS <span style="border: 1px solid black; padding: 0 2px;">12</span> FAULT/RT <span style="border: 1px solid black; padding: 0 2px;">13</span> VSEN4 <span style="border: 1px solid black; padding: 0 2px;">14</span>	 <span style="border: 1px solid black; padding: 0 2px;">28</span> VCC <span style="border: 1px solid black; padding: 0 2px;">27</span> UGATE1 <span style="border: 1px solid black; padding: 0 2px;">26</span> PHASE1 <span style="border: 1px solid black; padding: 0 2px;">25</span> LGATE1 <span style="border: 1px solid black; padding: 0 2px;">24</span> PGND <span style="border: 1px solid black; padding: 0 2px;">23</span> OCSET1 <span style="border: 1px solid black; padding: 0 2px;">22</span> VSEN1 <span style="border: 1px solid black; padding: 0 2px;">21</span> FB1 <span style="border: 1px solid black; padding: 0 2px;">20</span> NC <span style="border: 1px solid black; padding: 0 2px;">19</span> VSEN3 <span style="border: 1px solid black; padding: 0 2px;">18</span> DRIVE3 <span style="border: 1px solid black; padding: 0 2px;">17</span> GND <span style="border: 1px solid black; padding: 0 2px;">16</span> VAUX <span style="border: 1px solid black; padding: 0 2px;">15</span> DRIVE4

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VCC ..... +15V

PGOOD, FAULT and GATE Voltage ..... GND -0.3V to V<sub>CC</sub> +0.3V

Input, Output , or I/O Voltage ..... GND -0.3V to 7V

Recommended Operating Conditions

Supply Voltage; VCC..... +12V±10%

Ambient Temperature Range ..... 0°C~70°C

Junction Temperature Range ..... 0°C~125°C

Thermal Information

Thermal Resistance,  $\theta_{JA}$

SOIC package ..... 70°C/W

SOIC package (with 3in<sup>2</sup> of copper) ..... 50°C/W

Maximum Junction Temperature (Plastic Package) ..... 150°C

Maximum Storage Temperature Range ..... -65°C ~ 150°C

Maximum Lead Temperature (Soldering 10 sec) ..... 300°C

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=12V$ ,  $T_A=25^{\circ}C$ , Unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>VCC SUPPLY CURRENT</b>						
Supply Current	UGATE1, LGATE1, UGATE2, DRIVE3 and DRIVE4 open	$I_{CC}$		3		mA
<b>POWER ON RESET</b>						
Rising VCC Threshold	VOCSET=4.5V	$V_{CCTHR}$			10.4	V
Falling VCC Threshold	VOCSET=4.5V	$V_{CCTHF}$	8.2			V
Rising VAUX Threshold		$VAUX_{THR}$		2.5		V
VAUX Threshold Hysteresis		$VAUX_{HYS}$		500		mV
Rising VOCSET1 Threshold		$V_{OCSETH}$		1.26		V
<b>OSCILLATOR</b>						
Free Running Frequency	RT=Open	F	170	200	230	KHz
Total Variation	$6k\Omega < RT < 200k\Omega$		-15		+15	%
Ramp. Amplitude	RT=open	$\Delta V_{OSC}$		1.5		VP-P
<b>DAC AND STANDARD BUCK REGULATOR REFERENCE</b>						
DAC (VID0~VID4) Input Low Voltage		$V_{IDL}$			0.8	V
DAC (VID0~VID4) Input High Voltage		$V_{IDH}$	2.0			V
DACOUT Voltage Accuracy	$V_{DAC}=1.8V\sim 3.5V$		-1.0		+1.0	%
PWM2 Reference Voltage	Select < 0.8V			1.5		V
PWM2 Reference Voltage	Select > 2.0V			3.3		V
PWM2 Reference Voltage Tolerance				3		%
<b>1.5V AND 1.8V LINEAR REGULATORS ( OUT3, OUT4)</b>						
Regulation				3		%
VSEN3 Regulation Voltage		$V_{REG3}$		1.5		V
VSEN4 Regulation Voltage		$V_{REG4}$		1.8		V
Under-Voltage Level ( $V_{SEN}/V_{REG}$ )	$V_{SEN}$ Rising	$V_{SENUV}$		75		%
Under-Voltage Hysteresis ( $V_{SEN}/V_{REG}$ )	$V_{SEN}$ Falling			5		%
Output Drive Current ( All Linears )	$V_{AUX}-V_{DRIVE} > 0.6V$		20	30		mA

**ELECTRICAL CHARACTERISTICS** (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>SYNCHRONOUS PWM CONTROLLER AMPLIFIER</b>						
DC Gain	(G.B.D.)			80		dB
Gain-Bandwidth Product	(G.B.D.)	GBWP		13		MHz
Slew Rate	(G.B.D.) note 1.	S <sub>R</sub>		6		V/μs
<b>PWM CONTROLLER GATE DRIVERS</b>						
U <sub>GATE1,2</sub> Upper Drive Source	V <sub>CC</sub> =12V, V <sub>UGATE</sub> = 6V	I <sub>UGH</sub>		0.9		A
U <sub>GATE1,2</sub> Upper Drive Sink	V <sub>UGATE</sub> =1V	R <sub>UGL</sub>		2.8	3.5	Ω
Lower Drive Source	V <sub>CC</sub> =12V, V <sub>LGATE</sub> =1V	I <sub>LGH</sub>		1		A
Lower Drive Sink	V <sub>LGATE</sub> =1V	R <sub>LGL</sub>		2.2	3.0	Ω
<b>PROTECTION</b>						
V <sub>SEN1</sub> Over-Voltage ( V <sub>SEN1</sub> /DACOUT )	V <sub>SEN1</sub> Rising	OVP		116	120	%
FAULT Sourcing Current	V <sub>CC</sub> -V <sub>FAULT/RT</sub> =2.0V	I <sub>ovp</sub>		20		mA
OCSET1,2 Current Source	V <sub>OCSET</sub> =4.5VDC	I <sub>ocset</sub>	170	200	230	μA
Soft-Start Current		I <sub>ss</sub>		25		μA
<b>POWER GOOD</b>						
V <sub>SEN1</sub> Upper Threshold ( V <sub>SEN1</sub> /DACOUT )	V <sub>SEN1</sub> Rising		108		111	%
V <sub>SEN1</sub> Under-Voltage ( V <sub>SEN1</sub> /DACOUT )	V <sub>SEN1</sub> Falling		92		95	%
V <sub>SEN1</sub> Hysteresis (V <sub>SEN1</sub> /DACOUT)	Upper and Lower Threshold			2		%
P <sub>GOOD</sub> Voltage Low	I <sub>PGOOD</sub> =-4mA	V <sub>PGOOD</sub>		0.4	0.8	V

Note 1. Without internal compensation network, the gain bandwidth product is 13MHz. Being associated with internal compensation networks, the Bode Plot is shown in Fig. 3, "Internal Compensation Gain of PWM Error Amplifier".

## TYPICAL PERFORMANCE CHARACTERISTICS

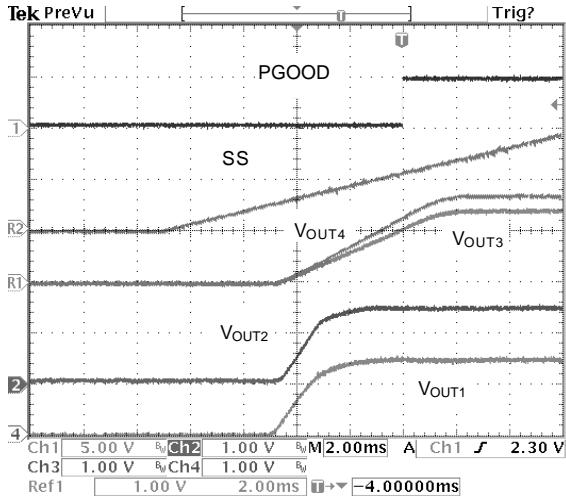


Fig. 1 Soft Start Interval with 4 Outputs and P<sub>GOOD</sub>

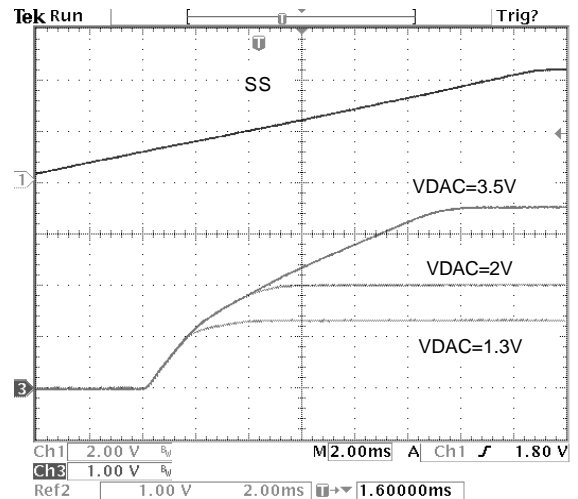


Fig. 2 Soft Start Initiates PWM Output

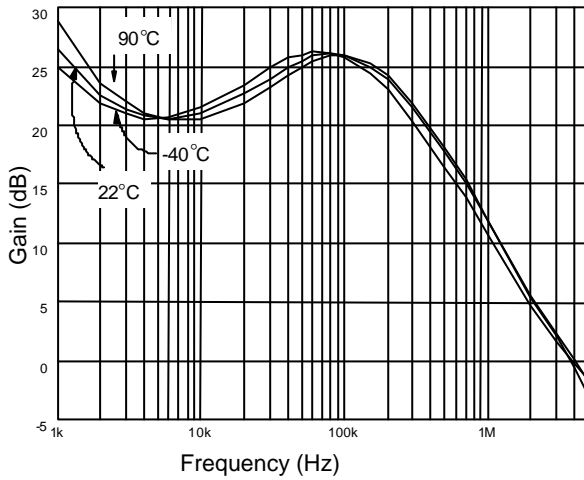


Fig. 3. Internal Compensation Gain of PWM Error Amplifier

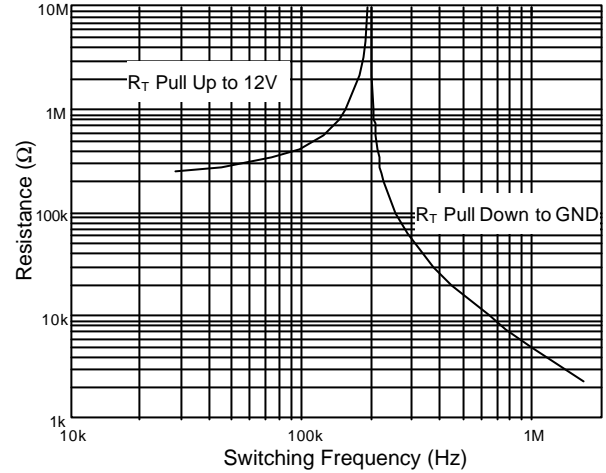


Fig. 4 R<sub>T</sub> Resistance vs. Frequency

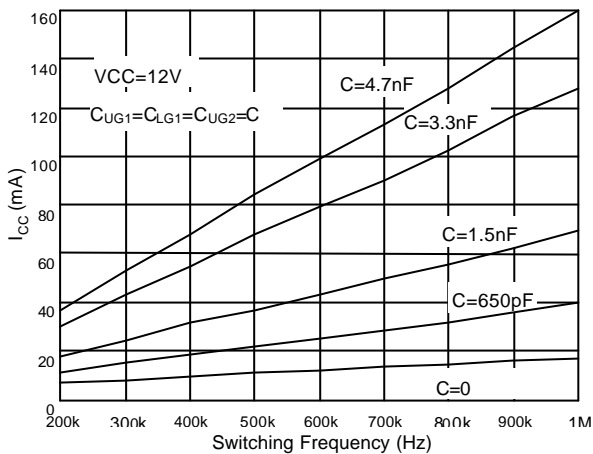


Fig. 5 Supply Current vs. Frequency

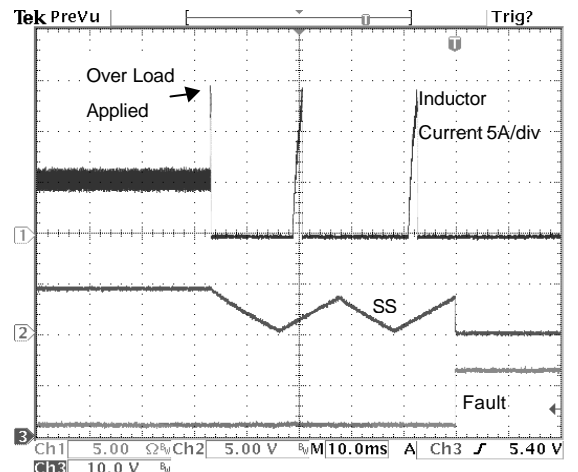


Fig. 6 Over Current ON Inductor

**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

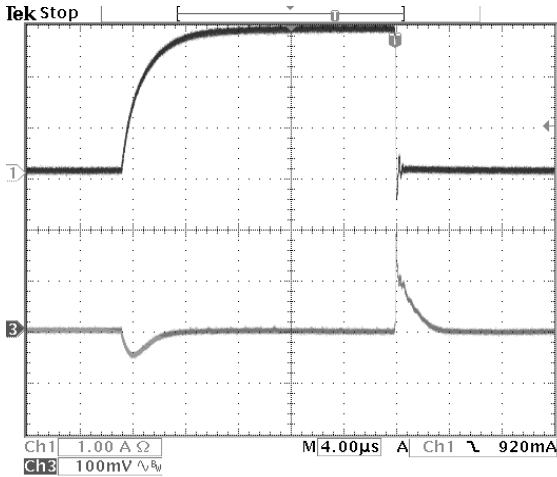


Fig. 7 Load Transient of Linear Controller

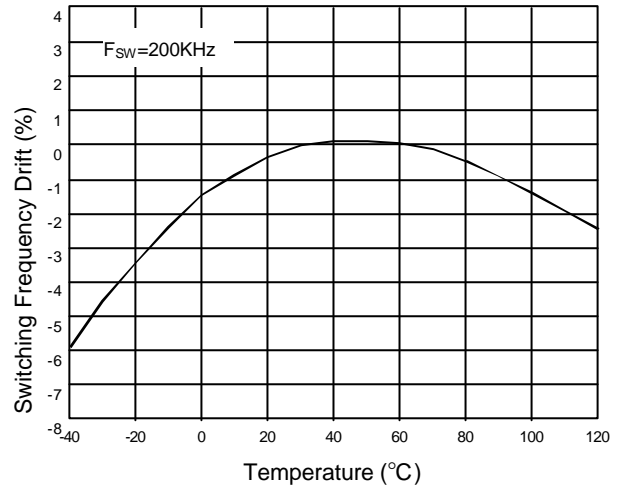


Fig. 8 Temperature vs. Switching Frequency Drift

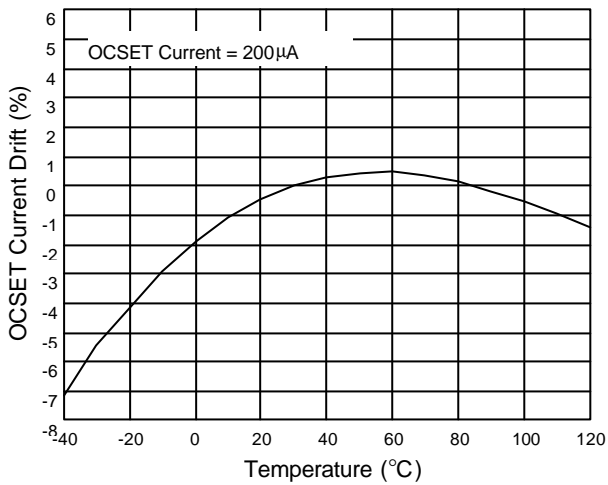


Fig. 9 Temperature vs. OCSET Current Drift

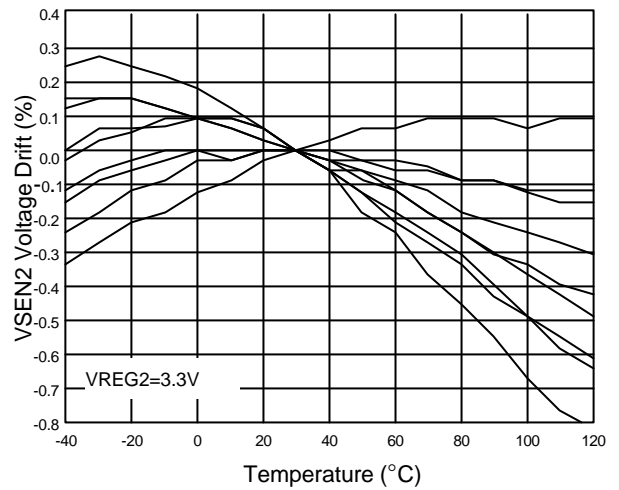


Fig. 10 Temperature Drift of 9 Different Parts

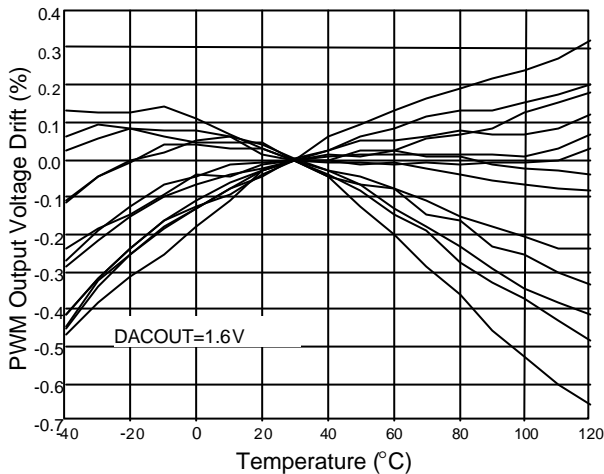


Fig. 11 Temperature Drift of 13 Different Parts

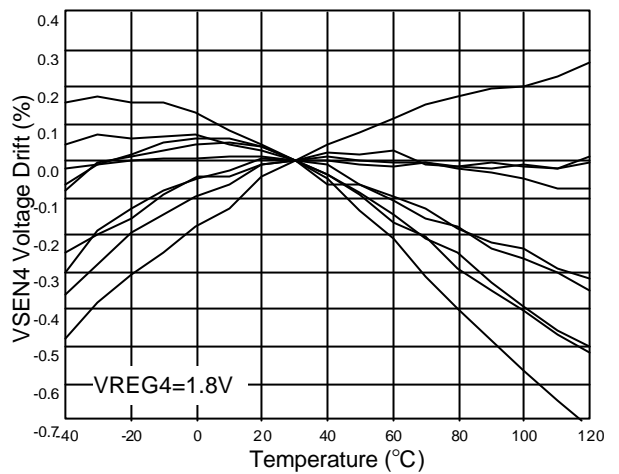


Fig. 12 Temperature Drift of 9 Different Parts

**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

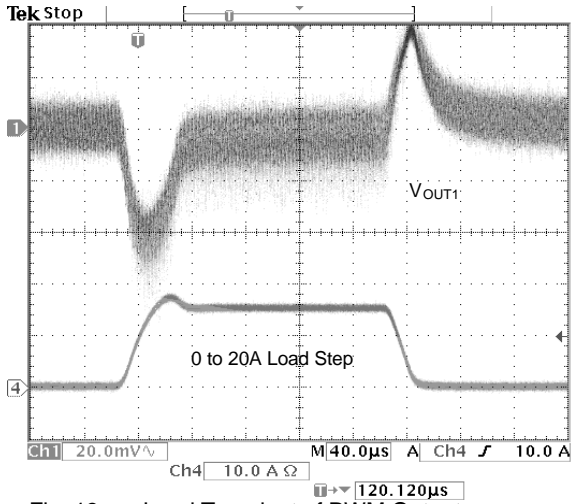


Fig. 13 Load Transient of PWM Output

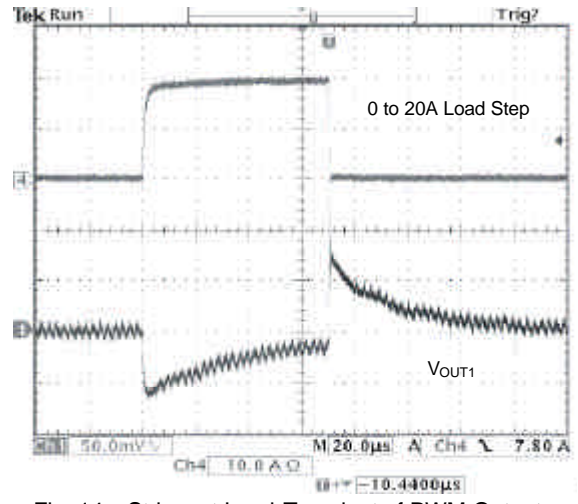


Fig. 14 Stringent Load Transient of PWM Output

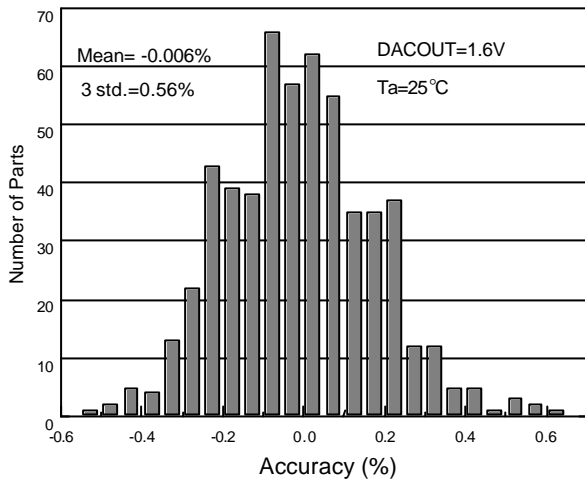


Fig. 15 FB Voltage Accuracy

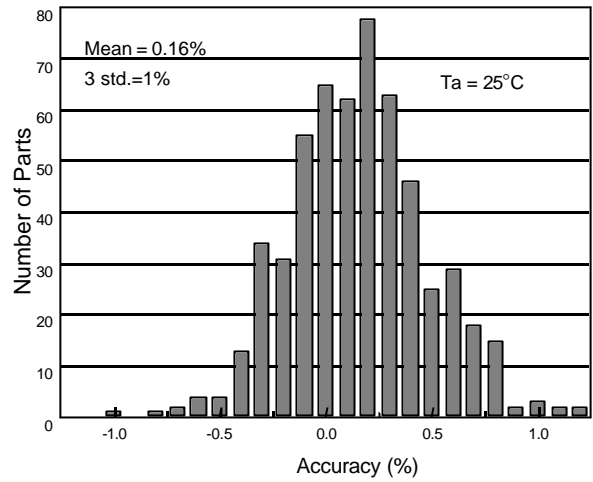
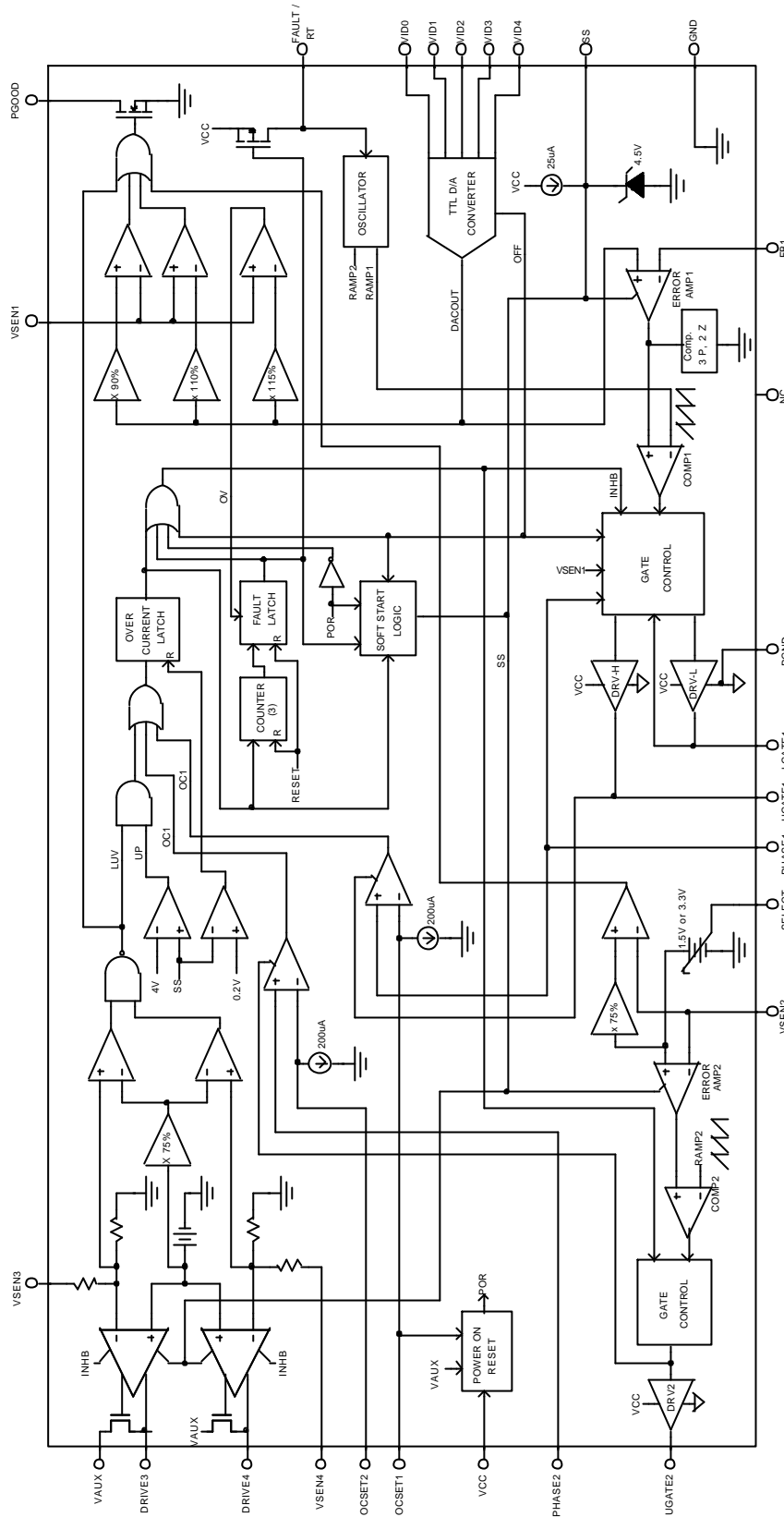


Fig. 16 VSEN3 Voltage Accuracy



■ BLOCK DIAGRAM



## ■ PIN DESCRIPTIONS

Pin 1: UGATE2: External high-side N-MOSFET gate drive pin. Connect UGATE2 to gate of the external high-side N-MOSFET .

Pin 2: PHASE2:

Over-current detection pin. Connect the PHASE2 pin to source of the external high-side N-MOSFET. This pin detects the voltage drop across the high-side N-MOSFET  $R_{DS(ON)}$  for over-current protection.

Pin 7: VID4:

Pin 6: VID3:

Pin 5: VID2:

Pin 4: VID1:

Pin 3: VID0: 5bit DAC voltage select pin. TTL-compatible inputs used to set the internal voltage reference VDAC. When left open, these pins are internally pulled up to 5V and provide logic ones. The level of VDAC sets the converter output voltage as well as the PGOOD and OVP thresholds.

Table 1 specifies the VDAC voltage for the 32 combinations of DAC inputs.

Pin 8: PGOOD: Power good indicator pin. PGOOD is an open drain output. This pin is pulled low when the converter output is  $\pm 10\%$  out of the VDAC reference voltage or the other outputs are below their under-voltage thresholds. The PGOOD output is open for VID codes that inhibit operation. See

Table 1.

Pin 9: OCSET2: Current limit sense pin. Connect a resistor  $R_{OCSET}$  from this pin to the drain of the external high-side N-MOSFET.  $R_{OCSET}$ , an internal  $200\mu A$  current source (IOCSET), and the upper N-MOSFET on-resistance ( $R_{DS(ON)}$ ) set the over-current trip point according to the following equation:

$$I_{PEAK} = \frac{IOCSET \times R_{OCSET}}{R_{DS(ON)}}$$

Pin 10: VSEN2: Connect this pin to the output of the standard buck PWM regulator. The voltage at this pin is regulated to the 1.5V/3.3V predetermined by the logic Low/High level status of the SELECT pin. This pin is also monitored by the PGOOD comparator circuit.

Pin 11: SELECT: This pin determines the output voltage of the AGP bus switching regulator. A low TTL input sets the output voltage to 1.5V, while a high input sets the output voltage to 3.3V.

Pin 12: SS: Soft-start pin. Connect a capacitor from this pin to ground. This capacitor, along with an internal  $25\mu A$  (typically) current source, sets the soft-start interval of the converter. Pulling this pin low will shut down the IC.

Pin 13: FAULT/RT: Frequency adjustment pin. Connecting a resistor (RT) from this pin to GND, increasing the frequency. Connecting a resistor (RT) from this pin to VCC, de-

creasing the frequency by the following figure (Fig.3).

This pin is 1.26V during normal operation, but it is pulled to VCC in the event of an over-voltage or over-current condition.

$$f = f_0 \left( 1 + \frac{25.2K}{R_T} \right),$$

$R_T$  pulled to GND

$$f = f_0 \left( 1 - \frac{VCC - 1.26V}{5 \times R_T} \right),$$

$R_T$  pulled to VCC,

where  $f_0$  is free run frequency.

- Pin14: VSEN4: Connect this pin to the 1.8V linear regulator's output. This pin is monitored for under-voltage events.
- Pin15: DRIVE4: Connect this pin to the gate of the external N-MOS to supply 1.8V power for Memory requirement.
- Pin 16: VAUX: The +3.3V input voltage at this pin is monitored for power-on – reset (POR) purpose. Connect to +5V provides boost current for the linear regulator's output.
- Pin 17: GND: Signal GND for IC. All voltage levels are measured with respect to this pin.
- Pin 18: DRIVE3: Connect this pin to the Gate of the external N-MOS for providing 1.5V power to GTL bus.
- Pin 19: VSEN3: Connect this pin to the 1.5V linear regulator's output. This pin is monitored for under-voltage events.
- Pin 20: COMP1: External compensation pin of the synchronous PWM converter. This pin is connected to error amplifier output and PWM comparator. A RC network is con-

nected to FB1 in to compensate the voltage control feedback loop of the converter.

- Pin 21: FB1: The error amplifier inverting input pin of the synchronous PWM converter. The FB1 pin and COMP1 pin are used to compensate the voltage-control feedback loop.
- Pin 22: VSEN1: Synchronous PWM converter's output voltage sense pin. Connect this pin to the converter output. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection function.
- Pin 23: OCSET1: Current limit sense pin. Connect a resistor  $R_{OCSET}$  from this pin to the drain of the external high-side N-MOSFET.  $R_{OCSET}$ , an internal 200 $\mu$ A current source ( $I_{OCSET}$ ), and the upper N-MOSFET on-resistance ( $R_{DS(ON)}$ ) set the over-current trip point according to the following equation:  

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The voltage at this pin is also monitored for power-on reset (POR) purpose.
- Pin 24: PGND: Driver power GND pin. PGND should be connected to a low impedance ground plane in close to lower N-MOSFET source.
- Pin 25: LGATE1: Lower N-MOSFET gate drive pin of the synchronous PWM converter.
- Pin 26: PHASE1: Over-current detection pin. Con-

Over-current detection pin. Con-

nect the PHASE1 pin to source of the external high-side N-MOSFET. This pin detects the voltage drop across the high-side N-MOSFET  $R_{DS(ON)}$  for over-current protection.

Pin 27: UGATE1: External high-side N-MOSFET gate drive pin. Connect UGATE1 to the synchronous PWM con-

verter's gate of the external high-side N-MOSFET .

Pin 28: VCC: The chip power supply pin. It also provides the gate bias charge for all the MOSFETs controlled by the IC. Recommended supply voltage is 12V. The voltage at this pin is monitored for Power-On-Reset purpose.

## ■ APPLICATIONS INFORMATION

The AIC1573 is designed for microprocessor computer applications with 3.3V and 5V power, and 12V bias input. This IC has two PWM controller and two linear controllers. The first PWM (PWM1) controller is designed to regulate the microprocessor core voltage (VOUT1) by driving 2 MOSFETs (Q1 and Q2) in a synchronous rectified buck converter configuration. The core voltage is regulated to a level programmed by the 5 bit D/A converter. The second PWM (PWM2) controller is designed to regulate the advanced graphics port (AGP) bus voltage (VOUT2). PWM2 One of the linear controllers is designed to regulate the advanced graphic port (AGP) bus voltage (VOUT2). PWM2 controller drives a MOSFET (Q3) in a standard buck converter and regulates the output voltage to a digitally-programmable level of 1.5V or 3.3V. Selection of either output voltage is achieved by applying the proper logic level at the SELECT pin. The two linear controllers supply the 1.5V GTL bus power (VOUT3) and 1.8V memory power (VOUT4).

The Power-On-Reset (POR) function continually monitors the input supply voltage +12V at VCC pin, the 5V input voltage at OCSET pin, and the 3.3V input at VAUX pin. The POR function initiates soft-start operation after all three input supply voltage exceeds their POR thresholds.

### Soft-Start

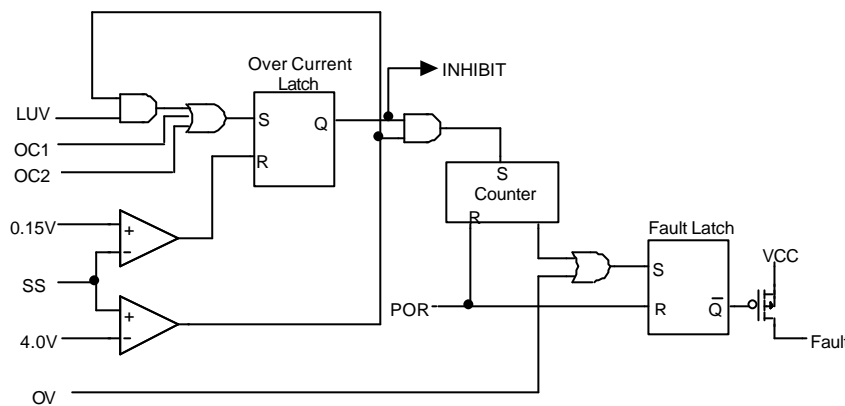
The POR function initiates the soft-start sequence. An internal  $25\mu\text{A}$  current source charges an external capacitor ( $C_{SS}$ ) on the SS pin to 4.5V. The PWM error amplifier reference input (Non-inverting terminal) and output (COMP1 pin) is clamped to a level proportional to the SS pin voltage. As the SS pin voltage slew from 1V to 4V, the output clamp generates PHASE pulses of increasing width that charge the output capacitors. After the output voltage increases to approximately 70% of the set value, the reference-input clamp slows the output voltage rate-of-rise and provides a smooth transition to the final set voltage. Additionally, all linear regulator's reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a rapid and controlled output voltage rise.

Fig.1 and Fig.2 show the soft-start sequence for the typical application. The internal oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on PHASE pin increases. The interval of increasing pulse width continues until output reaches sufficient voltage to transfer control to the input reference clamp.

Each linear output initially follows a ramp. When each output reaches sufficient voltage the input reference clamp slows the rate of output voltage rise. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their under-voltage levels.

### Fault Protection

All four outputs are monitored and protected against extreme overload. A sustained overload on any output or over-voltage on PWM1 output disables all outputs and drive the FAULT/RT pin to VCC.



**Fig. 17 Simplified Schematic of Fault Logic**

A simplified schematic is shown in figure 17. An over-voltage detected on VSEN1 immediately sets the fault latch. A sequence of three over-current fault signals also sets the fault latch. The over-current latch is set dependent on the status of the over-current (OC1 and OC2), linear under-voltage (LUV) and the soft-start signal. An under-voltage event on either linear output (VSEN3, VSEN4) is ignored until the soft-start interval. Cycling the bias input voltage (+12V off then on) resets the counter and the fault latch.

### Gate Drive Overlap Protection

The Overlap Protection circuit ensures that the Bottom MOSFET does not turn on until the Upper MOSFET source has reached a voltage low enough to ensure that shoot-through will not occur.

### Over-Voltage Protection

During operation, a short on the upper PWM1 MOSFET (Q1) causes VOUT1 to increase. When the output exceed the over-voltage threshold of 116% of DACOUT, the FAULT pin is set to fault latch and turns Q2 on as required in order to regulate VOUT1 to 116% of DACOUT. The fault latch raises the FAULT/RT pin close to VCC potential.

A separate over-voltage circuit provides protection during the initial application of power. For voltage on VCC pin below the power-on reset (and above ~4V), Should VSEN1 exceed 1.0V, the lower MOSFET (Q2) is driven on as needed to regulate VOUT1 to 1.0V.

### Over-Current Protection

All outputs are protected against excessive over-current. Both PWM controller uses upper MOSFET's on-resistance,  $R_{DS(ON)}$  to monitor the current for protection against shorted outputs. All linear controllers monitor VSEN for under-voltage to protect against excessive current.

When the voltage across Q1 ( $I_D R_{DS(ON)}$ ) exceeds the level ( $200\mu A R_{OCSET}$ ), this signal inhibit all outputs. Discharge soft-start capacitor ( $C_{SS}$ ) with  $28\mu A$  current sink, and increments the counter.  $C_{SS}$  recharges and initiates a soft-start cycle again until the counter increments to 3. This sets the fault latch to disable all outputs. Fig. 6 illustrates the over-current protection until an over load on OUT1.

Should excessive current cause VSEN to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch if  $C_{SS}$  is fully charged. Cycling the bias input power (off then on) reset the counter and the fault latch.

The over-current function for PWM controller will trip at a peak inductor current ( $I_{PEAK}$ ) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with MOSFET's temperature. To avoid over-current tripping in the normal operating load range, determine the  $R_{OCSET}$  resistor from the equation above with:

1. The maximum  $R_{DS(ON)}$  at the highest junction.
2. The minimum  $I_{OCSET}$  from the specification table.
3. Determine  $I_{PEAK} > I_{OUT(MAX)} + (\text{inductor ripple current}) / 2$ .

### OUT1 Voltage Program

The output voltage of the PWM1 converter is programmed to discrete levels between 1.3V to 3.5V. The VID pins program an internal voltage reference

(DACOUT) through a TTL compatible 5 bit digital to analog converter. The VID pins can be left open for a logic 1 input, because they are internally pulled up to 5V by a  $70k\Omega$  resistor. Changing the VID inputs during operation is not recommended. '11111' VID pin combinations disable the IC and open the PGOOD pin.

### OUT2 Voltage Selection

The AGP regulator output voltage is internally set to one of two discrete levels, based on the SELECT pin status. Left SELECT pin open, internal pulled high, the output voltage is 3.3V. Grounding SELECT pin will get the 1.5V output voltage.

The status of the SELECT pin can not be changed during operation of the IC without immediately causing a fault condition.

### Shutdown

Neither PWM output switches until the soft-start voltage exceeds the oscillator's valley voltage. Additionally, the reference on each linear's amplifier is clamped to the soft-start voltage. Holding the SS pin low turns off all four regulators.

The VID codes resulting in an INHIBIT as shown in Table 1 also shut down the IC.

### Oscillator Synchronization

The AIC1573 avoids the problem of cross talk between the converters by way of phase control method. Therefore, for both output voltage settings less than 2.4V or both greater than 2.4V, PWM1 operates out of phase with PWM2. For one PWM output voltage setting below 2.4V and the other PWM output voltage setting of 2.4V and above, PWM1 operates in phase with PWM2.

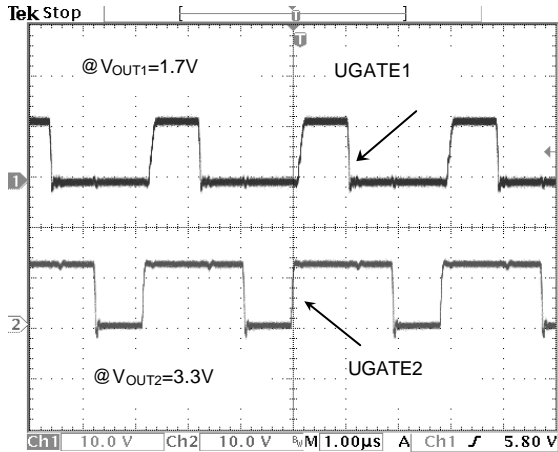


Fig. 18 PWM1 operates in phase with PWM2

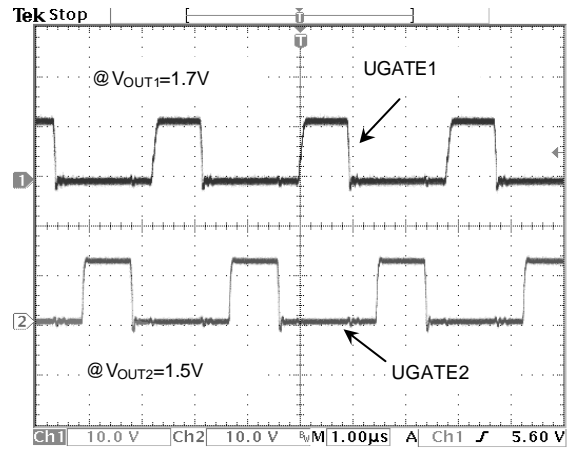


Fig. 19 PWM1 operates out of phase with PWM2

**Table 1 VOUT1 Voltage Program ( 0=connected to GND, 1=open or connected to 5V )**

For all package version											
PIN NAME					DACOUT VOLTAGE	PIN NAME					DACOUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30V	1	1	1	1	1	INHIBIT
0	1	1	1	0	1.35V	1	1	1	1	0	2.1 V
0	1	1	0	1	1.40V	1	1	1	0	1	2.2 V
0	1	1	0	0	1.45V	1	1	1	0	0	2.3 V
0	1	0	1	1	1.50V	1	1	0	1	1	2.4 V
0	1	0	1	0	1.55V	1	1	0	1	0	2.5 V
0	1	0	0	1	1.60V	1	1	0	0	1	2.6 V
0	1	0	0	0	1.65V	1	1	0	0	0	2.7 V
0	0	1	1	1	1.70V	1	0	1	1	1	2.8 V
0	0	1	1	0	1.75V	1	0	1	1	0	2.9 V
0	0	1	0	1	1.80 V	1	0	1	0	1	3.0 V
0	0	1	0	0	1.85 V	1	0	1	0	0	3.1 V
0	0	0	1	1	1.90 V	1	0	0	1	1	3.2 V
0	0	0	1	0	1.95 V	1	0	0	1	0	3.3 V
0	0	0	0	1	2.00 V	1	0	0	0	1	3.4 V
0	0	0	0	0	2.05 V	1	0	0	0	0	3.5 V

### Layout Considerations

Any inductance in the switched current path generates a large voltage spike during the switching interval. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component selection and tight layout of critical components, and short, wide metal trace minimize the voltage spike.

A ground plane should be used. Locate the input capacitors ( $C_{IN}$ ) close to the power switches. Minimize the loop formed by  $C_{IN}$ , the upper MOSFET (Q1) and the lower MOSFET (Q2) as possible. Connections should be as wide as short as possible to minimize loop inductance.

The connection between Q1, Q2 and output inductor should be as wide as short as practical. Since this connection has fast voltage transitions will easily induce EMI.

The output capacitor ( $C_{OUT}$ ) should be located as close the load as possible. Because minimize the transient load magnitude for high slew rate requires low inductance and resistance in circuit board

The AIC1573 is best placed over a quiet ground plane area. The GND pin should be connected to the groundside of the output capacitors. Under no circumstances should GND be returned to a ground inside the  $C_{IN}$ , Q1, Q2 loop. The GND and PGND pins should be shorted right at the IC. This help to minimize internal ground disturbances in the IC and prevents differences in ground potential from disrupting internal circuit operation.

The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 1A current. The traces for OUT2 need only be sized for 0.5A. Locate COUT2 close to the AIC1573.

The Vcc pin should be decoupled directly to GND by a 2.2 $\mu$ F ceramic capacitor, trace lengths should be as short as possible.

A multi-layer-printed circuit board is recommended. Figure 11 shows the connections of the critical components in the converter. The  $G_N$  and  $C_{OUT}$  could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer.

### PWM Output Capacitors

The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demand.

The ESR (equivalent series resistance) and ESL (equivalent series inductance) parameters rather than actual capacitance determine the buck capacitor values. For a given transient load magnitude, the output voltage transient change due to the output capacitor can be note by the following equation:

$$\Delta V_{OUT} = ESR \times \Delta I_{OUT} + ESL \times \frac{\Delta I_{OUT}}{\Delta T}, \quad \text{where}$$

$\Delta I_{OUT}$  is transient load current step.

After the initial transient, the ESL dependent term drops off. Because the strong relationship between output capacitor ESR and output load transient, the output capacitor is usually chosen for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. In most case, multiple electrolytic capacitors of small case size are better than a single large case capacitor.



### Output Inductor Selection

Inductor value and type should be chosen based on output slew rate requirement, output ripple requirement and expected peak current. Inductor value is primarily controlled by the required current response time. The AIC1573 will provide either 0% or 100% duty cycle in response to a load transient. The response time to a transient is different for the application of load and remove of load.

$$t_{RISE} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}},$$

$$t_{FALL} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}.$$

Where  $\Delta I_{OUT}$  is transient load current step.

In a typical 5V input, 2V output application, a 3μH inductor has a 1A/μS rise time, resulting in a 5μS delay in responding to a 5A load current step. To optimize performance, different combinations of input and output voltage and expected loads may require different inductor value. A smaller value of inductor will improve the transient response at the expense of increase output ripple voltage and inductor core saturation rating.

Peak current in the inductor will be equal to the maximum output load current plus half of inductor ripple current. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times L \times V_{IN}};$$

f = AIC1573 oscillator frequency.

The inductor must be able to withstand peak current without saturation, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss

### Input Capacitor Selection

Most of the input supply current is supplied by the input bypass capacitor, the resulting RMS current flow in the input capacitor will heat it up. Use a mix

of input bulk capacitors to control the voltage overshoot across the upper MOSFET. The ceramic capacitance for the high frequency decoupling should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedance. The buck capacitors to supply the RMS current is approximate equal to:

$$I_{RMS} = (1-D) \times \sqrt{D} \times \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left( \frac{V_{IN} \times D}{f \times L} \right)^2}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

, where

The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage.

### PWM MOSFET Selection

In high current PWM application, the MOSFET power dissipation, package type and heatsink are the dominant design factors. The conduction loss is the only component of power dissipation for the lower MOSFET, since it turns on into near zero voltage. The upper MOSFET has conduction loss and switching loss. The gate charge losses are proportional to the switching frequency and are dissipated by the AIC1573. However, the gate charge increases the switching interval,  $t_{SW}$ , which increase the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

$$P_{UPPER} = I_{OUT}^2 \times R_{DS(ON)} \times D + \frac{I_{OUT} \times V_{IN} \times t_{SW} \times f}{2}$$

$$P_{LOWER} = I_{OUT}^2 \times R_{DS(ON)} \times (1-D)$$

The equations above do not model power loss due to the reverse recovery of the lower MOSFET's body diode.

The  $R_{DS(ON)}$  is different for the two previous equations even if the type devices is used for both. This

is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Logic level MOSFETs should be selected based on on-resistance considerations,  $R_{DS(ON)}$  should be chosen base on input and output voltage, allowable power dissipation and maximum required output current. Power dissipation should be calculated based primarily on required efficiency or allowable thermal dissipation.

Rectifier Schottky diode is a clamp that prevent the loss parasitic MOSFET body diode from conducting during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode's rated reverse breakdown voltage must be greater than twice the maximum input voltage.

**Linear Controller MOSFET Selection**

The power dissipated in a linear regulator is:

$$P_{LINEAR} = I_{OUT} \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains junction temperature below the maximum rating while operation at the highest expected ambient temperature.

**Linear Output Capacitor**

The output capacitors for the linear regulator and linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. COUT3 and COUT4 should be selected for transient load regulation. The output capacitor for the linear regulator provides loop stability.

**PWM Feedback Analysis**

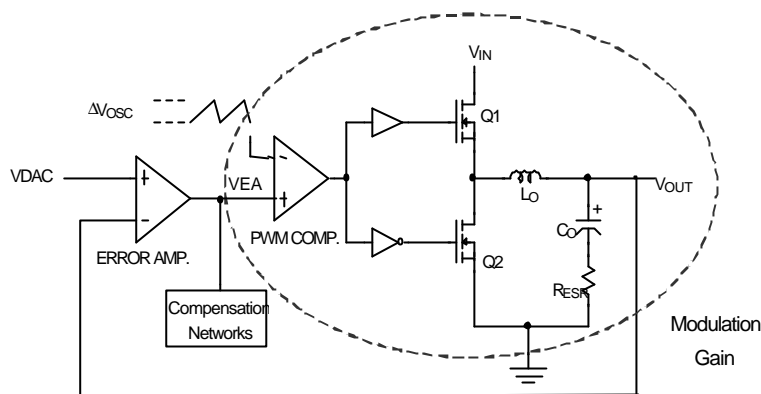


Fig 20. Control Loop

The compensation network consists of the error amplifier and built in compensation networks. The goal of the compensation network is to provide for fast response and adequate phase margin. Phase Margin is the difference between the closed loop phase at 0dB and 180 degree.

$$\text{Closed Loop Gain(dB)} = \text{Modulation Gain(dB)} + \text{Compensation Gain (dB)}$$

$$\begin{aligned} \text{Modulation Gain(dB)} \\ \approx 20 \log \left( \frac{V_{IN}}{\Delta V_{OSC}} \right) + 10 \log \left( 1 + \left( \frac{F}{F_{ESR}} \right)^2 \right) \end{aligned}$$

$$-10 \log \left[ \left[ 1 - \left( \frac{F}{F_{LC}} \right)^2 \right]^2 + \left( \frac{F}{F_{LC} \times Q} \right)^2 \right]$$

where

$$F_{LC} = \frac{1}{2p \sqrt{L_0 C_0}};$$

$$F_{ESR} = \frac{1}{2p \times R_{ESR} \times C_0};$$

$$\frac{1}{Q} = \sqrt{\frac{C_0}{L_0}} \times R_{ESR} + \sqrt{\frac{L_0}{C_0}} \times \frac{1}{R_{LOAD}}$$

The break frequency of Internal Compensation Gain are given by

$$F_{Z1} = 2.6 \text{ KHz};$$

$$F_{Z2} = 24 \text{ KHz};$$

$$F_{P1} = 30 \text{ KHz};$$

$$F_{P2} = 400 \text{ KHz}$$

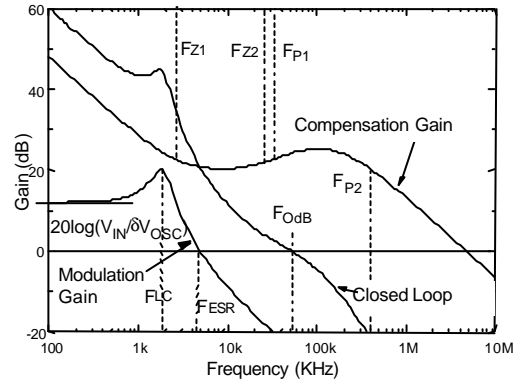


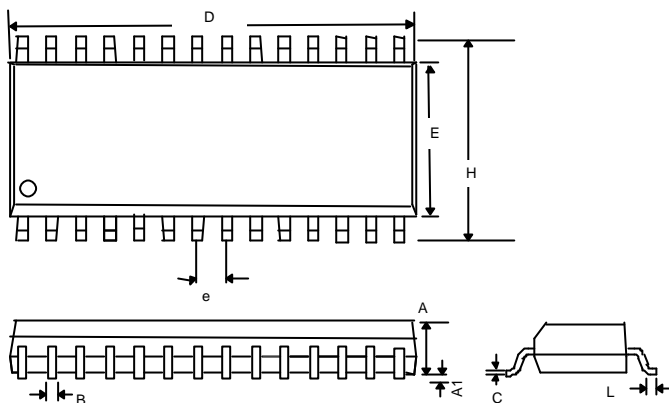
Fig. 21 Bode Plot of Converter Gain

### Bode Plot of Converter Gain

Sampling theory shows that F<sub>0dB</sub> must be less than half the switching frequency for the loop to be stable. But it must be considerably less than that, or there will be large amplitude switching frequency ripple at the output. Thus, the usual practice is to fix F<sub>0dB</sub> at 1/4 to 1/5 the switching frequency.

## PHYSICAL DIMENSIONS

### 28 LEAD PLASTIC SO (unit: mm)



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 (TYP)	
H	10.00	10.65
L	0.40	1.27