



# Complete 12-Bit A/D Converter

## AD574A\*

### FEATURES

**Complete 12-Bit A/D Converter with Reference and Clock**

**8- and 16-Bit Microprocessor Bus Interface**

**Guaranteed Linearity Over Temperature**

0°C to +70°C – AD574AJ, K, L

–55°C to +125°C – AD574AS, T, U

**No Missing Codes Over Temperature**

**35  $\mu$ s Maximum Conversion Time**

**Buried Zener Reference for Long-Term Stability**

and Low Gain T.C. 10 ppm/°C max AD574AL

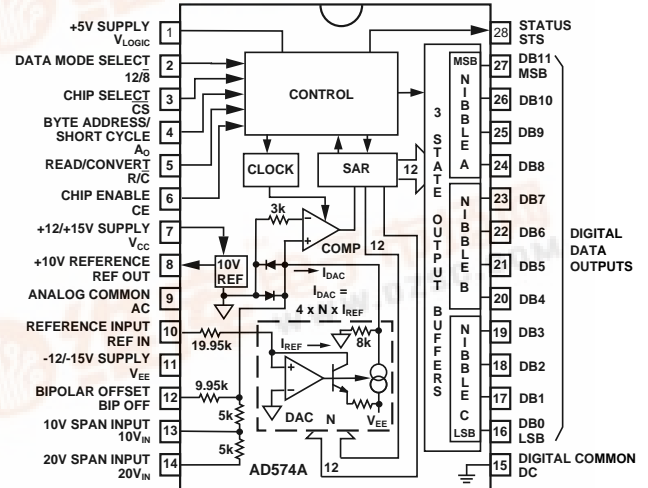
12.5 ppm/°C max AD574AU

**Ceramic DIP, Plastic DIP or PLCC Package**

**Available in Higher Speed, Pinout-Compatible Versions**  
(15  $\mu$ s AD674B, 80  $\mu$ s AD774B; 10  $\mu$ s (with SHA) AD1674)

**Available in Versions Compliant with MIL-STD-883 and JAN QPL**

### BLOCK DIAGRAM AND PIN CONFIGURATION



### PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I<sup>2</sup>L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I<sup>2</sup>L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0°C to +70°C temperature range. The AD574AS, T, and U are specified for the –55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

### PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 volts to +10 volts and 0 volts to +20 volts unipolar, –5 volts to +5 volts and –10 volts to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of  $\pm 0.1\%$  can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15 ppm/°C typical T.C. The reference is available externally and can drive up to 1.5 mA beyond the requirements of the reference and bipolar offset resistors.
4. AD674B (15  $\mu$ s) and AD774B (80  $\mu$ s) provide higher speed, pin compatibility; AD1674 (10  $\mu$ s) includes on-chip Sample-and-Hold Amplifier (SHA).

\*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

REV. B

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# AD574A—SPECIFICATIONS (@ +25°C with $V_{CC} = +15\text{ V}$ or $+12\text{ V}$ , $V_{LOGIC} = +5\text{ V}$ , $V_{EE} = -15\text{ V}$ or $-12\text{ V}$ unless otherwise noted)

| Model  | AD574AJ |      |          | AD574AK |      |          | AD574AL |      |          | Units        |
|--|---------|------|----------|---------|------|----------|---------|------|----------|--------------|
|  | Min     | Typ  | Max      | Min     | Typ  | Max      | Min     | Typ  | Max      |              |
| RESOLUTION   |         |      | 12       |         |      | 12       |         |      | 12       | Bits         |
| LINEARITY ERROR @ +25°C  |         |      | ±1       |         |      | ±1/2     |         |      | ±1/2     | LSB          |
| $T_{MIN}$ to $T_{MAX}$   |         |      | ±1       |         |      | ±1/2     |         |      | ±1/2     | LSB          |
| DIFFERENTIAL LINEARITY ERROR<br>(Minimum Resolution for Which No Missing Codes are Guaranteed)<br>$T_{MIN}$ to $T_{MAX}$ | 11      |      |          | 12      |      |          | 12      |      |          | Bits         |
| UNIPOLAR OFFSET (Adjustable to Zero)   |         |      | ±2       |         |      | ±1       |         |      | ±1       | LSB          |
| BIPOLAR OFFSET (Adjustable to Zero)  |         |      | ±4       |         |      | ±4       |         |      | ±2       | LSB          |
| FULL-SCALE CALIBRATION ERROR<br>(With Fixed 50 Ω Resistor from REF OUT to REF IN)<br>(Adjustable to Zero)                |         |      | 0.25     |         |      | 0.25     |         |      | 0.125    | % of FS      |
| TEMPERATURE RANGE  | 0       |      | +70      | 0       |      | +70      | 0       |      | +70      | °C           |
| TEMPERATURE COEFFICIENTS<br>(Using Internal Reference)<br>$T_{MIN}$ to $T_{MAX}$   |         |      |          |         |      |          |         |      |          |              |
| Unipolar Offset  |         |      | ±2 (10)  |         |      | ±1 (5)   |         |      | ±1 (5)   | LSB (ppm/°C) |
| Bipolar Offset   |         |      | ±2 (10)  |         |      | ±1 (5)   |         |      | ±1 (5)   | LSB (ppm/°C) |
| Full-Scale Calibration   |         |      | ±9 (50)  |         |      | ±5 (27)  |         |      | ±2 (10)  | LSB (ppm/°C) |
| POWER SUPPLY REJECTION<br>Max Change in Full-Scale Calibration   |         |      |          |         |      |          |         |      |          |              |
| $V_{CC} = 15\text{ V} \pm 1.5\text{ V}$ or $12\text{ V} \pm 0.6\text{ V}$  |         |      | ±2       |         |      | ±1       |         |      | ±1       | LSB          |
| $V_{LOGIC} = 5\text{ V} \pm 0.5\text{ V}$  |         |      | ±1/2     |         |      | ±1/2     |         |      | ±1/2     | LSB          |
| $V_{EE} = -15\text{ V} \pm 1.5\text{ V}$ or $-12\text{ V} \pm 0.6\text{ V}$  |         |      | ±2       |         |      | ±1       |         |      | ±1       | LSB          |
| ANALOG INPUT   |         |      |          |         |      |          |         |      |          |              |
| Input Ranges   |         |      |          |         |      |          |         |      |          |              |
| Bipolar  | -5      |      | +5       | -5      |      | +5       | -5      |      | +5       | Volts        |
|  | -10     |      | +10      | -10     |      | +10      | -10     |      | +10      | Volts        |
| Unipolar   | 0       |      | +10      | 0       |      | +10      | 0       |      | +10      | Volts        |
|  | 0       |      | +20      | 0       |      | +20      | 0       |      | +20      | Volts        |
| Input Impedance  |         |      |          |         |      |          |         |      |          |              |
| 10 Volt Span   | 3       | 5    | 7        | 3       | 5    | 7        | 3       | 5    | 7        | kΩ           |
| 20 Volt Span   | 6       | 10   | 14       | 6       | 10   | 14       | 6       | 10   | 14       | kΩ           |
| DIGITAL CHARACTERISTICS <sup>1</sup> ( $T_{MIN}$ – $T_{MAX}$ )   |         |      |          |         |      |          |         |      |          |              |
| Inputs <sup>2</sup> (CE, $\overline{CS}$ , R/ $\overline{C}$ , $A_0$ )   |         |      |          |         |      |          |         |      |          |              |
| Logic “1” Voltage  | +2.0    |      | +5.5     | +2.0    |      | +5.5     | +2.0    |      | +5.5     | Volts        |
| Logic “0” Voltage  | -0.5    |      | +0.8     | -0.5    |      | +0.8     | -0.5    |      | +0.8     | Volts        |
| Current  | -20     |      | +20      | -20     |      | +20      | -20     |      | +20      | μA           |
| Capacitance  |         | 5    |          |         | 5    |          |         | 5    |          | pF           |
| Output (DB11–DB0, STS)   |         |      |          |         |      |          |         |      |          |              |
| Logic “1” Voltage ( $I_{SOURCE} \leq 500\text{ μA}$ )  | +2.4    |      |          | +2.4    |      |          | +2.4    |      |          | Volts        |
| Logic “0” Voltage ( $I_{SINK} \leq 1.6\text{ mA}$ )  |         |      | +0.4     |         |      | +0.4     |         |      | +0.4     | Volts        |
| Leakage (DB11–DB0, High-Z State)   | -20     |      | +20      | -20     |      | +20      | -20     |      | +20      | μA           |
| Capacitance  |         | 5    |          |         | 5    |          |         | 5    |          | pF           |
| POWER SUPPLIES   |         |      |          |         |      |          |         |      |          |              |
| Operating Range  |         |      |          |         |      |          |         |      |          |              |
| $V_{LOGIC}$  | +4.5    |      | +5.5     | +4.5    |      | +5.5     | +4.5    |      | +5.5     | Volts        |
| $V_{CC}$   | +11.4   |      | +16.5    | +11.4   |      | +16.5    | +11.4   |      | +16.5    | Volts        |
| $V_{EE}$   | -11.4   |      | -16.5    | -11.4   |      | -16.5    | -11.4   |      | -16.5    | Volts        |
| Operating Current  |         |      |          |         |      |          |         |      |          |              |
| $I_{LOGIC}$  |         | 30   | 40       |         | 30   | 40       |         | 30   | 40       | mA           |
| $I_{CC}$   |         | 2    | 5        |         | 2    | 5        |         | 2    | 5        | mA           |
| $I_{EE}$   |         | 18   | 30       |         | 18   | 30       |         | 18   | 30       | mA           |
| POWER DISSIPATION  |         | 390  | 725      |         | 390  | 725      |         | 390  | 725      | mW           |
| INTERNAL REFERENCE VOLTAGE   | 9.98    | 10.0 | 10.02    | 9.98    | 10.0 | 10.02    | 9.99    | 10.0 | 10.01    | Volts        |
| Output Current (Available for External Loads) <sup>3</sup><br>(External Load Should not Change During Conversion)        |         |      | 1.5      |         |      | 1.5      |         |      | 1.5      | mA           |
| PACKAGE OPTIONS <sup>4</sup>   |         |      |          |         |      |          |         |      |          |              |
| Ceramic (D-28)   |         |      | AD574ASD |         |      | AD574AKD |         |      | AD574ALD |              |
| Plastic (N-28)   |         |      | AD574AJN |         |      | AD574AKN |         |      | AD574ALN |              |
| PLCC (P-28A)   |         |      | AD574AJP |         |      | AD574AKP |         |      |          |              |
| LCC (E-28A)  |         |      | AD574AJE |         |      | AD574AKE |         |      |          |              |

## NOTES

<sup>1</sup>Detailed Timing Specifications appear in the Timing Section.

<sup>2</sup>12/8 Input is not TTL-compatible and must be hard wired to  $V_{LOGIC}$  or Digital Common.

<sup>3</sup>The reference should be buffered for operation on  $\pm 12\text{ V}$  supplies.

<sup>4</sup>D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

Specifications subject to change without notice.

# AD574A

| Model   | AD574AS   |          |              | AD574AT   |          |              | AD574AU   |          |              | Units          |
|---|-----------|----------|--------------|-----------|----------|--------------|-----------|----------|--------------|----------------|
|   | Min       | Typ      | Max          | Min       | Typ      | Max          | Min       | Typ      | Max          |                |
| RESOLUTION  |           |          | 12           |           |          | 12           |           |          | 12           | Bits           |
| LINEARITY ERROR @ +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub>   |           |          | ±1<br>±1     |           |          | ±1/2<br>±1   |           |          | ±1/2<br>±1   | LSB<br>LSB     |
| DIFFERENTIAL LINEARITY ERROR<br>(Minimum Resolution for Which No<br>Missing Codes are Guaranteed)<br>T <sub>MIN</sub> to T <sub>MAX</sub>       | 11        |          |              | 12        |          |              | 12        |          |              | Bits           |
| UNIPOLAR OFFSET (Adjustable to Zero)  |           |          | ±2           |           |          | ±1           |           |          | ±1           | LSB            |
| BIPOLAR OFFSET (Adjustable to Zero)   |           |          | ±4           |           |          | ±4           |           |          | ±2           | LSB            |
| FULL-SCALE CALIBRATION ERROR<br>(With Fixed 50 Ω Resistor from REF OUT to REF IN)<br>(Adjustable to Zero)                                       |           |          | 0.25         |           |          | 0.25         |           |          | 0.125        | % of FS        |
| TEMPERATURE RANGE   | −55       |          | +125         | −55       |          | +125         | −55       |          | +125         | °C             |
| TEMPERATURE COEFFICIENTS<br>(Using Internal Reference)<br>(T <sub>MIN</sub> to T <sub>MAX</sub> )   |           |          |              |           |          |              |           |          |              |                |
| Unipolar Offset   |           |          | ±2 (5)       |           |          | ±1 (2.5)     |           |          | ±1 (2.5)     | LSB (ppm/°C)   |
| Bipolar Offset  |           |          | ±4 (10)      |           |          | ±2 (5)       |           |          | ±1 (2.5)     | LSB (ppm/°C)   |
| Full-Scale Calibration  |           |          | ±20 (50)     |           |          | ±10 (25)     |           |          | ±5 (12.5)    | LSB (ppm/°C)   |
| POWER SUPPLY REJECTION<br>Max Change in Full-Scale Calibration  |           |          |              |           |          |              |           |          |              |                |
| V <sub>CC</sub> = 15 V ± 1.5 V or 12 V ± 0.6 V  |           |          | ±2           |           |          | ±1           |           |          | ±1           | LSB            |
| V <sub>LOGIC</sub> = 5 V ± 0.5 V  |           |          | ±1/2         |           |          | ±1/2         |           |          | ±1/2         | LSB            |
| V <sub>EE</sub> = −15 V ± 1.5 V or −12 V ± 0.6 V  |           |          | ±2           |           |          | ±1           |           |          | ±1           | LSB            |
| ANALOG INPUT  |           |          |              |           |          |              |           |          |              |                |
| Input Ranges  |           |          |              |           |          |              |           |          |              |                |
| Bipolar   | −5<br>−10 |          | +5<br>+10    | −5<br>−10 |          | +5<br>+10    | −5<br>−10 |          | +5<br>+10    | Volts<br>Volts |
| Unipolar  | 0<br>0    |          | +10<br>+20   | 0<br>0    |          | +10<br>+20   | 0<br>0    |          | +10<br>+20   | Volts<br>Volts |
| Input Impedance   |           |          |              |           |          |              |           |          |              |                |
| 10 Volt Span  | 3         | 5        | 7            | 3         | 5        | 7            | 3         | 5        | 7            | kΩ             |
| 20 Volt Span  | 6         | 10       | 14           | 6         | 10       | 14           | 6         | 10       | 14           | kΩ             |
| DIGITAL CHARACTERISTICS <sup>1</sup> (T <sub>MIN</sub> –T <sub>MAX</sub> )  |           |          |              |           |          |              |           |          |              |                |
| Inputs <sup>2</sup> (CE, $\overline{\text{CS}}$ , R/ $\overline{\text{C}}$ , A <sub>0</sub> )   |           |          |              |           |          |              |           |          |              |                |
| Logic “1” Voltage   | +2.0      |          | +5.5         | +2.0      |          | +5.5         | +2.0      |          | +5.5         | Volts          |
| Logic “0” Voltage   | −0.5      |          | +0.8         | −0.5      |          | +0.8         | −0.5      |          | +0.8         | Volts          |
| Current   | −20       |          | +20          | −20       |          | +20          | −20       |          | +20          | μA             |
| Capacitance   |           | 5        |              |           | 5        |              |           | 5        |              | pF             |
| Output (DB11–DB0, STS)  |           |          |              |           |          |              |           |          |              |                |
| Logic “1” Voltage (I <sub>SOURCE</sub> ≤ 500 μA)  | +2.4      |          |              | +2.4      |          |              | +2.4      |          |              | Volts          |
| Logic “0” Voltage (I <sub>SINK</sub> ≤ 1.6 mA)  |           |          | +0.4         |           |          | +0.4         |           |          | +0.4         | Volts          |
| Leakage (DB11–DB0, High-Z State)  | −20       |          | +20          | −20       |          | +20          | −20       |          | +20          | μA             |
| Capacitance   |           | 5        |              |           | 5        |              |           | 5        |              | pF             |
| POWER SUPPLIES  |           |          |              |           |          |              |           |          |              |                |
| Operating Range   |           |          |              |           |          |              |           |          |              |                |
| V <sub>LOGIC</sub>  | +4.5      |          | +5.5         | +4.5      |          | +5.5         | +4.5      |          | +5.5         | Volts          |
| V <sub>CC</sub>   | +11.4     |          | +16.5        | +11.4     |          | +16.5        | +11.4     |          | +16.5        | Volts          |
| V <sub>EE</sub>   | −11.4     |          | −16.5        | −11.4     |          | −16.5        | −11.4     |          | −16.5        | Volts          |
| Operating Current   |           |          |              |           |          |              |           |          |              |                |
| I <sub>LOGIC</sub>  |           | 30       | 40           |           | 30       | 40           |           | 30       | 40           | mA             |
| I <sub>CC</sub>   |           | 2        | 5            |           | 2        | 5            |           | 2        | 5            | mA             |
| I <sub>EE</sub>   |           | 18       | 30           |           | 18       | 30           |           | 18       | 30           | mA             |
| POWER DISSIPATION   |           | 390      | 725          |           | 390      | 725          |           | 390      | 725          | mW             |
| INTERNAL REFERENCE VOLTAGE<br>Output Current (Available for External Loads) <sup>3</sup><br>(External Load Should not Change During Conversion) | 9.98      | 10.0     | 10.02<br>1.5 | 9.98      | 10.0     | 10.02<br>1.5 | 9.99      | 10.0     | 10.01<br>1.5 | Volts<br>mA    |
| PACKAGE OPTION <sup>4</sup><br>Ceramic (D-28)   |           | AD574ASD |              |           | AD574ATD |              |           | AD574AUD |              |                |

## NOTES

<sup>1</sup>Detailed Timing Specifications appear in the Timing Section.

<sup>2</sup>12/8 Input is not TTL-compatible and must be hard wired to V<sub>LOGIC</sub> or Digital Common.

<sup>3</sup>The reference should be buffered for operation on ±12 V supplies.

<sup>4</sup>D = Ceramic DIP.

Specifications subject to change without notice.



## **THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE**

### **DEFINITIONS OF SPECIFICATIONS**

#### **LINEARITY ERROR**

Linearity error refers to the deviation of each individual code from a line drawn from “zero” through “full scale”. The point used as “zero” occurs 1/2 LSB (1.22 mV for 10 volt span) before the first code transition (all zeros to only the LSB “on”). “Full scale” is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, L, T, and U grades are guaranteed for maximum nonlinearity of  $\pm 1/2$  LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and S grades are guaranteed to  $\pm 1$  LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

#### **DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)**

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

#### **UNIPOLAR OFFSET**

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

#### **BIPOLAR OFFSET**

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

#### **QUANTIZATION UNCERTAINTY**

Analog-to-digital converters exhibit an inherent quantization uncertainty of  $\pm 1/2$  LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

#### **LEFT-JUSTIFIED DATA**

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to  $\frac{4095}{4096}$ . This implies a binary point to the left of the MSB.

#### **FULL-SCALE CALIBRATION ERROR**

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05% to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4.

#### **TEMPERATURE COEFFICIENTS**

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at  $T_{\text{MIN}}$  or  $T_{\text{MAX}}$ .

#### **POWER SUPPLY REJECTION**

The standard specifications for the AD574A assume use of +5.00 V and  $\pm 15.00$  V or  $\pm 12.00$  V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

#### **CODE WIDTH**

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44 mV out of 10 volts for a 12-bit ADC.





It is critically important that the AD574A power supplies be filtered, well regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed circuit construction is preferred.

The analog common at Pin 9 is the ground reference point for the internal reference and is thus the “high quality” ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an environment of high digital noise content, the analog and digital commons should be connected together at the package. In some situations, the digital common at Pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5 V, +12 V/+15 V and -12 V/-15 V), the analog input, and the conversion initiation command, as discussed on the next

All of the thin-film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees  $\pm 1$  LSB max zero offset error and  $\pm 0.25\%$  (10 LSB) max full-scale error. (Typical full-scale error is  $\pm 2$  LSB.) If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed. If the full-scale trim is not needed, a  $50\ \Omega \pm 1\%$  metal film resistor should be connected between Pin 8 and Pin 10.

## UNIPOLAR CALIBRATION

If Pin 12 is connected to Pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately  $\pm 15$  mV of offset trim range.

# AD574A

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale (9.9963 for a 10 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

## BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a  $50 \Omega \pm 1\%$  fixed resistor. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale ( $-4.9988$  V for the  $\pm 5$  V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale ( $+4.9963$  V the  $\pm 5$  V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

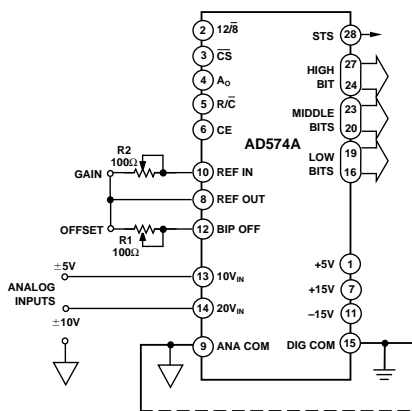


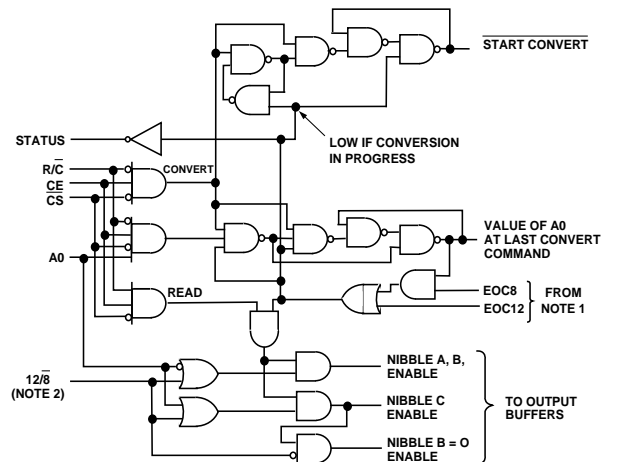
Figure 5. Bipolar Input Connections

## CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD574A.

The control signals CE,  $\overline{CS}$ , and  $\overline{R/C}$  control the operation of the converter. The state of  $\overline{R/C}$  when CE and  $\overline{CS}$  are both asserted determines whether a data read ( $\overline{R/C} = 1$ ) or a convert ( $\overline{R/C} = 0$ ) is in progress. The register control inputs  $A_0$  and  $12/\overline{8}$  control conversion length and data format. The  $A_0$  line is usually tied to the least significant bit of the address bus. If a conversion is started with  $A_0$  low, a full 12-bit conversion cycle is initiated. If  $A_0$  is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations,  $A_0$  determines whether the three-state buffers containing the 8 MSBs of the conversion result ( $A_0 = 0$ ) or the 4 LSBs ( $A_0 = 1$ ) are enabled. The  $12/\overline{8}$  pin determines whether the output data is to be organized as two 8-bit words ( $12/\overline{8}$  tied to DIGITAL COMMON) or a single 12-bit word ( $12/\overline{8}$  tied to  $V_{\text{LOGIC}}$ ). The  $12/\overline{8}$  pin is not TTL-compatible and must be hard-wired to either  $V_{\text{LOGIC}}$  or DIGITAL COMMON. In the 8-bit mode, the byte addressed when  $A_0$  is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that  $A_0$  change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.



NOTE 1: WHEN START CONVERT GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12-BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2:  $12/\overline{8}$  IS NOT A TTL-COMPATIBLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO  $V_{\text{LOGIC}}$  OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

Table I. AD574A Truth Table

| CE | $\overline{CS}$ | $\overline{R/C}$ | $12/\overline{8}$ | $A_0$ | Operation                         |
|----|-----------------|------------------|-------------------|-------|-----------------------------------|
| 0  | X               | X                | X                 | X     | None                              |
| X  | 1               | X                | X                 | X     | None                              |
| 1  | 0               | 0                | X                 | 0     | Initiate 12-Bit Conversion        |
| 1  | 0               | 0                | X                 | 1     | Initiate 8-Bit Conversion         |
| 1  | 0               | 1                | Pin 1             | X     | Enable 12-Bit Parallel Output     |
| 1  | 0               | 1                | Pin 15            | 0     | Enable 8 Most Significant Bits    |
| 1  | 0               | 1                | Pin 15            | 1     | Enable 4 LSBs + 4 Trailing Zeroes |

## TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD574A control signals should provide the system designer with useful insight into the operation of the device.

Table II. Convert Start Timing—Full Control Mode

| Symbol           | Parameter                           | Min | Typ | Max | Units         |
|------------------|-------------------------------------|-----|-----|-----|---------------|
| $t_{\text{DSC}}$ | STS Delay from CE                   |     |     | 400 | ns            |
| $t_{\text{HEC}}$ | CE Pulse Width                      | 300 |     |     | ns            |
| $t_{\text{SSC}}$ | $\overline{CS}$ to CE Setup         | 300 |     |     | ns            |
| $t_{\text{HSC}}$ | $\overline{CS}$ Low During CE High  | 200 |     |     | ns            |
| $t_{\text{SRC}}$ | $\overline{R/C}$ to CE Setup        | 250 |     |     | ns            |
| $t_{\text{HRC}}$ | $\overline{R/C}$ Low During CE High | 200 |     |     | ns            |
| $t_{\text{SAC}}$ | $A_0$ to CE Setup                   | 0   |     |     | ns            |
| $t_{\text{HAC}}$ | $A_0$ Valid During CE High          | 300 |     |     | ns            |
| $t_{\text{C}}$   | Conversion Time                     |     |     |     |               |
|                  | 8-Bit Cycle                         | 10  |     | 24  | $\mu\text{s}$ |
|                  | 12-Bit Cycle                        | 15  |     | 35  | $\mu\text{s}$ |



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to valid logic levels after the conversion cycle is completed. The STS line goes high 600 ns after R/C goes low and returns low 300 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 12, the data lines are enabled during the time when R/C is high. The falling edge of R/C starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/C.

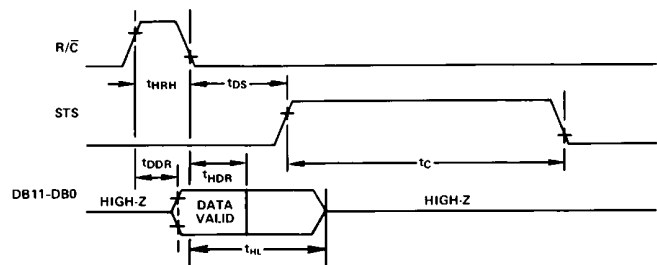


Figure 12. High Pulse for R/C—Outputs Enabled While R/C High, Otherwise High-Z

Table IV. Stand-Alone Mode Timing

| Symbol           | Parameter                  | Min | Typ  | Max | Units |
|------------------|----------------------------|-----|------|-----|-------|
| t <sub>HRL</sub> | Low R/C Pulse Width        | 250 |      |     | ns    |
| t <sub>DS</sub>  | STS Delay from R/C         |     | 600  |     | ns    |
| t <sub>HDR</sub> | Data Valid After R/C Low   | 25  |      |     | ns    |
| t <sub>HL</sub>  | Output Float Delay         |     | 150  |     | ns    |
| t <sub>HS</sub>  | STS Delay After Data Valid | 300 | 1000 |     | ns    |
| t <sub>HRH</sub> | High R/C Pulse Width       | 300 |      |     | ns    |
| t <sub>DDR</sub> | Data Access Time           |     | 250  |     | ns    |

Usually the low pulse for R/C stand-alone mode will be used. Figure 13 illustrates a typical stand-alone configuration for 8086 type processors. The addition of the 74F/S374 latches improves bus access/release times and helps minimize digital feedthrough to the analog portion of the converter.

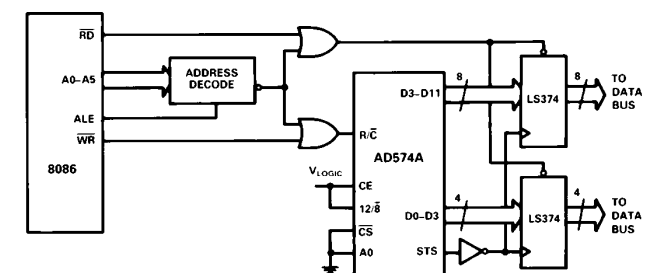


Figure 13. 8086 Stand-Alone Configuration

**INTERFACING THE AD574A TO MICROPROCESSORS**  
The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of “do-nothing” instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/8 input. In 16-bit bus applications (12/8 high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/8 low) is done in a left-justified format. The even address (A0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD574A data lines for right justified 8-bit bus interface.

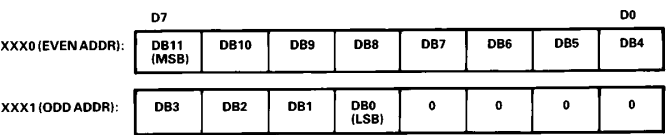


Figure 14. AD574A Data Format for 8-Bit Bus

SPECIFIC PROCESSOR INTERFACE EXAMPLES

Z-80 System Interface

The AD574A may be interfaced to the Z-80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O or mapped configuration. The Z-80 uses address lines A0-A7 to decode the I/O port address.

An interesting feature of the Z-80 is that during I/O operations a single wait state is automatically inserted, allowing the AD574A to be used with Z-80 processors having clock speeds up to 4MHz. For applications faster than 4 MHz use the wait state generator in Figure 16. In a memory mapped configuration the AD574A may be interfaced to Z-80 processors with clock speeds of up to 2.5 MHz.

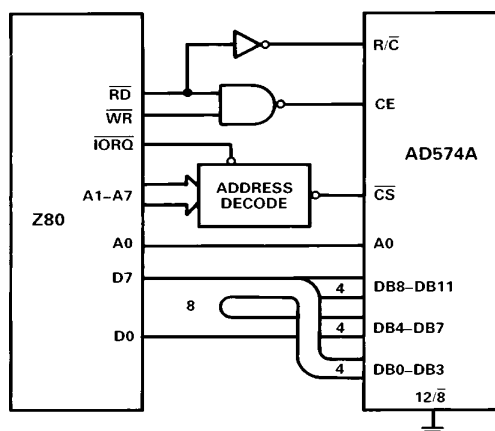


Figure 15. Z80—AD574A Interface

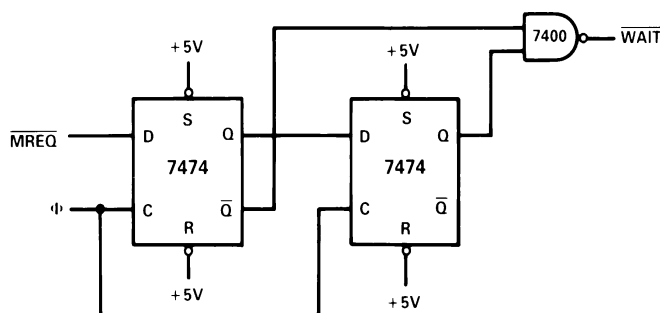


Figure 16. Wait State Generator

## IBM PC Interface

The AD574A appears in Figure 17 interfaced to the 4 MHz 8088 processor of an IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal DMA cycles which use the same I/O address space. This active low signal is applied to  $\overline{CS}$ .  $\overline{IOR}$  and  $\overline{IOW}$  are used to initiate the conversion and read, and are gated together to drive the chip enable, CE. Because the data bus width is limited to 8 bits, the AD574A data resides in two adjacent addresses selected by A0.

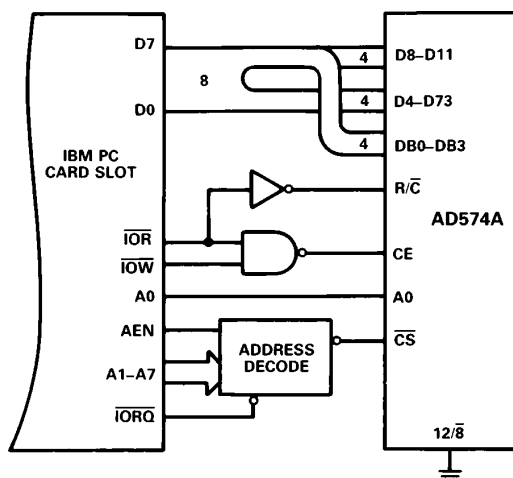


Figure 17. IBM PC—AD574A Interface

Note: Due to the large number of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD574As to the I/O bus.

## 8086 Interface

The data mode select pin ( $12/\overline{8}$ ) of the AD574A should be connected to  $V_{\text{LOGIC}}$  to provide a 12-bit data output. To prevent possible bus contention, a demultiplexed and buffered address/data bus is recommended. In the cases where the 8-bit short conversion cycle is not used, A0 should be tied to digital common. Figure 18 shows a typical 8086 configuration.

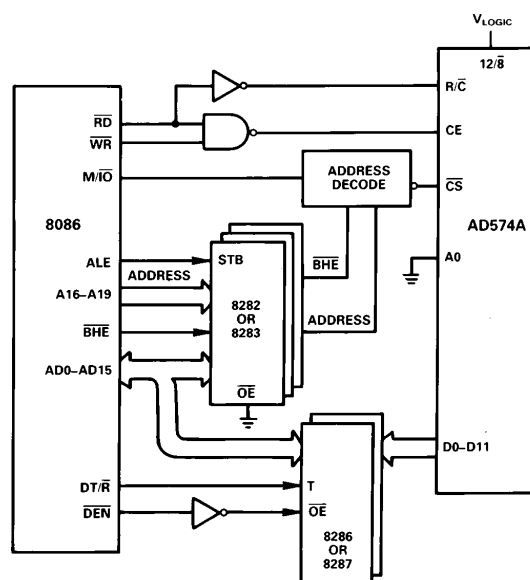


Figure 18. 8086—AD574A with Buffered Bus Interface

For clock speeds greater than 4 MHz wait state insertion similar to Figure 16 is recommended to ensure sufficient CE and R/C pulse duration.

The AD574A can also be interfaced in a stand-alone mode (see Figure 13). A low going pulse derived from the 8086's  $\overline{WR}$  signal logically ORed with a low address decode starts the conversion. At the end of the conversion, STS clocks the data into the three-state latches.

## 68000 Interface

The AD574, when configured in the stand-alone mode, will easily interface to the 4 MHz version of the 68000 microprocessor. The 68000 R/W signal combined with a low address decode initiates conversion. The  $\overline{UDS}$  or  $\overline{LDS}$  signal, with the decoded address, generates the  $\overline{DTACK}$  input to the processor, latching in the AD574A's data. Figure 19 illustrates this configuration.

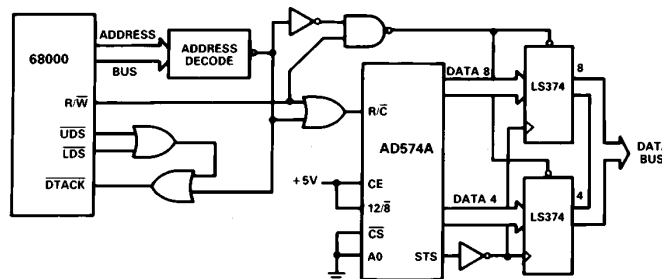


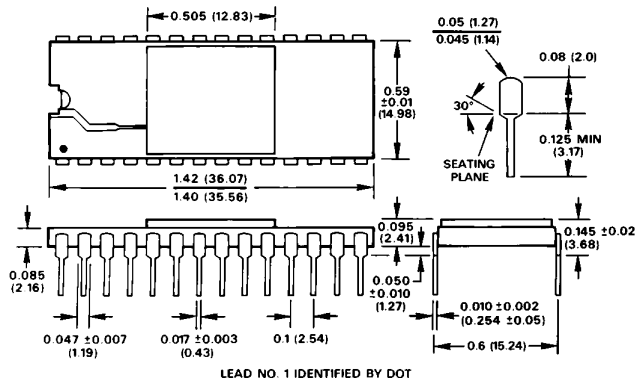
Figure 19. 68000—AD574A Interface

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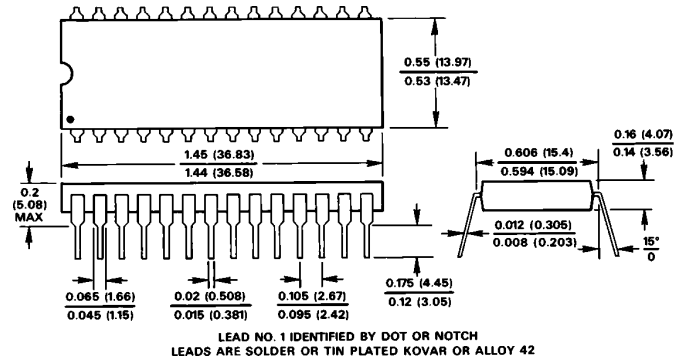
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

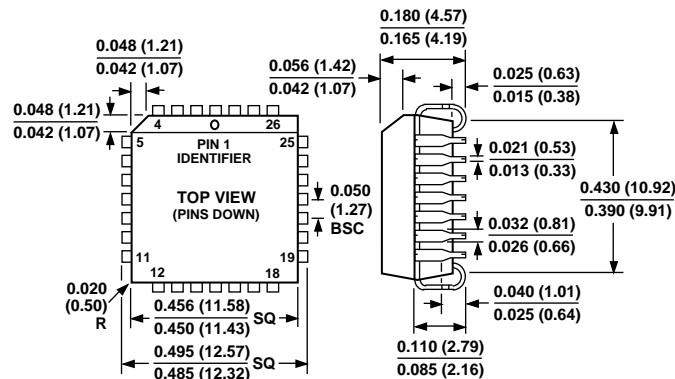
28-Pin Ceramic DIP Package (D-28)



28-Lead Plastic DIP Package (N-28A)



28-Terminal PLCC Package (P-28A)



28-Terminal LCC Package (E-28A)

