



ADC674A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR ADC574A/674A-TYPE A/D CONVERTERS
Conversion Time: 15 μ s max
Bus Access Time: 150ns max
A₀ Input: Bus Contention During Read Operation Eliminated
- FULLY SPECIFIED FOR OPERATION ON ± 12 V OR ± 15 V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE:
0°C to +75°C ADC674AJH, KH, JP, KP Grades
-55°C to +125°C (ADC674ASH, TH Grades)

DESCRIPTION

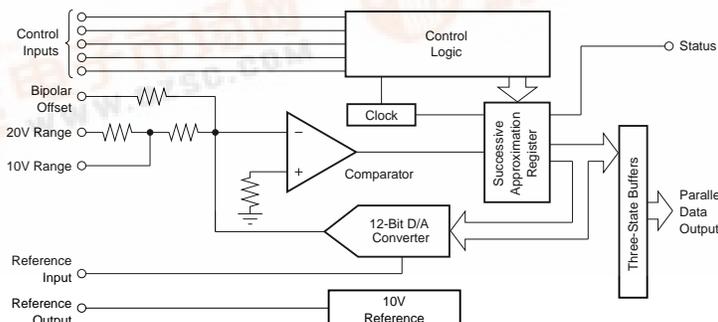
The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ± 5 V, and ± 10 V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15 μ s maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ± 12 V or ± 15 V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_{EE} = -12\text{V}$ or -15VDC , and $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise noted.

PARAMETER	ADC674AJP, JH, SH			ADC674AKP, KH, TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
ANALOG INPUTS Voltage Ranges: Unipolar Bipolar Impedance: 0 to +10V, $\pm 5\text{V}$ $\pm 10\text{V}$, 0V to +20V		0 to +10, 0 to +20 ± 5 , ± 10			*	*	V V k Ω k Ω
DIGITAL INPUTS (CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O , 12/8) Over Temperature Range Voltages: Logic 1 Logic 0 Current Capacitance	+2 -0.5 -5		± 5.5 ± 0.8 ± 5	*	*	*	V V μA pF
TRANSFER CHARACTERISTICS ACCURACY At +25°C Linearity Error Unipolar Offset Error (adjustable to zero) Bipolar Offset Error (adjustable to zero) Full-Scale Calibration Error ⁽¹⁾ (adjustable to zero) No Missing Codes Resolution (differential linearity) Inherent Quantization Error T_{MIN} to T_{MAX} Linearity Error: J, K Grades S, T Grades Full-Scale Calibration Error Without Initial Adjustmen ⁽¹⁾ : J, K Grades S, T Grades Adjusted to zero at +25°C: J, K Grades S, T Grades No Missing Codes Resolution (differential linearity)	11	$\pm 1/2$	± 1 ± 2 ± 10 ± 0.25 ± 1 ± 1 ± 0.47 ± 0.75 ± 0.22 ± 0.5	12	*	$\pm 1/2$ * ± 4 * $\pm 1/2$ $\pm 3/4$ ± 0.37 ± 0.5 ± 0.12 ± 0.25	LSB LSB LSB % of FS ⁽²⁾ Bits LSB LSB LSB % of FS % of FS % of FS % of FS Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX}) ⁽³⁾ Unipolar Offset: J, K Grades S, T Grades Max Change: All Grades Bipolar Offset: All Grades Max Change: J, K Grades S, T Grades Full-Scale Calibration: J, K Grades S, T Grades Max Change: J, K Grades S, T Grades			± 10 ± 5 ± 2 ± 10 ± 2 ± 4 ± 45 ± 50 ± 9 ± 20			± 5 ± 2.5 ± 1 ± 5 ± 1 ± 2 ± 25 ± 25 ± 5 ± 10	ppm/°C ppm/°C LSB ppm/°C LSB LSB ppm/°C ppm/°C LSB LSB
POWER SENSITIVITY Change in Full-Scale Calibration +13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V +16.5V < V_{EE} < +13.5V or -12.6V < V_{EE} < -11.4V +4.5V < V_{LOGIC} < +5.5V			± 2 ± 2 $\pm 1/2$			± 1 ± 1 *	LSB LSB LSB
CONVERSION TIME ⁽⁴⁾ 8-Bit Cycle 12-Bit Cycle	6 9	8 12	10 15	*	*	*	μs μs
DIGITAL OUTPUT (DB ₁₁ —DB ₀ , Status) (Over Temperature Range) Outputs Codes: Unipolar Bipolar Logic Levels: Logic 0 ($I_{\text{SINK}} = 1.6\text{mA}$) Logic 1 ($I_{\text{SOURCE}} = 500\mu\text{A}$) Leakage, Data Bits Only, High-Z State Capacitance	+2.4 -5		Unipolar Straight Binary (USB) Bipolar Offset Binary (BOB) +0.4 +5	*	*	*	V V μA pF
INTERNAL REFERENCE VOLTAGE Voltage Source Current Available for External Loads ⁽⁵⁾	+9.9 2	± 10	± 10.1	*	*	*	V mA

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_{EE} = -12\text{V}$ or -15VDC , and $V_{LOGIC} = +5\text{V}$, unless otherwise noted.

PARAMETER	ADC674AJP, AJH, ASH			ADC674AKP, AKH, ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}		+11.4	*		*	V	
V_{EE}	-11.4		-16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation ($\pm 15\text{V}$ Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN} , T_{MAX})							
Specification: K, J Grades	0		+75	*		*	$^\circ\text{C}$
S, T Grades	-55		+125	*		*	$^\circ\text{C}$
Storage	-65		+150	*		*	$^\circ\text{C}$

* Specifications same as ADC674AJP, AJH, ASH.

NOTES: (1) With fixed 50 Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at $+25^\circ\text{C}$ (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a $\pm 10\text{V}$ input range, FS means 20 V; for a 0 to $+10\text{V}$ range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendor's 674A type specification tables. (3) Using internal reference. (4) See Controlling the ADC674A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either $\pm 12\text{V}$ or $\pm 15\text{V}$ power supplies.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0 to $+16.5\text{V}$
V_{EE} to Digital Common	0 to -16.5V
V_{LOGIC} to Digital Common	0 to $+7\text{V}$
Analog Common to Digital Common	$\pm 1\text{V}$
Control Inputs (CE, $\overline{\text{CS}}$, A_0 , 12/ $\overline{\text{B}}$, R/ $\overline{\text{C}}$)	
to Digital Common	-0.5V to $V_{LOGIC} + 0.5\text{V}$
Analog Inputs REF IN, BIP. OFF., $10V_{IN}$)	
to Analog Common	$\pm 16.5\text{V}$
$20V_{IN}$ to Analog Common	$\pm 24\text{V}$
REF OUT	Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature	$+165^\circ\text{C}$
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Thermal Resistance, θ_{JA} : Ceramic	50°C/W
Plastic	100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC674As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic “-BI” models: $+85^\circ\text{C}$

Ceramic “-BI” models: $+125^\circ\text{C}$

All units are 100% electrically tested after burn-in is completed. To order burn-in, add “-BI” to the base model number (e.g., ADC674AKP-BI).

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR max (T_{MIN} to T_{MAX})
ADC674AJP	Plastic DIP	0°C to $+75^\circ\text{C}$	$\pm 1\text{LSB}$
ADC674AKP	Plastic DIP	0°C to $+75^\circ\text{C}$	$\pm 1/2\text{LSB}$
ADC674AJH	Ceramic DIP	0°C to $+75^\circ\text{C}$	$\pm 1\text{LSB}$
ADC674AKH	Ceramic DIP	0°C to $+75^\circ\text{C}$	$\pm 1/2\text{LSB}$
ADC674ASH	Ceramic DIP	-55°C to $+125^\circ\text{C}$	$\pm 1\text{LSB}$
ADC674ATH	Ceramic DIP	-55°C to $+125^\circ\text{C}$	$\pm 3/4\text{LSB}$

BURN-IN SCREENING OPTION

See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMPERATURE (160 Hours) ⁽¹⁾
ADC674AJP-BI	Plastic DIP	0°C to $+75^\circ\text{C}$	$+85^\circ\text{C}$
ADC674AKP-BI	Plastic DIP	0°C to $+75^\circ\text{C}$	$+85^\circ\text{C}$
ADC674AJH-BI	Ceramic DIP	0°C to $+75^\circ\text{C}$	$+125^\circ\text{C}$
ADC674AKH-BI	Ceramic DIP	0°C to $+75^\circ\text{C}$	$+125^\circ\text{C}$
ADC674ASH-BI	Ceramic DIP	-55°C to $+125^\circ\text{C}$	$+125^\circ\text{C}$
ADC674ATH-BI	Ceramic DIP	-55°C to $+125^\circ\text{C}$	$+125^\circ\text{C}$

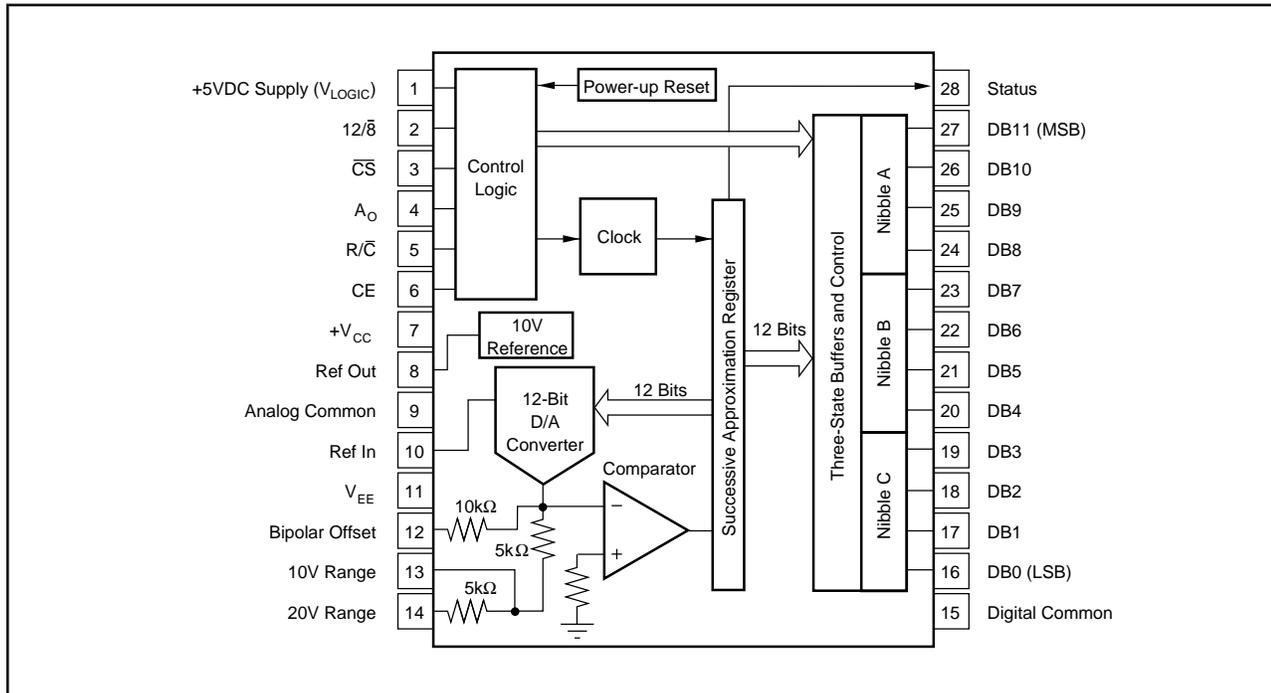
NOTE: (1) Or equivalent combination of time and temperature.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ADC674AJP	Plastic DIP	215
ADC674AKP	Plastic DIP	215
ADC674AJH	Ceramic DIP	149
ADC674AKH	Ceramic DIP	149
ADC674ASH	Ceramic DIP	149
ADC674ATH	Ceramic DIP	149
ADC674AJP-BI	Plastic DIP	215
ADC674AKP-BI	Plastic DIP	215
ADC674AJH-BI	Ceramic DIP	149
ADC674AKH-BI	Ceramic DIP	149
ADC674ASH-BI	Ceramic DIP	149
ADC674ATH-BI	Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/\bar{C} input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs ($12/\bar{8}$, $\bar{C}\bar{S}$, A_0 , R/\bar{C} , and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table I. The control function truth table is listed in Table II.

CE	$\bar{C}\bar{S}$	R/\bar{C}	$12/\bar{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. Control Input Truth Table.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\bar{C}\bar{S}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/\bar{C} (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit ($A_0 = "1"$) or 12-bit ($A_0 = "0"$) conversion mode. When reading output data in two 8-bit bytes, $A_0 = "0"$ accesses ± 8 MSBs (high byte) and $A_0 = "1"$ accesses 4LSBs and trailing "0s" (low byte).
$12/\bar{8}$ (Pin 2)	Data Mode Select ("1" = 12-bits) ("0" = 8-bits)	When reading output data, $12/\bar{8} = "1"$ enables all 12 output bits simultaneously. $12/\bar{8} = "0"$ will enable the MSBs or LSBs as determined by the A_0 line.

TABLE I. ADC674A Control Line Functions.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/\bar{C} . In this mode $\bar{C}\bar{S}$ and A_0 are connected to digital common and CE and $12/\bar{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/\bar{C} . The three-state data output buffers are enabled when R/\bar{C} is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case, the R/\bar{C} pulse must remain low for a minimum of 50ns.

Figure 1 illustrates timing when conversion is initiated by an R/\bar{C} pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/\bar{C} and are enabled for external access of the data after completion of the conversion. Figure 2 illustrates the timing when conversion is initiated by a positive R/\bar{C} pulse. In this mode, the output data from the previous conversion is enabled during the positive portion of R/\bar{C} . A new conversion is started on the falling edge of R/\bar{C} , and the three-state outputs return to the high impedance state until the next occurrence of a high R/\bar{C} pulse. Timing specifications for stand-alone operation are listed in Table III.

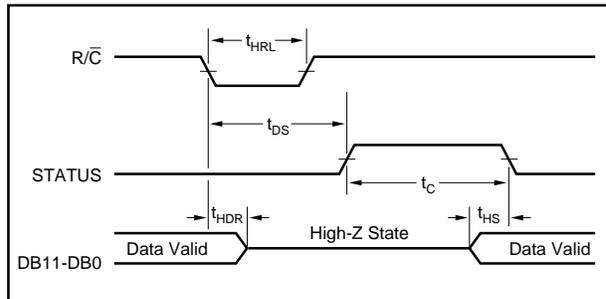


FIGURE 1. R/\bar{C} Pulse Low—Outputs Enabled After Conversions.

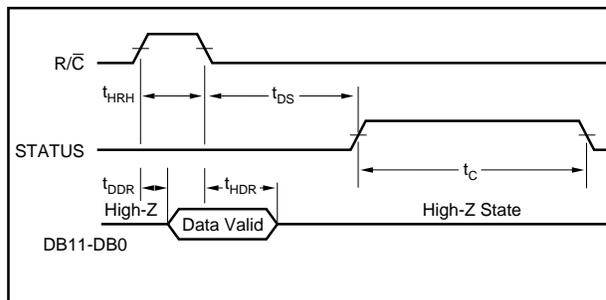


FIGURE 2. R/\bar{C} Pulse High—Outputs Enabled Only While R/\bar{C} is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/\bar{C} Pulse Width	50			ns
t_{DS}	STS Delay from R/\bar{C}			200	ns
t_{HDR}	Data Valid After R/\bar{C} Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/\bar{C} Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE III. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion the 3LSBs (DB0 - DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\bar{C}\bar{S}$, and R/\bar{C}) as shown in Table II. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 3. The specifications for timing are contained in Table IV.

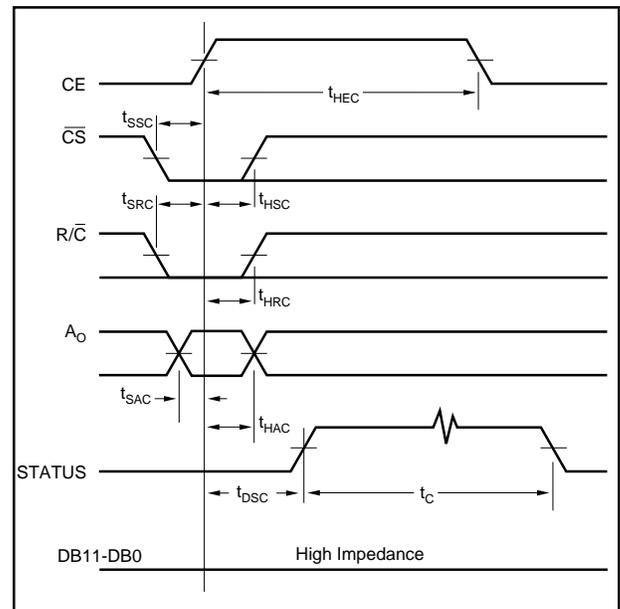


FIGURE 3. Conversion Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	\overline{CS} to CE Setup	50	20		ns
t_{HSC}	\overline{CS} Low During CE High	50	20		ns
t_{SRC}	R/ \overline{C} to CE Setup	50	0		ns
t_{HRC}	R/ \overline{C} Low During CE High	50	20		ns
t_{SAC}	A ₀ To CE Setup	0			ns
t_{HAC}	A ₀ Valid During CE high	50	20		ns
t_c	Conversion Time, 12 Bit Cycle	9	12	15	μ s
	8 Bit Cycle	6	8	10	μ s
Read Mode					
t_{DD}	Access Time From CE		75	150	ns
t_{HD}	Data Valid After CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	\overline{CS} to CE Setup	50	0		ns
t_{SRR}	R/ \overline{C} to CE Setup	0			ns
t_{SAR}	A ₀ to CE Setup	50	25		ns
t_{HSR}	\overline{CS} Valid After CE Low		0		ns
t_{HRR}	R/ \overline{C} high After CE Low		0		ns
t_{HAR}	A ₀ Valid After CE Low		50		ns
t_{HS}	STS delay After Data Valid	100	300	600	ns

NOTE: Specifications are at + 25°C and measured at 50% level of transitions.

TABLE IV. Timing Specifications

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A₀ changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A₀, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/ \overline{C} high, STATUS low, CE high, and \overline{CS} low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/ $\overline{8}$ and A₀. See Figure 4 and Table IV for timing relationships and specifications.

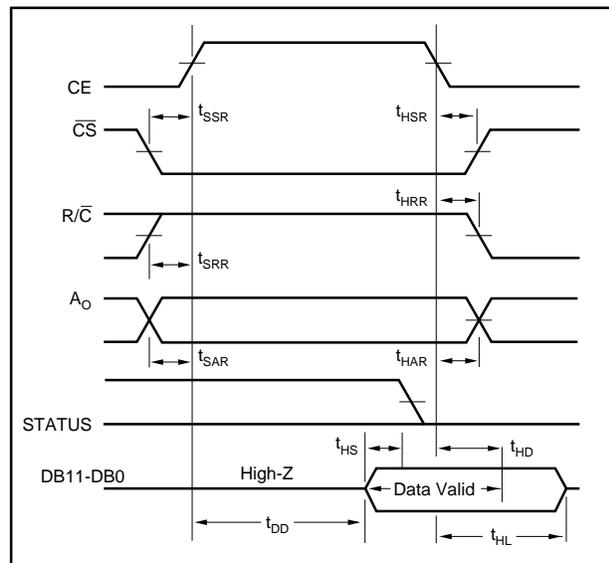


FIGURE 4. Read Cycle Timing.

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