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National Semiconductor

February 2001

CLC114
Quad, Low Power Video Buffer

General Description

The CLC114 is a high performance, close loop quad buffer intended for power sensitive applications. Requiring only 30mW of quiescent power dissipation per channel (±5V supplies), the CLC114 offers a small signal bandwidth of 200MHz (0.5Vpp) and a slew rate of 450V/µs.

Designed specifically for high density crosspoint switch and analog multiplexer applications, the CLC114 offers excellent linearity and wide channel isolation (62dB @ 10MHz). Driving a typical crosspoint switch load, the CLC114 offers differential gain and phase performance of 0.08% and 0.1% gain flatness through 30MHz is typically 0.1dB.

With its patented closed loop topology , the CLC114 has significant performance advantages over conventional open loop designs. Applications requiring low output impedance and true unity gain stability through very high frequencies (active filters, dynamic load buffering, etc.) Will benefit from the CLC114's superior performance.

Constructed using an advanced, complementary bipolar process and National's proven high speed architectures, the CLC114 is available in several versions to meet a variety of requirements.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-92339

*Space level versions also available.

*For more information, visit http://www.national/com/mil

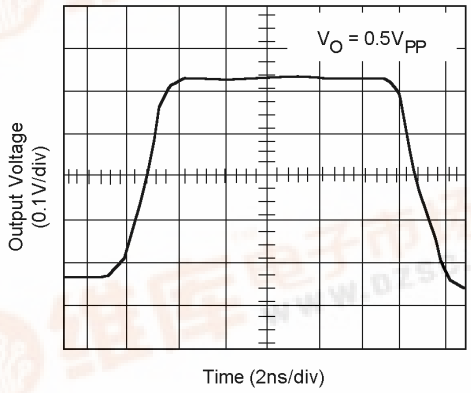
Features

- Closed loop, quad buffer
- 200MHz small signal bandwidth
- 450V/us slew rate
- Low power, 30mW per channel (±5V sup.)
- 62dB channel isolation (10MHz)
- Specified for crosspoint switch loads

Applications

- Video crosspoint switch driver
- Video distribution buffer
- Video switching buffer
- Video signaling multiplexing
- Instrumentation amps
- Active filters

Small Signal Pulse Response



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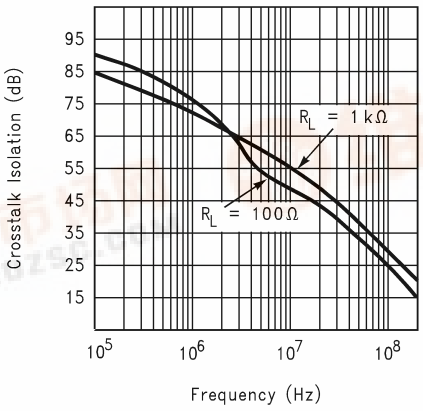
Typical Application



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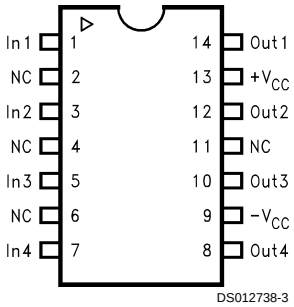
Connection Diagram



Pinout

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-Pin Plastic DIP	−40˚C to +85˚C	CLC114AJP	CLC114AJP	N14A
14-Pin Plastic SOIC	−40˚C to +85˚C	CLC114AJE	CLC114AJE	M14A,B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	30mA
Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C
ESD Rating	500V

Operating Ratings

Thermal Resistance Package	(θ_{JC})	(θ_{JA})
MDIP	65˚C/W	115˚C/W
SOIC	55˚C/W	125˚C/W

Electrical Characteristics

(V_{CC} = ±5 V, R_L = 100Ω; Unless Specified)

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature		CLC114AI	+25˚C	−40˚C	+25˚C	+85˚	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} <0.5V_{PP}	200	>135	>135	>120	MHz
LSBW		V_{OUT}<2V_{PP}	95	>70	>70	>70	MHz
	Gain Flatness	V_{OUT}< 0.5V_{PP}					
GFPL	Peaking	DC to 30MHz	0.0	<0.3	<0.2	<0.3	dB
GFPH	Peaking	30MHz to 200MHz	0.0	<1.3	<0.7	<0.7	dB
GFR	Rolloff	DC to 60MHz	0.1	<0.8	<0.8	<1.0	dB
XT	Crosstalk (All Hostile)	10MHz	62	>58	>58	>60	dB
Time Domain Response							
TRS1	Rise and Fall Time	0.5V Step	1.8	<2.8	<2.8	<3.0	ns
TRS2		2V Step	5	<7	<7	<8	ns
TS1	Settling Time to 0.1%	2V Step	10	<15	<15	<20	ns
TS01	to 0.01%	2V Step	20	<30	<30	<40	ns
OS	Overshoot	0.5V Step	3	<15	<10	<15	%
SR	Slew Rate		450	>180	>200	>180	V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	2V_{PP},20MHz	−50	<−34	<−38	<−38	dBc
HD3	3rd Harmonic Distortion	2V_{PP},20MHz	−58	<−50	<−50	<−45	dBc
SNF	Equivalent Input Noise Noise Floor	>1MHz	−155	<−153	<−153	<−153	dBm_{1Hz}
Static, DC Performance							
GA	Small Signal Gain	100Ω Load	0.97	>0.95	>0.96	>0.96	V/V
ILIN	Integral Endpoint Linearity	±1V, Full Scale	0.4	<1.0	<0.6	<0.5	%
VIO	Output Offset Voltage(Note 3)		±0.5	<±8.2	<±5.0	<±8.0	mV
DVIO	Average Temperature Coefficient		±9.0	<±40	–	<±30	µV/˚C
IBN	Input Bias Current (Note 3)		±1.0	<±10	<±5	<±4	µA
DIBN	Average Temperature Coefficient		±6.0	<±62	–	<±25	nA/˚C
PSRR	Power Supply Rejection Ratio		56	>48	>48	>46	dB
ICC	Supply Current, Total (Note 3)	No Load, Quiescent	12.0	<17.0	<16.5	<16.0	mA
Miscellaneous Performance							
RIN	Input Resistance		1.5	>0.3	>1.0	>2.0	MΩ
CIN	Input Capacitance		1.8	<3.5	<3.0	<3.5	pF
RO	Output Impedance	DC	2.5	<5.0	<3.5	<3.5	Ω
VO	Output Voltage Range	No Load	±4.0	>±3.6	>±3.8	>±3.8	V
IO	Output Current		25	>12	>20	>25	mA

Electrical Characteristics (Continued)

(V_{CC} = ±5 V, R_L = 100Ω; Unless Specified)

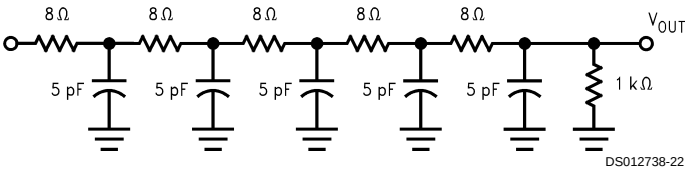
Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Performance Driving a Crosspoint Switch							
	Gain Flatness $V_{OUT} < 2V_{PP}$	DC to 5MHz	±0.02				dB
	Gain Flatness $V_{OUT} < 2V_{PP}$	DC to 30MHZ	±0.1				dB
	Differential Gain	3.58 & 4.43MHz	0.08				%
	Differential Phase	3.58 & 4.43MHz	0.1				deg
	2nd Harmonic Distortion	5MHz,$2V_{PP}$	−60				dBc
		30MHz,$2V_{PP}$	−43				dBc
	3rd Harmonic Distortion	5MHz,$2V_{PP}$	−58				dBc
		30MHz,$2V_{PP}$	−43				dBc
	Crosstalk (All Hostile)	5MHz	58				dB
		10MHz	54				dB
		30MHz	42				dB

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

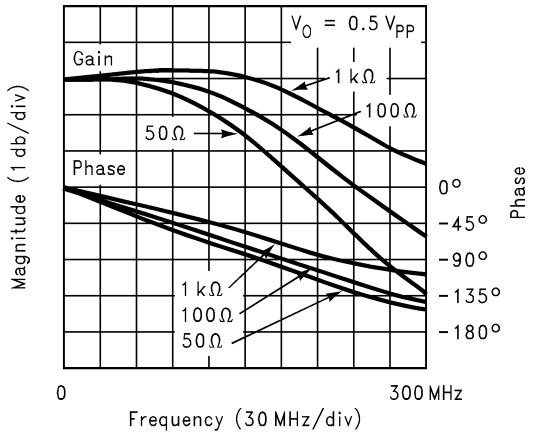
Note 3: AJ-level: spec. is 100% tested at +25˚C.

Test Load



Typical Performance Characteristics

Gain and Phase vs. Load



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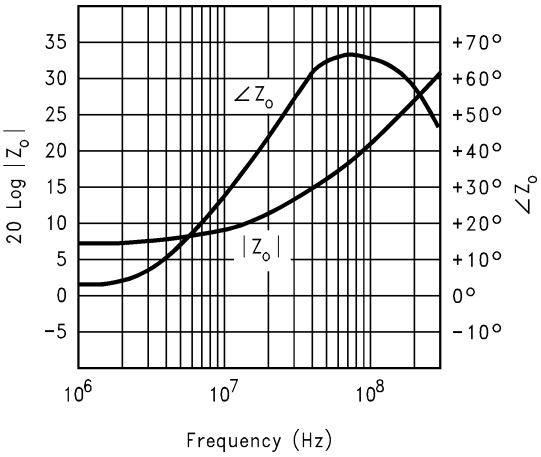
Output Impedance



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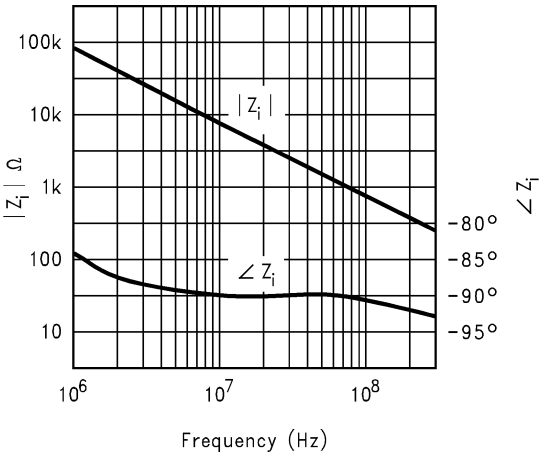
Input Impedance



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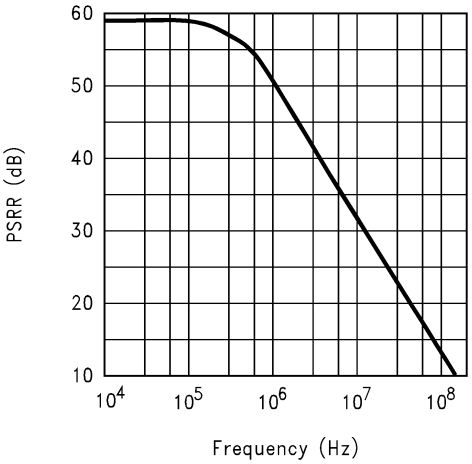
PSRR



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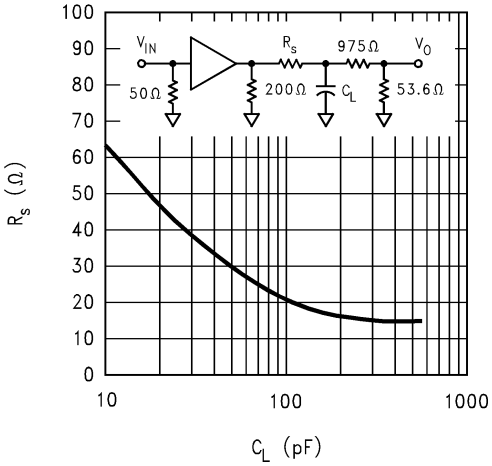
Recommended R_S vs. Load Capacitance



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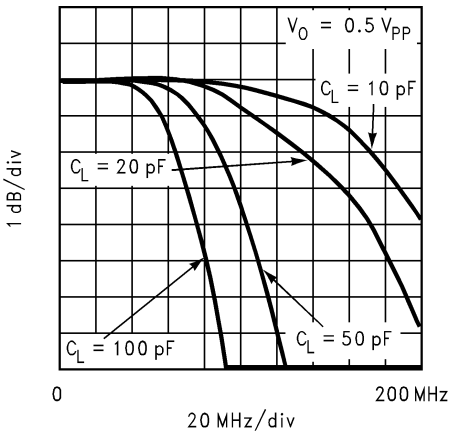
| S_{21}| vs. C_L with Recommended R_S



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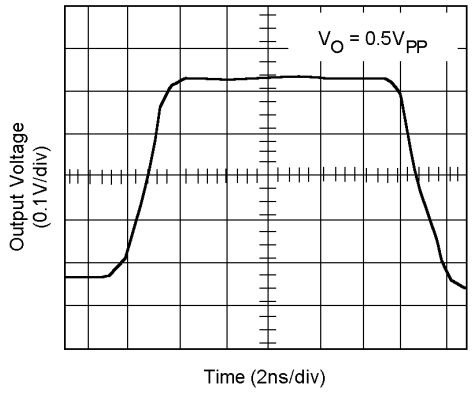
Typical Performance Characteristics (Continued)

Small Signal Pulse Response



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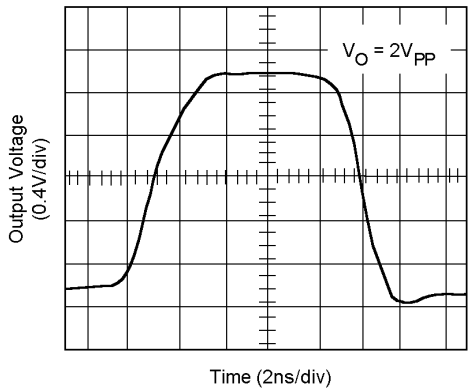
Large Signal Pulse Response



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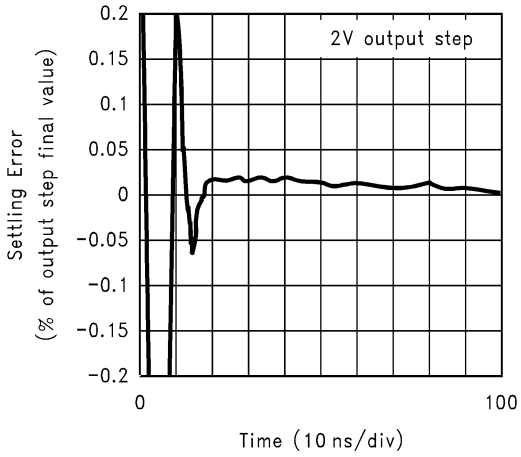
Short-Term Settling Time



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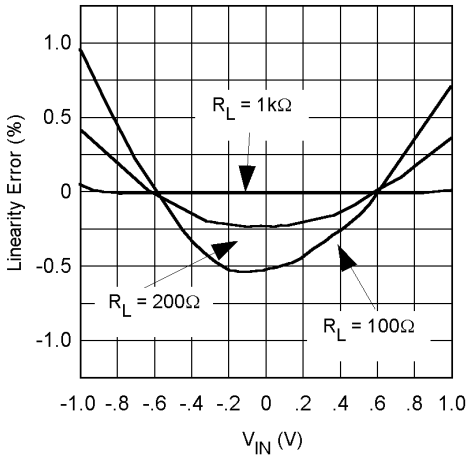
Integral Linearity Error



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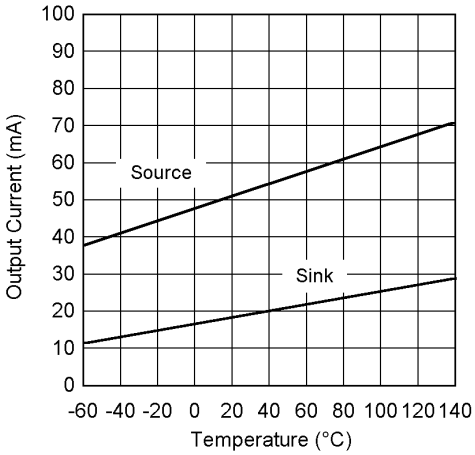
Output Current vs. Temperature



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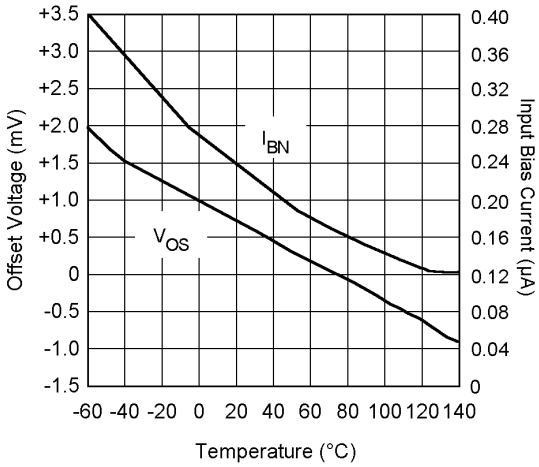
Typical D.C. Errors vs. Temperature



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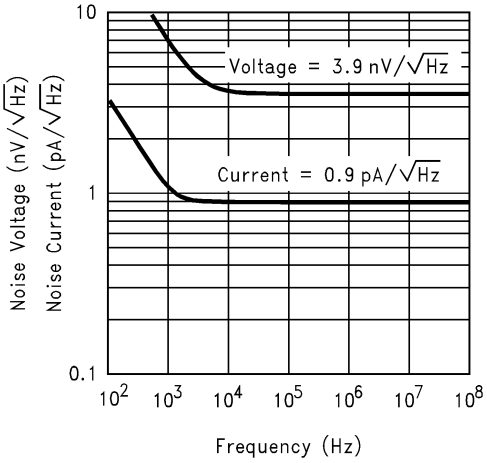
Typical Performance Characteristics (Continued)

Equivalent Input Noise



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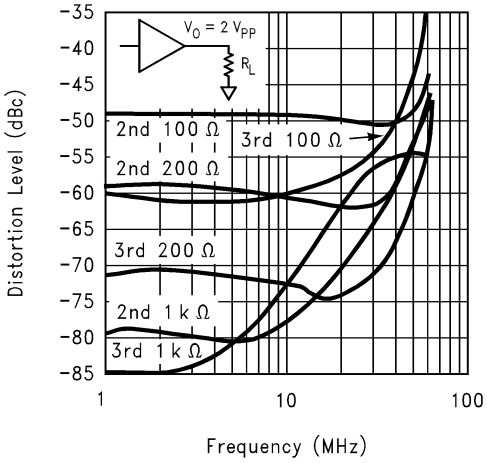
2nd and 3rd Harmonic Distortion



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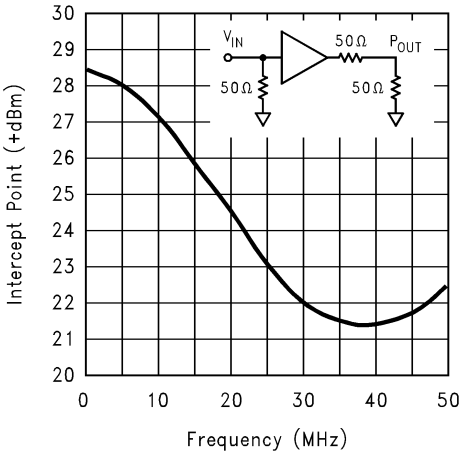
2-Tone, 3rd Order Intermodulation Intercept



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Application Division

Operation

The CLC114 is a quad, low power, high speed, unity gain buffer. The closed loop topology provides accuracy not found in open loop designs. The input stage incorporates a slew enhancement circuit which allows low quiescent power without sacrificing AC performance.

PC Board Layout and Crosstalk

High frequency devices demand a good printed circuit board layout for optimum performance. The CLC114, with power gain to 200 MHz, is no exception. A ground plane and power supply bypassing with good high frequency ceramic capacitors in close proximity to the supply pins is essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies. This can be accomplished by grounding the bypass capacitors at the same point in the ground plane while keeping the power supply side of the bypass capacitors within 0.1" of the CLC114 supply pins.

Crosstalk (undesired signal coupling between buffer channels) is strongly dependent on board layout. Closely spaced signal traces on the circuit board will degrade crosstalk due to interface capacitance. For this reason it is recommended that unused package pins (2, 4, 6, 11) be connected to the ground plane for better channel isolation at the device pins. Similarly, crosstalk can be improved by using a grounded guard trace between signal traces. This will reduce the distributed capacitance between signal lines.

Following are two graphs depicting the effects of crosstalk. All-hostile crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel. *Figure 2*, "All-hostile Crosstalk Isolation", shows this effect as a function of input signal frequency. R_L is the resistive load for each driven channel. *Figure 3*, "Most Susceptible Channel-to-Channel Pulse Coupling", describes one effect of crosstalk when one channel is driven with a $2V_{PP}$ step (tr = 5ns) while the output of the undriven channel is measured. From*Figure 2* it can be observed that crosstalk decreases as the signal frequency is reduced. Similarly, the pulse coupling crosstalk will decrease as the rise time increases.

Evaluation Board

An evaluation board for the CLC114 is available. This board maybe ordered as part CLC730023.

Application Division (Continued)

Unused Buffer

It is recommended that the inputs of any unused buffers be tied to ground through 50Ω resistors.

Differential Gain and Phase

The CLC114 was designed to minimize deferential gain and phase errors when driving the distributed capacitance of a video cross point switch. Refer to the section “Performance Driving a Crosspoint Switch” for typical values.

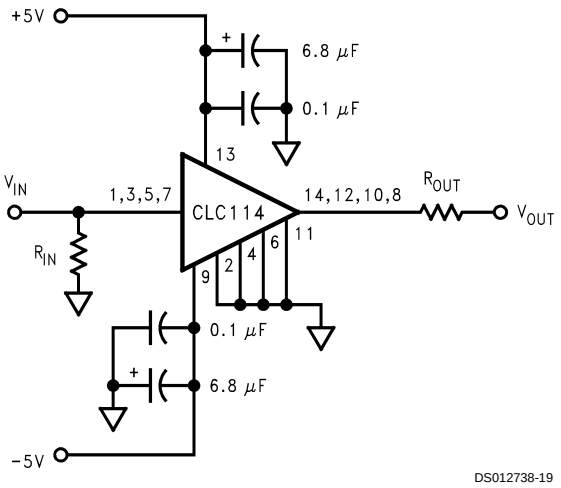


FIGURE 1. Recommended Circuit

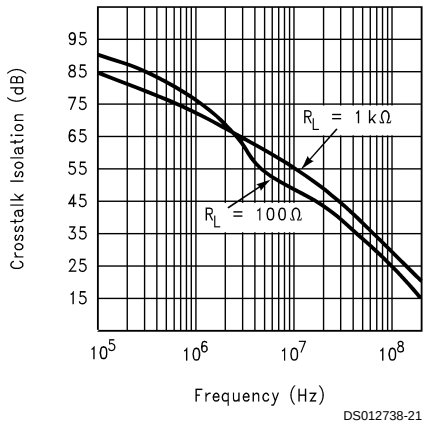


FIGURE 2. All- Hostile Crosstalk Isolation

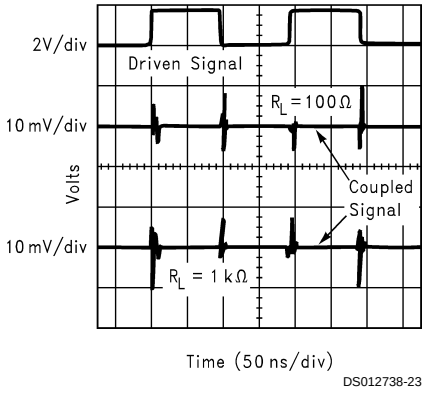
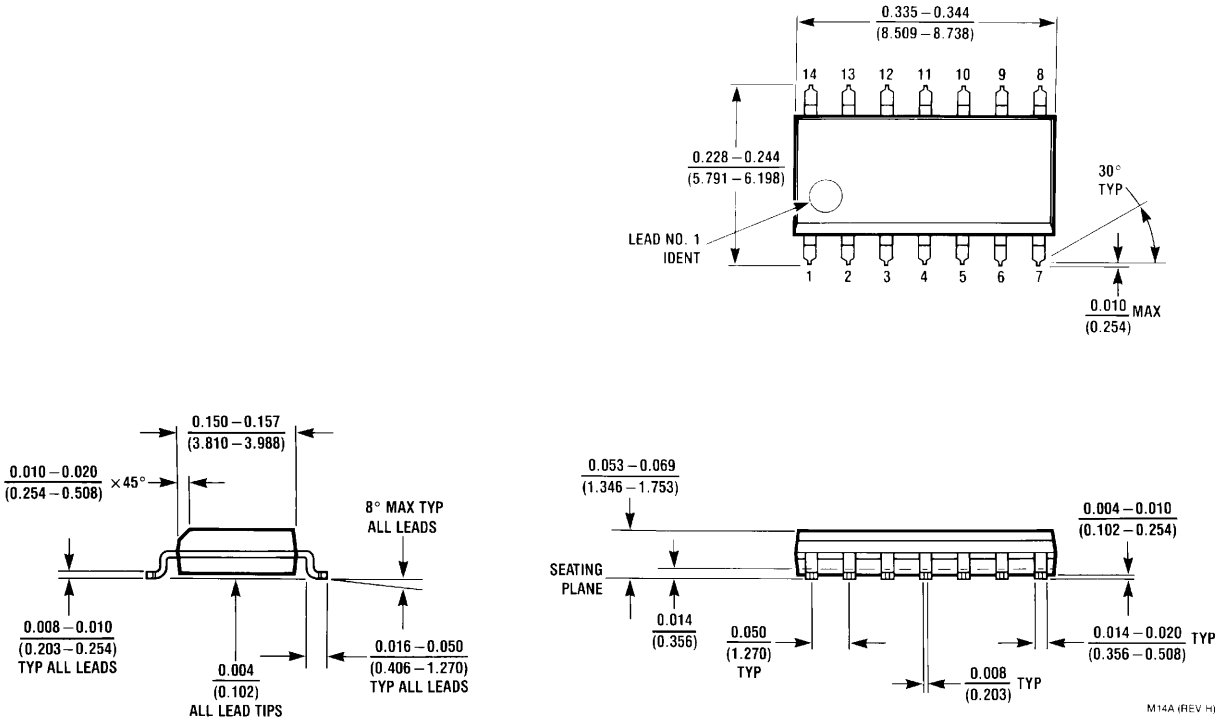
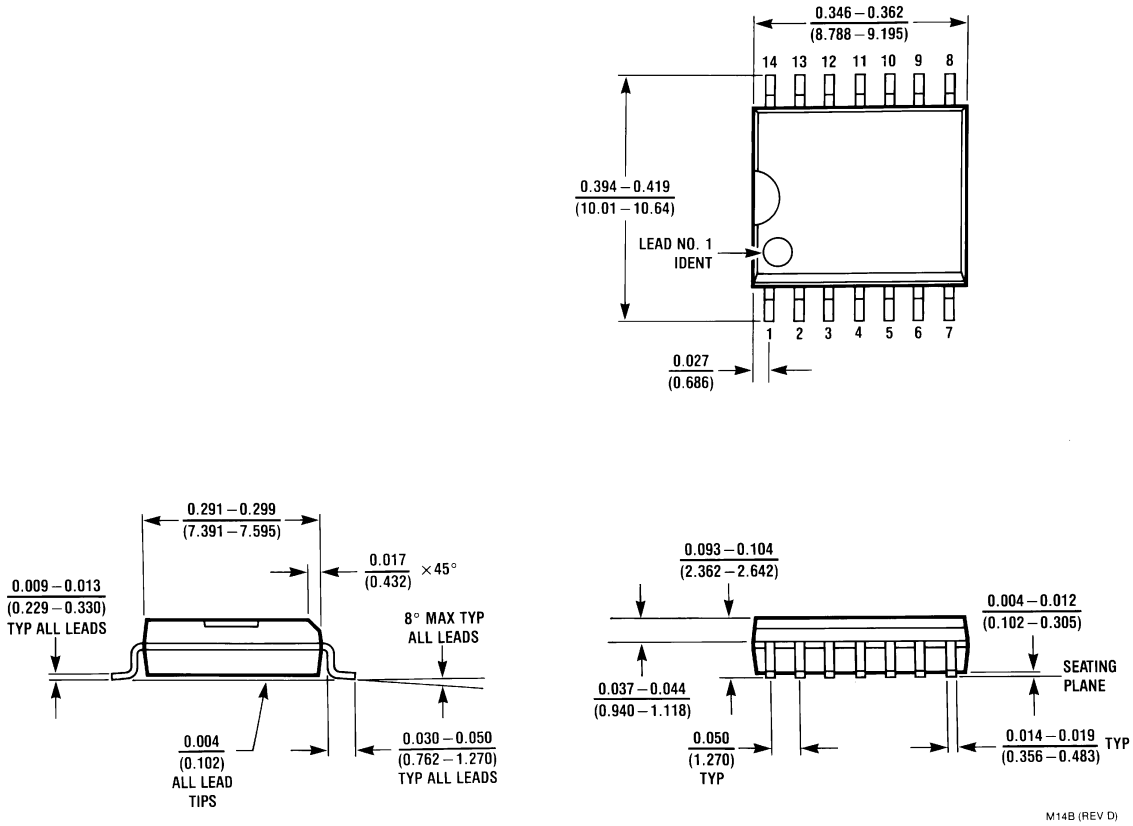


FIGURE 3. Most susceptible Channel-to-Channel Pulse Coupling

Physical Dimensions inches (millimeters) unless otherwise noted

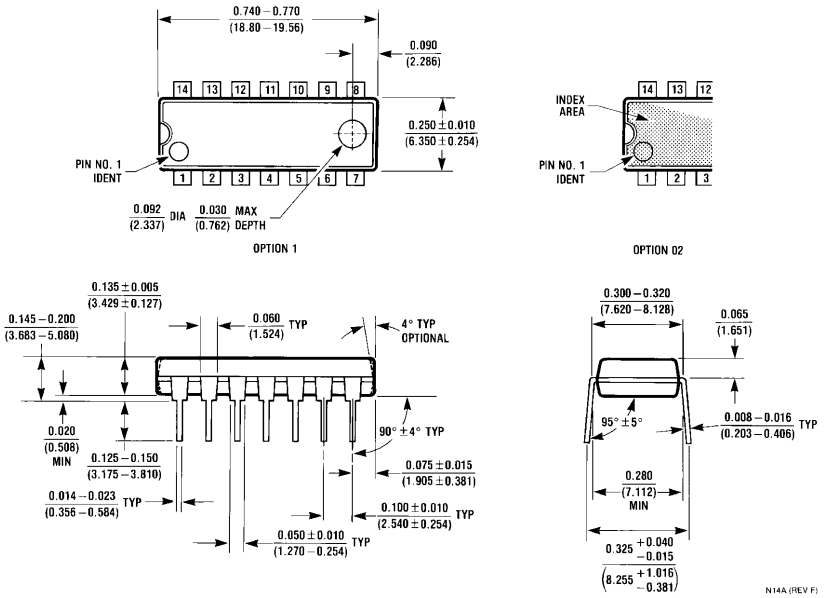


14-Pin SOIC
NS Package Number M14A



14-Pin SOIC
NS Package Number M14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin MDIP
NS Package Number N14A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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