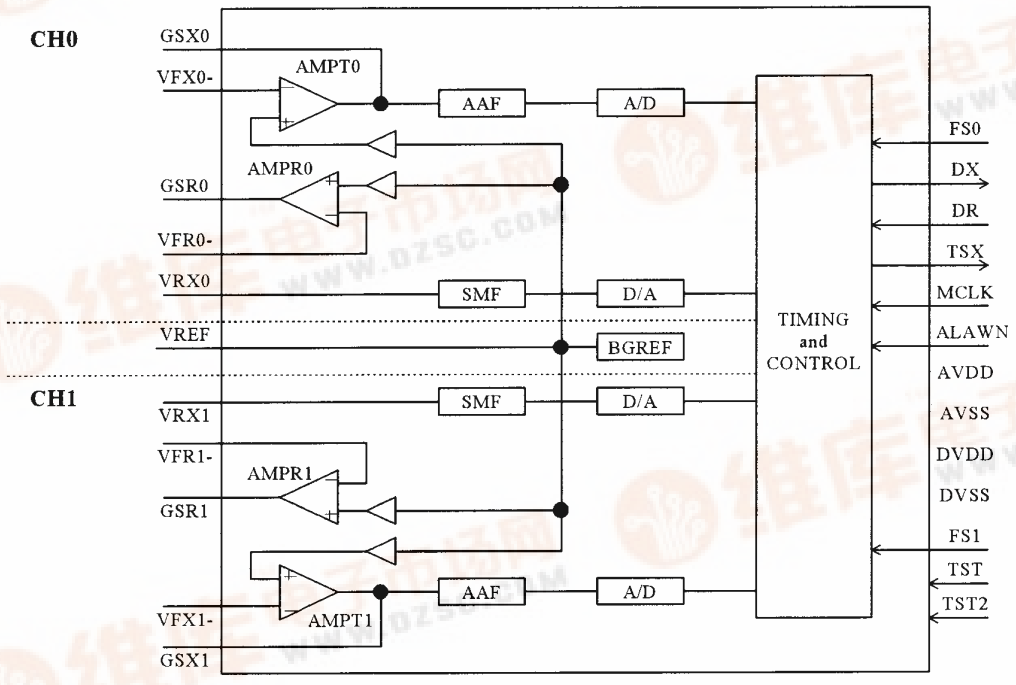
AK2302
Dual PCM Codec/Filter COMBO LSI

Features

- ☐Meets ITU recommendations
- ☐Complete CODEC and filtering system for two telephone lines including
  - free operational amplifier for gain adjustment in both direction
  - internal precision reference voltage
  - antialiasing filtering
  - smoothing filtering
  - sinX/X correction
  - A-law/μ-law pin selectable
  - interface to PCM highway for both channels in common
  - separate frame sync at each channel
- ☐Single +5V±5% operation
- ☐24pin VSOP small package (7.9×7.6mm)
- ☐Auto power save mode
- ☐Power on reset

Block Diagram



General Description

(Description)

□Time Slot Assignment
Some type of time slot assignment is necessary because two channels are sharing a signal PCM data input pin and a output pin.

Synchronous timing for the dual CODEC is defined by either FS0 or FS1 whichever comes first after the device initialization sequence(first FS). Another FS must be delayed from the first one by the multiple of 8 MCLK cycles. FS0 and FS1 must be derived from MCLK, and their periodicity must be 256 MCLK cycles.

Time slot 0 is determined by the slot defined by FS0 or FS1 whichever comes first. If the other channel is to be used, FS for other channel must be delayed from the first by a multiple 8 MCLK cycles.

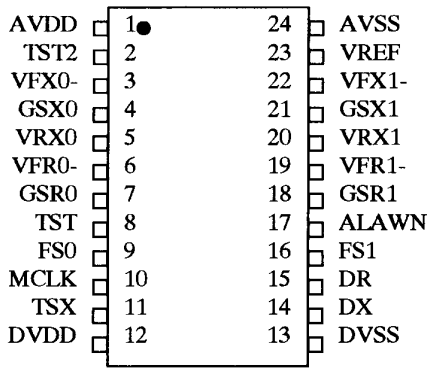
In order to change channel in use and time slot assignment for each channel in use, the device must be reset in power down mode (TST pin low or absence of first FS), before channels and time slots can be selected as described above.

□Power Down
The device goes into power down mode if TST pin is low or the FS0 or FS1 defining slot0, i.e. first FS, is not present more than 4×Ts(=500)μsec. In power down mode, MCLK doesn't need to be input.

□Power on Reset
When power is first applied, power on reset circuitry initializes AK2302. During the 150 ms (typical value) initialization sequence, any input signal on FSn (n=0 or 1) will not be taken notice of ("don't care").

□MCLK
MCLK must be supplied constantly except when the device is in power down mode.

■Pin assignment



Circuit Description

Block	Function
AMPT0,1	Op-amp for input gain adjustment. AK2302 has an op-amp at each analog input. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor lager than 10kΩ is recommended for the feedback resistor.
AMPR0,1	Op-amp for output gain adjustment. AK2302 has an op-amp at each analog output. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor lager than 10kΩ is recommended for the feedback resistor.
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voiceband. AAF is a 2nd order RC low-pass filter.
A/D	Converts analog signal to 8bit PCM data according to the companding schemes of ITU recommendation G.711; A-law or μ-law. The band limiting filter is also integrated. The selection of companding schemes is set by ALAWN pin as follows: "H": μ-Law "L": A-Law
D/A	Expands 8bit PCM data according to A-law or μ-law. The selection of companding schemes is set by ALAWN pin as follows: "H": μ-Law "L": A-Law
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of D/A output.
BGREF	Provides the stable analog ground voltage (2.4V) using an on-chip band-gap reference circuit which is temperature compensated.
TIMING and CONTROL	8bit PCM data of CH0 and CH1 is multiplexed into serial data of 2.048Mb/s at the rising edges of MCLK and comes out from DX. The start bit of transmit PCM data of CH0 and CH1 are defined by FS0 and FS1 respectively. This 3-state output remains in the high impedance state except during the assigned transmit time slot. Receive serial PCM data from DR at the rate of 2.048Mb/s at the falling edges of MCLK is demultiplexed into 2CH serial data. The start bit of receive PCM data of CH0 and CH1 are defined by FS0 and FS1 respectively. The received data is divided into 8bit blocks and sent to CH0 and CH1 sequentially.

Pin/Function

Pin#	Name	I/O	Function	Remarks
1	AVDD	-	Analog positive supply voltage. Systems analog +5V supply.	
2	TST2	I	Test pin. Tie to logic high for normal operation. The device enters test mode with TST2 low.	
3	VFX0-	I	Transmit analog input. Inverting input of transmit input amplifier for channel 0.	
4	GSX0	O	Output of transmit input amplifier for channel 0.	
5	VRX0	O	Receive analog output of SMF for channel 0. This output can drive 10kΩ or larger, and 50pF or smaller.	
6	VFR0-	I	Inverting input of receive output amplifier for channel 0.	
7	GSR0	O	Output of receive output amplifier for channel 0.	
8	TST	I	Test (Power down) pin. Tie to logic high for normal operation. The device enters power down mode with TST low.	
9	FS0	I	Frame sync input for channel 0. FS0 must be derived from MCLK, and its periodicity must be 256 MCLK cycles.	
10	MCLK	I	Master clock 2.048MHz input.	
11	TSX	O	Open drain output. Pulsing low during digital transmission cycles.	
12	DVDD	-	Digital positive supply voltage. System digital +5V supply.	
13	DVSS	-	Digital negative supply voltage. System digital ground.	
14	DX	O	Serial output of 2.048Mb/s PCM data. The PCM data is shifted out at the rising edges of MCLK. The start bit of transmit PCM data is defined by either FS0 or FS1. This tri-state output remains in the high impedance state except during the assigned transmit time slot.	
15	DR	I	Serial input of 2.048Mb/s PCM data. The PCM data is shifted in at the falling edges of MCLK. The start bit of receive PCM data is defined by either FS0 or FS1.	
16	FS1	I	Frame sync input for channel 1. FS1 must be derived from MCLK, and its periodicity must be 256 MCLK cycles.	
17	ALAWN	I	Companding schemes selection. "H": μ-Law "L": A-Law	
18	GSR1	O	Output of receive output amplifier for channel 1.	
19	VFR1-	I	Inverting input of receive output amplifier for channel 1.	
20	VRX1	O	Receive analog output of SMF for channel 1. This output can drive 10kΩ or larger, and 50pF or smaller.	
21	GSX1	O	Output of transmit input amplifier for channel 1.	
22	VFX1-	I	Transmit analog input. Inverting input of transmit input amplifier for channel 1.	
23	VREF	O	Analog ground output. To stabilize the analog ground, connect to AVSS with 1.0μF or larger.	
24	AVSS	-	Analog negative supply voltage. System analog ground.	

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply Voltages				
Digital Power Supply	DVDD	-0.3	6.5	V
Analog Power Supply 1)	AVDD	-0.3	6.5	V
DVSS Voltage	DVSS	-0.1	0.1	V
Digital Input Voltage	VTD	-0.3	AVDD+0.3	V
Analog Input Voltage	VTA	-0.3	AVDD+0.3	V
Input current (except power supply pins)	IIN	-10	10	mA
Storage Temperature	Tstg	-55	125	°C

Note 1) All voltages with respect to ground. : AVSS=DVSS=0V

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies 1)					
Analog power supply	AVDD	4.75	5.0	5.25	V
Digital power supply	DVDD	4.75	5.0	AVDD	V
Ambient Operating Temperature	Ta	-40		85	°C
Master Clock Frequency	MCLK		2.048		MHz

Note 1) If DVDD is greater than AVDD, then IDD will increase

Note) All voltages reference to ground : AVSS=DVSS=0V

Electrical Characteristics

Unless otherwise noted, guaranteed for AVDD=DVDD=+5V±5%, Ta = -40~+85°C, MCLK=2.048MHz.

■ DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption	PDD	Normal operation Supplying MCLK Outputs unloaded		60	80	mW
Output High Voltage	VOH	IOH=-3.2mA	2.4			V
Output Low Voltage	VOL	IOL=3.2mA			0.4	V
Input High Voltage	VIH		2.0			V
Input Low Voltage	VIL				0.8	V
Input Leakage Current	I i	All pins except TST,TST2	-10		+10	μA
Input Capacitance	Ci				5	pF
Output Leakage Current	Io	Tri-state mode	-10		+10	μA

■Absolute Gain

Parameter	Conditions	Min	Typ	Max	Units
Analog Input Level	Input: 0dBm0@1020Hz		0.849		Vrms
Absolute Transmit Gain		-0.25	–	0.25	dB
	VDD=5V, Ta=25°C	-0.15	–	0.15	dB
Analog Output Level	Input: 0dBm0@1020Hz		0.849		Vrms
Absolute Receive Gain		-0.25	–	0.25	dB
	VDD=5V, Ta=25°C	-0.15	–	0.15	dB
Maximum Overload Level	3.14dBm0		1.219		Vrms

■Gain Tracking

Parameter	Conditions		Min	Typ	Max	Units
Transmit Gain Tracking Error	Reference Level:	-55dBm0~-50dBm0	-1.2	–	1.2	
	-10dBm0	-50dBm0~-40dBm0	-0.4	–	0.4	dB
	1020Hz Tone	-40dBm0~ 3dBm0	-0.2	–	0.2	
Receive Gain Tracking Error	Reference Level:	-55dBm0~-50dBm0	-1.2	–	1.2	
	-10dBm0	-50dBm0~-40dBm0	-0.4	–	0.4	dB
	1020Hz Tone	-40dBm0~ 3dBm0	-0.2	–	0.2	

■Frequency Response

Parameter	Conditions		Min	Typ	Max	Units
Transmit Frequency Response	Relative to:	0.05kHz	–	–	-30	
	0dBm0@1020Hz	0.06kHz	–	–	-26	
		0.2kHz	-1.8	–	0	
		0.3~3.0kHz	-0.15	–	0.15	dB
		3.4kHz	-0.8	–	0	
		4.0kHz	–	–	-14	
Receive Frequency Response	Relative to:	0~3.0kHz	-0.15	–	0.15	
	0dBm0@1020Hz	3.4kHz	-0.8	–	0	dB
		4.0kHz	–	–	-14	

Note) Not tested in production. Parameters guaranteed by design.

■Distortion

Parameter	Conditions		Min	Typ	Max	Units
Transmit Signal to Distortion	1020Hz Tone	-40dBm0~-45dBm0	36	–	–	
		-30dBm0~-40dBm0	30	–	–	dB
		0dBm0~-30dBm0	25	–	–	
Receive Signal to Distortion	1020Hz Tone	-40dBm0~-45dBm0	36	–	–	
		-30dBm0~-40dBm0	30	–	–	dB
		0dBm0~-30dBm0	25	–	–	
Single Frequency Distortion Transmit			–	–	-46	dB
Single Frequency Distortion Receive			–	–	-46	dB
Intermodulation Distortion	-6dBm@860Hz,1380Hz		–	–	-42	dB

Note) C-message Weighted for μ-Law, Psophometric Weighted for A-Law

■Envelope delay Distortion

Parameter	Conditions	Min	Typ	Max	Units
Transmit Delay, Absolute	f =1600Hz	–	–	315	μs
Transmit Delay, Relative	f =500Hz～600Hz	–	–	220	μs
	f =600Hz～1000Hz	–	–	145	
	f =1000Hz～2600Hz	–	–	75	
	f =2600Hz～2800Hz	–	–	105	
	f =2800Hz～3000Hz	–	–	155	
Receive Delay, Absolute	f =1600Hz				μs
	1st FS channel	–	–	200	
	2nd FS channel	–	–	202	
Receive Delay, Relative	f =500Hz～1000Hz	-40	–	–	μs
	f =1000Hz～1600Hz	-30	–	–	
	f =1600Hz～2600Hz	–	–	90	
	f =2600Hz～2800Hz	–	–	125	
	f =2800Hz～3000Hz	–	–	175	

Note) Not tested in production. Parameters guaranteed by design.

■Noise

Parameter	Conditions		Min	Typ	Max	Units
Transmit Noise 1)	μ-law, C-message		–	5	10	dBrnC0
	A-law, Psophometric		–	-85	-80	dBm0p
Receive Noise 2)	μ-law, C-message		–	5	10	dBrnC0
	A-law, Psophometric		–	-85	-80	dBm0p
Noise, Single Frequency	VFXIN = 0 Vrms, DR = DX f=0～100kHz		–	–	-53	dBm0
PSRR, Transmit 3)	AVDD=DVDD=5V±100mVop f=0～50kHz		40	–	–	dB
PSRR, Receive 3)	AVDD=DVDD=5V±100mVop f=0～50kHz		40	–	–	dB
Spurious Out-of-Band Signal at VRX Output 3)	0dBm0,	4.6～7.6kHz	–	–	-32	dB
	0.3～3.4kHz	7.6～8.4kHz	–	–	-40	
	PCM CODE	8.4～100kHz	–	–	-32	

Note 1) Analog Input = Analog Ground
Note 2) Digital Input(RD) = +0 Code
Note 3) Not tested in production. Parameters guaranteed by design.

■Interchannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive	0dBm0@VFXIN, Idle PCM code	–	–	-75	dB
Receive to Transmit	0dBm0 code level, VFXIN = 0 Vrms	–	–	-75	dB
Transmit to Transmit	0dBm0@VFXIN, Idle PCM code	–	–	-75	dB
Receive to Receive	0dBm0 code level, VFXIN = 0 Vrms	–	–	-75	dB

■Intrachannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive	0dBm0@VFXIN, Idle PCM code	–	–	-75	dB
Receive to Transmit	0dBm0 code level, VFXIN = 0 Vrms	–	–	-75	dB

Note) Not tested in production. Parameters guaranteed by design.

■ Analog Interface Transmit Input Amplifier

Parameter	Conditions	Min	Typ	Max	Units
Input Leakage Current	0.6V < V < 4.2V	-100	–	+100	nA
Input Resistance		10	–	–	MΩ
Input Voltage	Relative AVSS	2.3	2.4	2.5	V
Voltage Gain		5000	–	–	V/V
Unity-Gain Bandwidth		1	2	–	MHz
Offset Voltage		-20	–	+20	mV
Load Resistance		10	–	–	kΩ
Load Capacitance		–	–	50	pF
Output Voltage Swing		–	3.6	–	Vp-p
Output Resistance		–	–	10	Ω
Power Supply Rejection Ratio	Feedback Resistor less than 20kΩ 1) f = 0~60kHz,	40	–	–	dB

Note 1) Between GSXn and VFXn- (n = 0 or 1)

Note) Not tested in production. Parameters guaranteed by design.

■Analog Interface Receive Output

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	0dBm0 PCM code	2.3	2.4	2.5	V
Load Resistance		10			kΩ
Load Capacitance				50	pF
Output Voltage Swing			3.6		Vp-p
Output Resistance				10	Ω

Note) Not tested in production. Parameters guaranteed by design.

■Analog Interface Receive Output Amplifier

Parameter	Conditions	Min	Typ	Max	Units
Input Leakage Current	0.6V < V < 4.2V	-100	–	+100	nA
Input Resistance		10	–	–	MΩ
Input Voltage	Relative AVSS	2.3	2.4	2.5	V
Voltage Gain		5000	–	–	V/V
Unity-Gain Bandwidth		1	2	–	MHz
Offset Voltage		-20	–	+20	mV
Load Resistance		10	–	–	kΩ
Load Capacitance		–	–	50	pF
Output Voltage Swing		–	3.6	–	Vp-p
Output Resistance		–	–	10	Ω
Power Supply Rejection Ratio	Feedback Resistor less than 20kΩ 1) f = 0~60kHz,	40	–	–	dB

Note 1) Between GSXn and VFXn- (n = 0 or 1)

Note) Not tested in production. Parameters guaranteed by design.

■Timing Specification

Unless otherwise noted, the specification applies for TA = -40 to +85°C, DVDD = AVDD = 5V+/-5%,DVSS = AVSS = 0V and MCLK = 2.048 MHz. All other limits are assured by correlation with other production tests and/or product design and characterization. All timing parameters are measured at VOH = 2.0V and VOL =0.7V.

Parameter	Symbol	Min	Typ	Max	Units	Ref fig
Frequency of Master Clock	$1/t_{PM}$	–	2.048	–	MHz	1,2
Width of Master Clock High	t_{WMH}	195	–	–	ns	1,2
Width of Master Clock Low	t_{WML}	195	–	–	ns	1,2
Rise time of Master Clock	t_{RM}	–	–	40	ns	1,2
Fall time of Master Clock	t_{FM}	–	–	40	ns	1,2
Delay time to Valid Data from FS or MCLK, whichever comes later, and Delay time from FS to Data Output disabled[1)]	t_{DZF}	20	–	165	ns	2
Delay time from MCLK Low to Data Output disable	t_{DZC}	50	–	165	ns	1
Setup time from DR Valid to MCLK Low	t_{SDM}	40	–	–	ns	1,2
Hold time from MCLK Low to DR Invalid	t_{HMD}	50	–	–	ns	1,2
Hold time from MCLK Low to Frame Sync High	t_{HMF}	10	–	–	ns	2
Setup time from Frame Sync to MCLK Low	t_{SFM}	70	–	T_{PM}-70	ns	2
Hold time from 3rd period of MCLK Low to Frame Sync	t_{HMF1}	90	–	–	ns	2
Delay time from MCLK High to Data Valid[1)]	t_{DMD}	0	–	170	ns	1,2
Setup time from FS to MCLK Low	t_{SF}	80	–	T_{PM}-80	ns	1
Hold time from MCLK low to FS Low	t_{HF}	100	–	–	ns	1
Delay time to TSX Low[2)]	t_{XDP}	0	–	140	ns	1
Hold time from bit clock Low to Frame Sync	t_{HOLD}	0	–	–	ns	1

Note 1) Load on DX 150 pF plus 2 LSTTL load

Note 2) Load on TSX 0-150 pF plus pull up resistor 1.5k Ω minimum

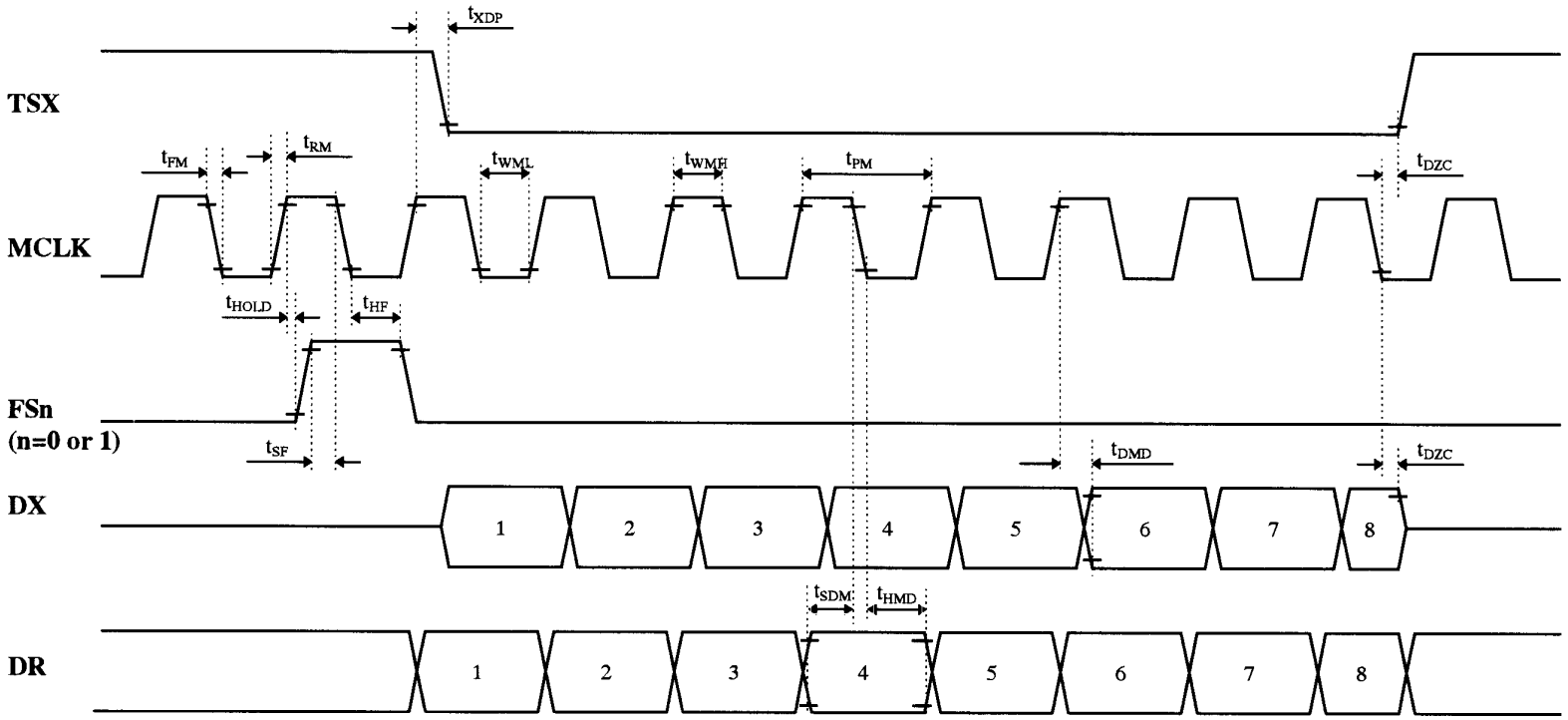


Figure 1. Short Frame Sync Timing Diagram

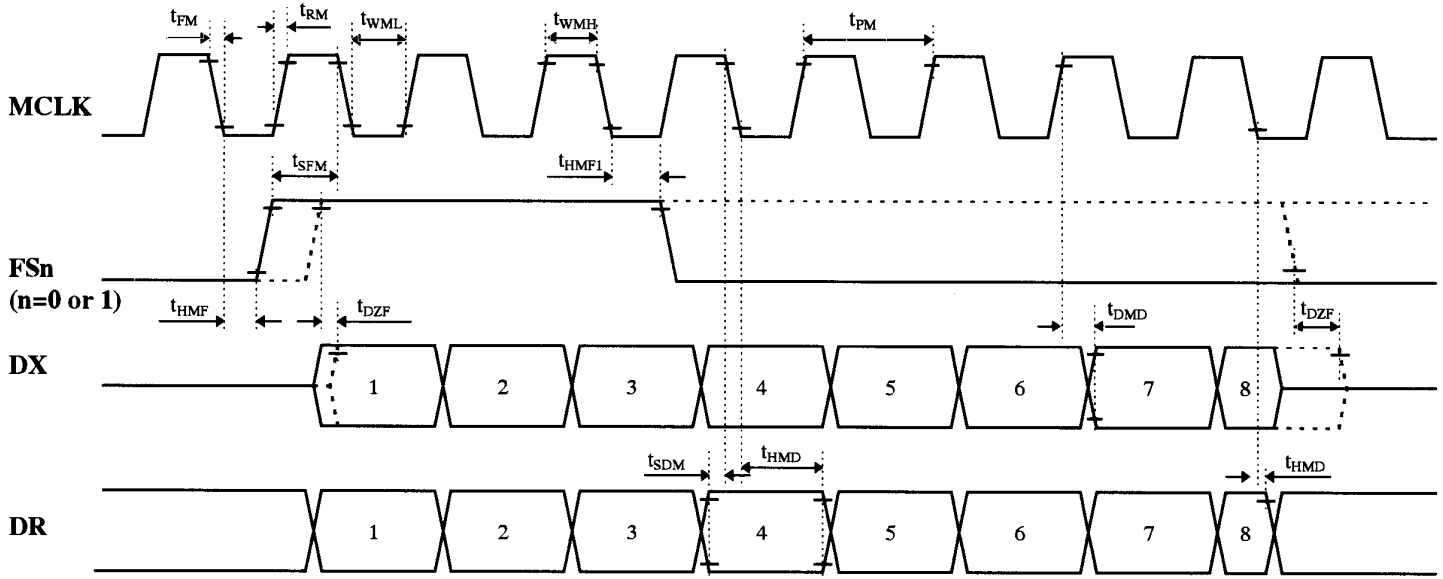
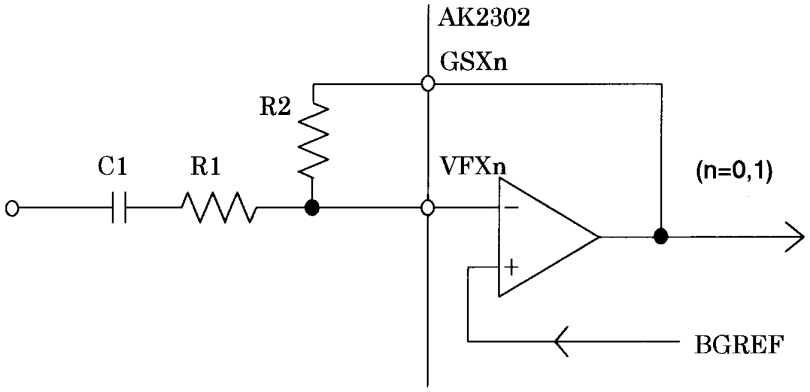


Figure 2. Long Frame Sync Timing Diagram

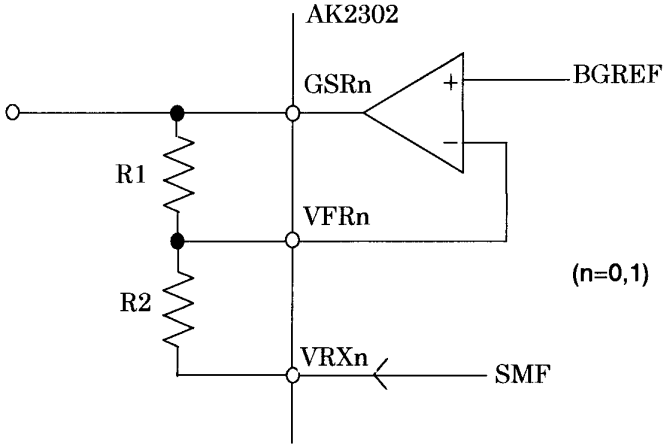
Application Circuit Example

◎Analog input circuit (AMPT0,1)
AK2302 has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment.
Op-amp can be used as an inverting amplifier. Feedback resistor must be 10kΩor larger.



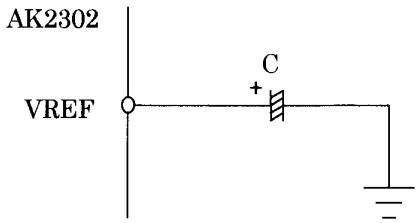
C1=0.47μF
R1=R2=33kΩ

◎Analog output circuit (AMPR0,1)
AK2302 has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment.
Op-amp can be used as an inverting amplifier. Feedback resistor must be 10kΩor larger.

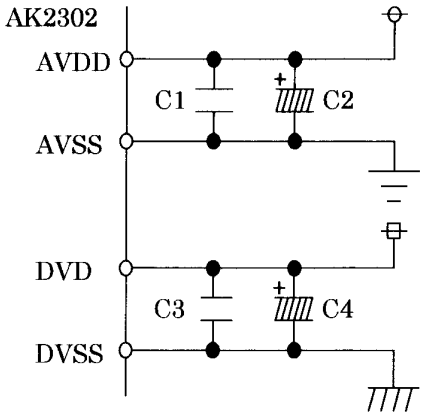


R1=R2=33kΩ

◎Analog ground stabilization capacitor
To stabilize analog ground (VREF), connect to AVSS through 1.0μF or larger capacitor.

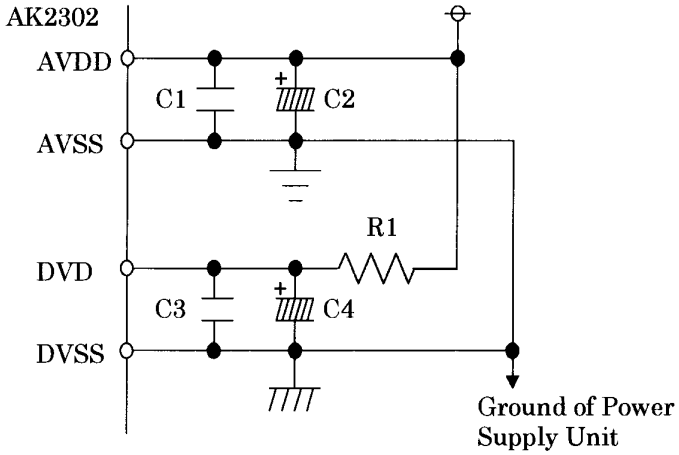


◎Power Supply
To attenuate the power supply noise, connect capacitors between AVDD and AVSS, and DVDD and DVSS, as shown below.



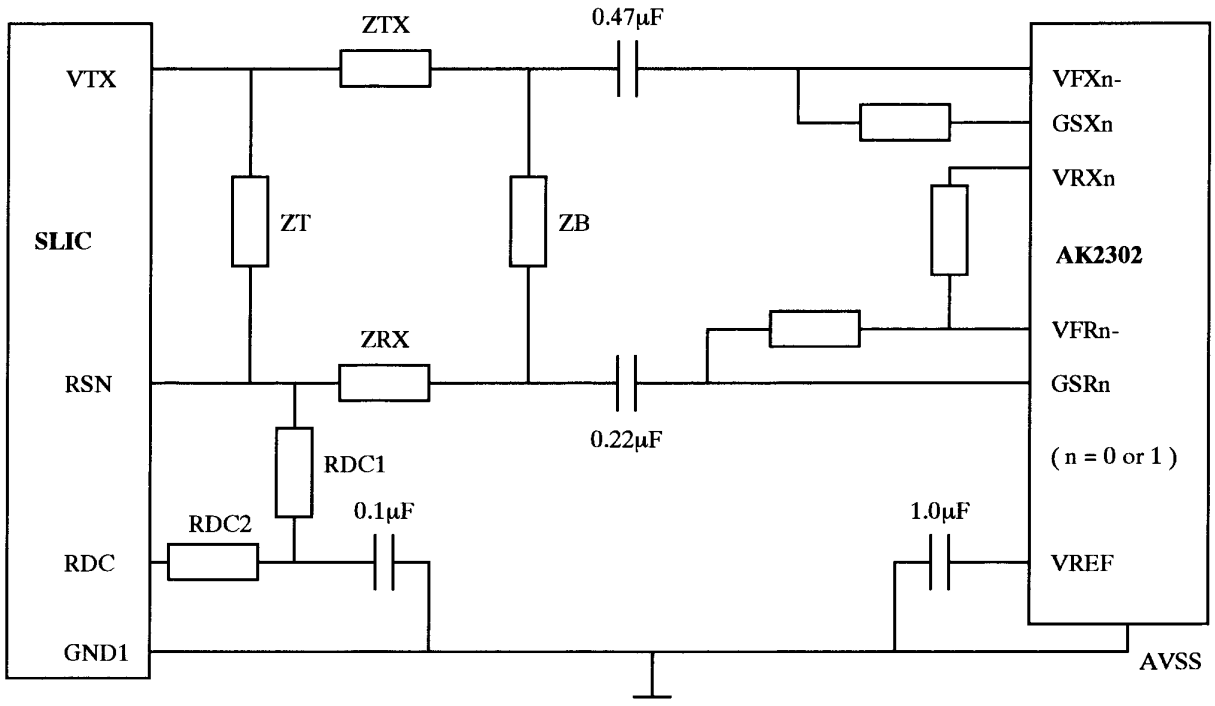
C1=C3=0.1μF
C2=C4=100μF

To use the same supply for both digital and analog power supply (DVDD and AVDD), insert 10Ω resistor between AVDD and DVDD. AVSS and DVSS must be separated on the board, and connected them at power supply unit.



C1=C3=0.1μF
C2=C4=100μF
R1=10Ω

◎Application for SLIC
The example of application circuit with SLIC.

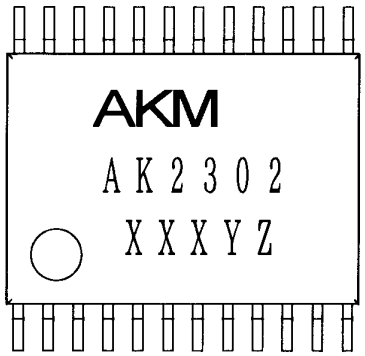


Packaging Information

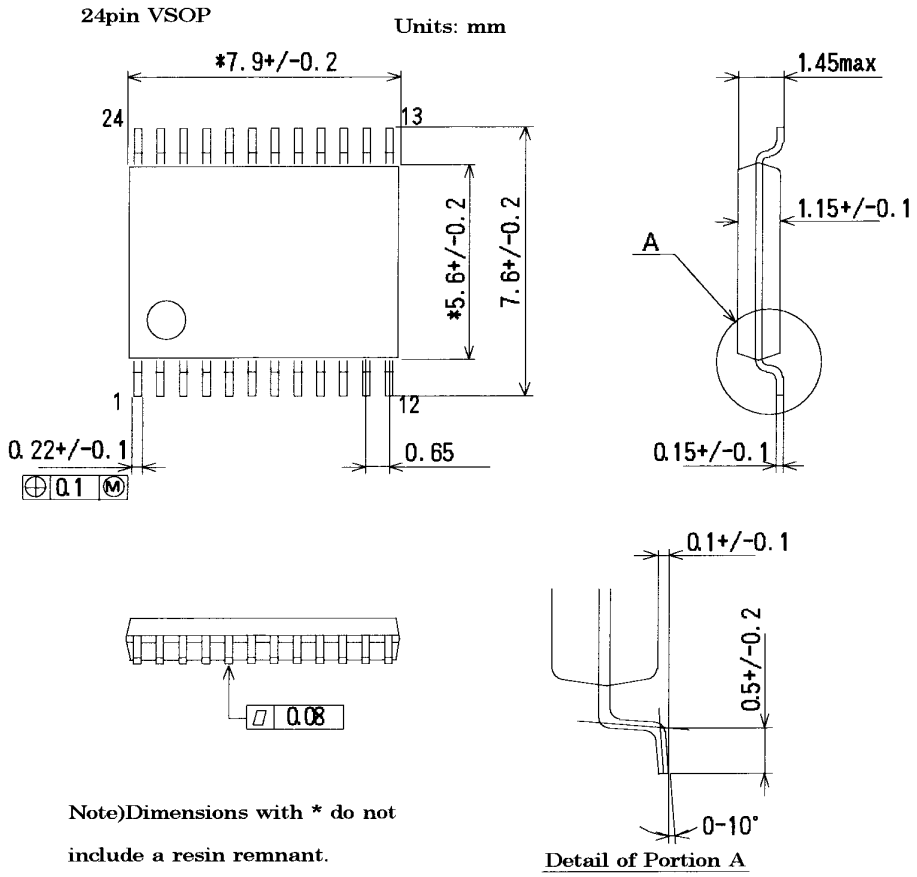
□24pin VSOP

■**Marking**

(1) Pin#1 indication
(2) Date Code: 5 digit XXXYZ
(3) Marketing Code: AK2302
(4) AKM Logo



■Outline Dimensions



[Material] Resin : Low Stress Type Epoxy Resin
Lead Frame : Cu

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