AK2500B

DS3/STS-1 Analog Line Receiver

GENERAL DESCRIPTION

The AK2500B is a DSP based line receiver. It provides the analog receive line interface functions for a 44.736 MHz DS3 or 51.84 MHz STS-1 interface. The device operates from a single +3.3 Volt supply and is transparent to the framing format.

FEATURE

- "Robust" DSP based line receiver
- AK2500B Provides Complete Analog Line Receiver for DS3 and STS-1 Applications
- Provides Line Equalization, and Clock and Data Recovery Functions

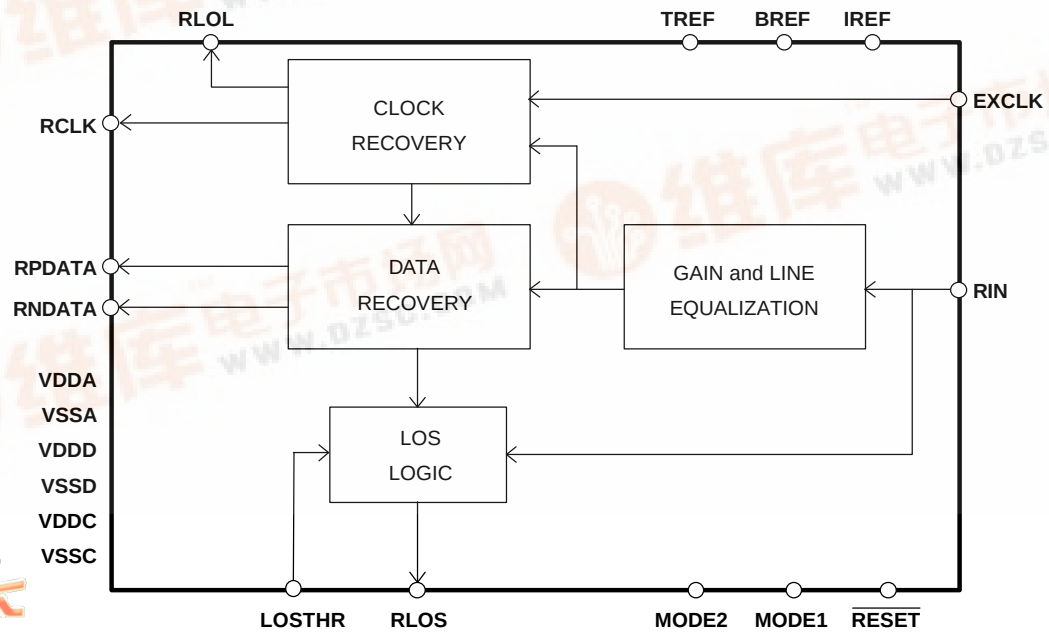
PACKAGE

- 24 pin SOP

APPLICATIONS

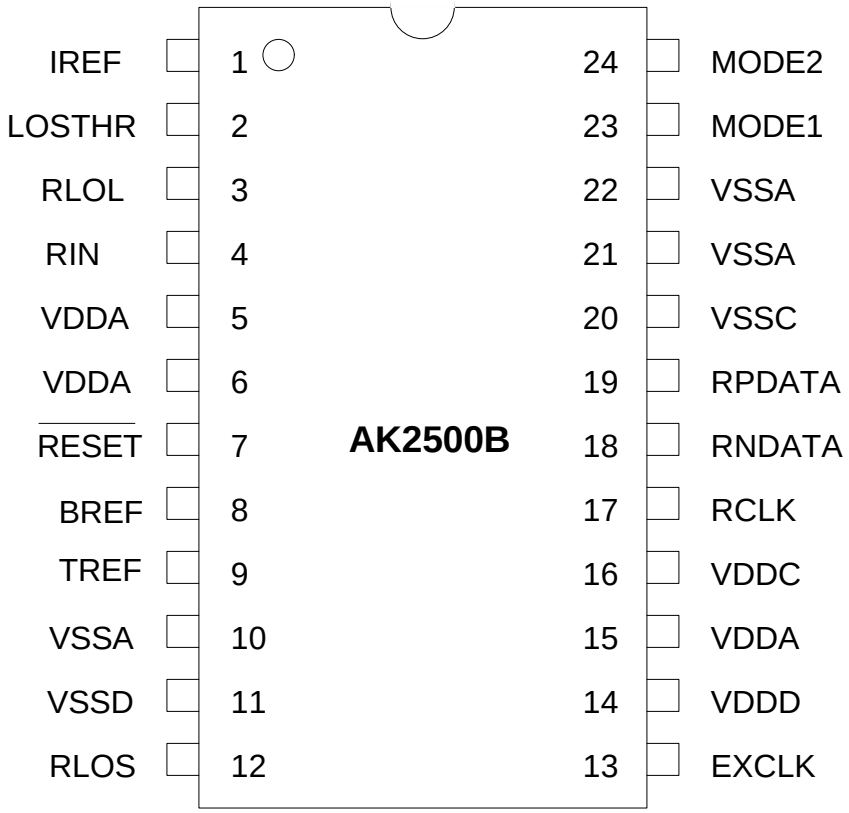
- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-3 cross connect.
- Interfacing customer premises equipment to a line.

BLOCK DIAGRAM



PIN LOCATION

24 PIN SOP Package



PIN CONDITION

No.	Pin Name	I/O	Pin Type	Maximum AC load	Minimum DC load	Status on Reset	Remarks
1	IREF	O	Analog				Note 1
2	LOSTHR	I	Analog				
3	RLOL	O	CMOS	15pF		"H"	
4	RIN	I	Analog				Note 2
5	VDDA	-					
6	VDDA	-					
7	$\overline{\text{RESET}}$	I	CMOS				Note 3
8	BREF	O	Analog				
9	TREF	O	Analog				
10	VSSA	-					
11	VSSD	-					
12	RLOS	O	CMOS	15pF		"H"	
13	EXCLK	I	CMOS				
14	VDDD	-					
15	VDDA	-					
16	VDDC	-					
17	RCLK	O	CMOS	15pF		"L"	
18	RNDATA	O	CMOS	15pF		"L"	
19	RPDATA	O	CMOS	15pF		"L"	
20	VSSC	-					
21	VSSA	-					
22	VSSA	-					
23	MODE1	I	Analog				
24	MODE2	I	Analog				

Note:

1)External resister 4.9 kohm is connected between IREF and VSS.

2)Input impedance of RIN is more than 5kohm.

3)Pulled up to VDD with internal register. (typical 50k ohm)

PIN DESCRIPTION

No.	Pin Name	I/O	Function
1	IREF	O	**Current reference output determined by the external resister.** External resistance 4.9 kohm(+/-1%) should be connected between this pin and VSSA.
2	LOSTHR	I	**Loss of Signal Threshold Control** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD at LOSTHR (see Table 6).
3	RLOL	O	**Receive PLL Loss-of-Lock** Active High alarm. If the recovered clock frequency is larger than approximately 0.5% of EXCLK, RLOL alarm goes High.
4	RIN	I	**Receive Input** Unbalanced analog receive input. The B3ZS receive signal is input to this pins. Data and clock are recovered and output on RPDATA, RNDATA and RCLK.
5	VDDA	-	**Power Supply for the analog part.** +3.3 volts.
6	VDDA	-	
7	$\overline{\text{RESET}}$	I	**Active low RESET.** Pulled up to VDD with internal resister.
8	BREF	O	**Bottom voltage reference level output.** An external capacitor (0.1uF±20%) should be connected between this pin and VSSA.
9	TREF	O	**Top voltage reference level output.** An external capacitor (0.1uF±20%) should be connected between this pin and VSSA.
10	VSSA	-	**Ground for the analog part.** 0 volts.
11	VSSD	-	**Ground for the digital part.** 0 volts.
12	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of the incoming signal at RIN.
13	EXCLK	I	**External Reference Clock.** A valid DS3 or STS-1 clock must be provided at this input. The duty cycle of EXCLK, referenced to VDD/2 levels, must be 40% - 60%. The EXCLK frequency determines the operating frequency of the device.
14	VDDD	-	**Power Supply for the digital part.** +3.3 volts
15	VDDA	-	**Power Supply for the analog part.** +3.3 volts.
16	VDDC	-	**Power Supply for the output buffer.** +3.3 volts.
17	RCLK	O	**Recovered Clock.**
18	RNDATA	O	**Receive Negative Data.**
19	RPDATA	O	**Receive Positive Data.**
20	VSSC	-	**Ground for the output buffer.** 0 volts.
21	VSSA	-	**Ground for the analog part.** 0 volts.
22	VSSA	-	
23	MODE1	I	**Mode Control.** Equalizer enable/bypass mode, Test mode are selectable as shown in Table 4.
24	MODE2	I	

FUNCTIONAL DESCRIPTION

The AK2500B provides the basic receiver functions of a high-speed line card as shown in Fig.7.
The receiver extracts data and clock from a B3ZS coded signal and outputs clock and synchronized data.

Signal Requirements

Pulse characteristics are specified at the DSX-3.

Table 1. DS3 Interface Specification

Parameter	Specification
Line Rate	44.736Mbps±20ppm
Line Code	B3ZS
Test Load	75Ω±5%
Standards	GR-499-CORE , ANSI T1-102 , T1.404

Table 2. STS-1 Interface Specification

Parameter	Specification
Line Rate	51.840Mbps±20ppm
Line Code	B3ZS
Test Load	75Ω±5%
Standards	GR-253-CORE , ANSI T1-102

Equalization

The incoming data may have the loss of cable and/or flat. Cable type and length from the cross-connect are specified as shown in Table 3. Equalizer compensates appropriately for a nominal DSX-3/STS-1 pulse as attenuated by 0 - 450 feet of 728A cable.

Table 3. DS3/STS-1 Cable Specification

Parameter	Specification
Cable Type	Type 728A coaxial cable (or equivalent)
Cable Length	0 – 450 feet (from DSX-3 point)

Equalizer Bypass

If the incoming signal is attenuated by flat loss only (zero cable loss), the internal equalizer should be bypassed with MODE1=1, MODE2=1. (See Table 4) The level of the incoming signal should satisfy the RIN input range (50mVpk - 1000mVpk for DS3/STS-1).

Table 4. Mode Control

MODE2 (pin24)	MODE1 (pin23)	Function
0	0	Equalizer Enable
1	OPEN	TEST MODE (Factory use only)
	1	Equalizer Bypass

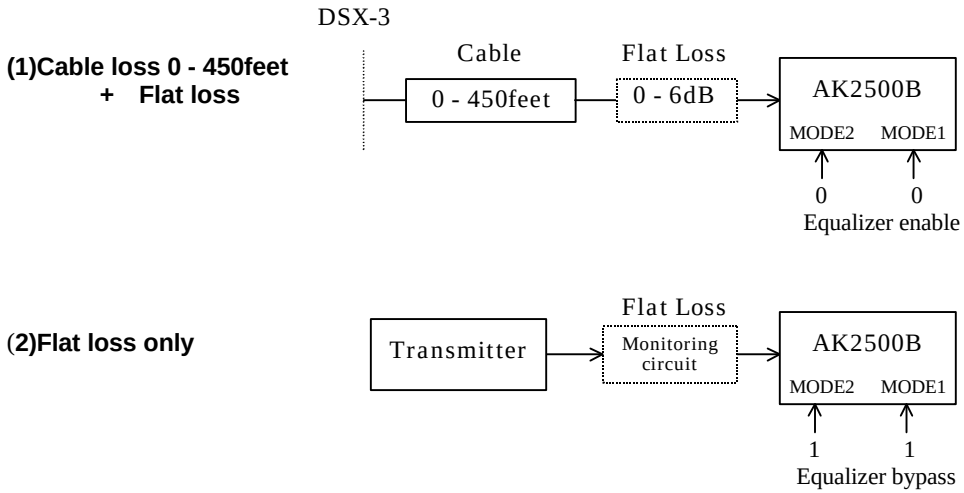


Fig. 1 AK2500B Application

Clock Acquisition

If a valid input signal is assumed to be already present at the analog input, the maximum time between the application of device power and error-free operation is typically 20 ms.

Table 5. PLL Lock Acquisition Time

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

	Conditions	min	typ	Max	Units
Power up	Power : Off -> On Input data : Valid		20		ms
Input data restore	Power : On Input data : Loss -> Valid		1.0	5.0	ms

Output Jitter

Typical output jitter characteristics is shown in the table of ANALOG SPECIFICATIONS (page.11).

Jitter Transfer

Jitter transfer characteristics is shown in the table of ANALOG SPECIFICATIONS (page.11).

Jitter Tolerance

Compliance with GR-499-CORE, GR-253-CORE, ITU-T G.752, G.824
Typical jitter tolerance characteristics is shown in the table of ANALOG SPECIFICATIONS (page.11).

Loss-of-Lock Detection

If the recovered clock frequency is larger than approximately 0.5% of EXCLK, RLOL alarm goes High.

External Reference Clock

An external reference clock EXCLK is used to set the frequency of the PLL. The frequency of EXCLK should be within the ideal clock±100ppm.

Reset

AK2500B/01B goes into RESET status if $\overline{\text{RESET}}$ input is low.
Output pins status is as follows during the low input on $\overline{\text{RESET}}$.

RLOS, RLOL	:	High
RPDATA, RNDATA, RCLK	:	Low

Loss of Signal

This device detects the loss of signal by analog and digital methods. RLOS goes high if either the analog or digital loss has detected.

Analog Loss of Signal(ALOS)

Analog loss detector operates as follows.

- Analog loss detector monitors the peak level of the incoming signal.
- If the peak level falls below Alarm set threshold as shown in Table 6, output pins status is as follows.

RLOS : High
RPDATA: Low
RNDATA: Low
RCLK : Recovered from EXCLK

Table 6. Analog Loss-of-Signal thresholds

LOSTHR Voltage	Clear Alarm Level		Set Alarm Level		Units
	Min. Upper Threshold	Max. Upper Threshold	Min. Lower Threshold	Max. Lower Threshold	
GND	71	125	59	105	mV
VDD/2	56	99	47	83	mV
VDD	45	79	37	66	mV

Notes:

- Set Alarm Level is 0.5dB lower than Clear Alarm Level
- Measured with PN20 pattern, 450ft cable loss, flat loss

Digital Loss of Signal(DLOS)

Digital loss detector operates as follows.

- A digital loss detector monitors consecutive 0s and 1s density in recovered data.
- RLOS is set high if 175±5 consecutive 0s is detected.
- RPDATA,RNDATA are set low if ALOS is detected.
- RLOS is set low if 33% 1s density (58 1s in 175 consecutive bits) and no consecutive 100 bits of 0s are detected.

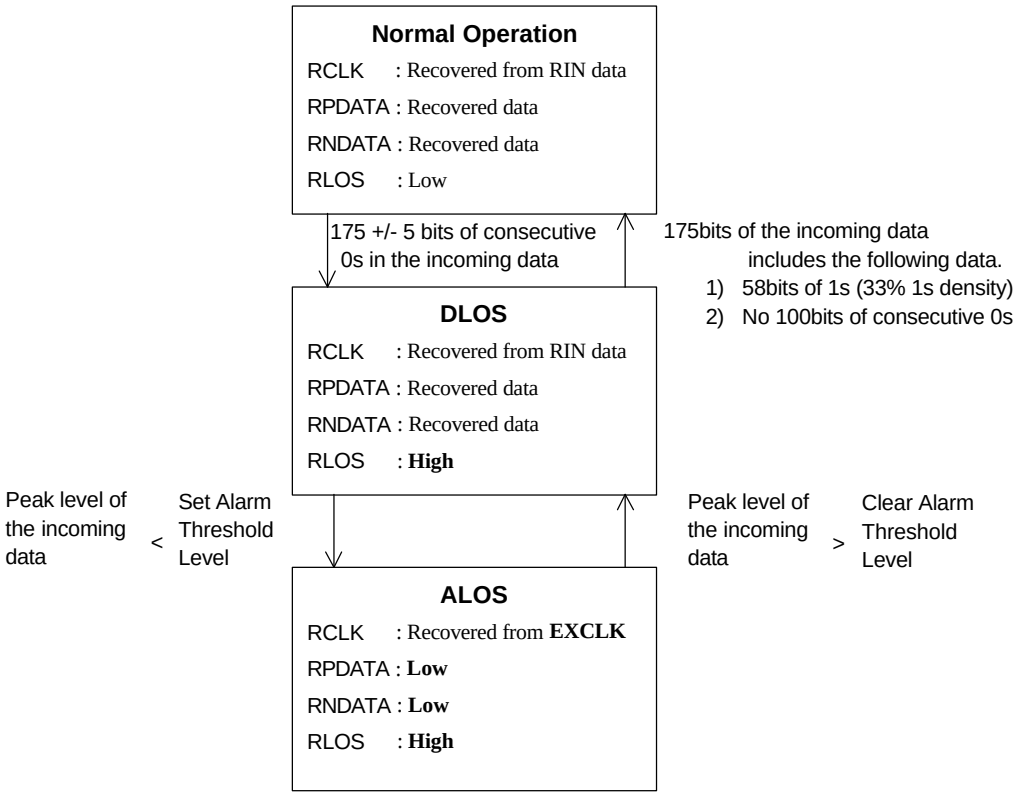


Fig. 2 Loss of Signal state diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND) (Note 1)	V+	-0.3	4.6	V
Input Voltage, Any Pin	Vin	GND-0.3	(V+)+0.3	V
Input Current, Any Pin (Note 2)	Iin	-	10	mA
Ambient Operating Temperature	TA	-40	85	°C
Storage Temperature	tstg	-65	150	°C
Power Dissipation	PD	-	1	W

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note; 1.GND=VSSA=VSSC=VSSD=0V
2.Transient currents of up to 100 mA will not cause SCR latch up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Units
DC Supply (referenced to GND)	V+		3.0	3.3	3.6	V
Ambient Operating Temperature	TA		-40	25	85	°C
Supply Current:	IS					
DS3		PN20	-	95	105	mA
STS-1		PN20	-	100	110	mA
EXCLK Frequency						
DS3			44.736 - 100ppm	44.736	44.736 + 100ppm	MHz
STS-1			51.84 - 100ppm	51.84	51.84 + 100ppm	MHz

ANALOG SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Condition	Min	Typ	Max	Units
Jitter Transfer	3dB Bandwidth	-	205	-	kHz
with repetitive 100 pattern (Note 4)	Peaking	-	0.05	0.1	dB
Jitter Tolerance					
(Including cable loss)	5kHz		18		UIpp
(Note 4, 5)	10kHz		8		UIpp
	60kHz		1.5		UIpp
	300kHz		0.4		UIpp
	1MHz		0.3		UIpp
Signal Noise Immunity (Note 6)		-	11	-	dB
Output Jitter with Jitter-Free Input	All one's pattern	-	1.4	-	nsp-p
(Note4)	Repetitive 1000 pattern	-	1.8	-	nsp-p
Output Clock Duty Cycle (Note4)		45	-	55	%
Receiver Input Range		50	-	1000	mVpk
DLOS detection		170	175	180	bits
RIN to RPDATA Delay Time				8	bits

Note; 4. Measured with repetitive input at nominal DSX-3 level with (V+)=3.3V, TA=25°C
5. Typical performance is shown in Fig. 3.
6. Measured with sinusoidal noise, peak amplitude of noise is 11dB down from peak amplitude of signal. The noise frequency is 22MHz±22kHz(DS3), 26MHz±26kHz(STS-1).

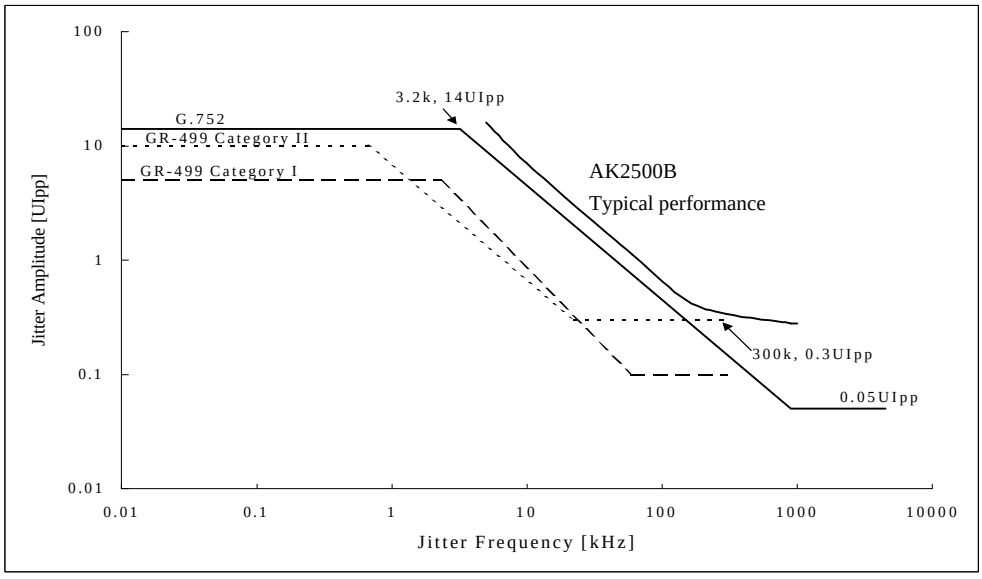


Fig. 3 Jitter Tolerance(STS-1)

DS3 SWITCHING SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter	Symbol	Min	Typ	Max	Units
RCLK Pulse Width (Note 10, 11)	tpwh	10.1	11.177	12.2	ns
	tpwl	10.1	11.177	12.2	ns
EXCLK Duty Cycle (EXCLK Min Rise/Fall time : 5ns)	tpwh1	40	-	60	%
Rise Time, RCLK (Note 11)	tr	-	-	3.5	ns
Fall Time, RCLK (Note 11)	tf	-	-	3.5	ns
Delay time from RCLK rising to RDATA(Note 12)	tdcrd	0	-	3.5	ns
Setup time from RCLK falling to RDATA(Note 12)	tscrd	5.0	-	-	ns
Hold time from RCLK falling to RDATA(Note 12)	thcrd	8.4	-	-	ns

STS-1 SWITCHING SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter	Symbol	Min	Typ	Max	Units
RCLK Pulse Width (Note 11, 13)	tpwh	8.7	9.645	10.6	ns
	tpwl	8.7	9.645	10.6	ns
EXCLK Duty Cycle(EXCLK Min Rise/Fall time : 5ns)	tpwh1/tpw	40	-	60	%
Rise Time, RCLK (Note 11)	tr	-	-	3.5	ns
Fall Time, RCLK (Note 11)	tf	-	-	3.5	ns
Delay time from RCLK rising to RDATA(Note 12)	tdcrd	0	-	3.5	ns
Setup time from RCLK falling to RDATA(Note 12)	tscrd	5.0	-	-	ns
Hold time from RCLK falling to RDATA(Note 12)	thcrd	7.0	-	-	ns

Note; 10. Assumes PLL is locked to 44.736 MHz signal.
11. The sum of the pulse widths must always meet the frequency specifications.
12. At max load of 10 pF.
13. Assumes PLL is locked to 51.84 MHz signal.

DIGITAL CHARACTERISTICS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 14)	VIH	(V+) x 0.7	-	(V+)	V
Low-Level Input Voltage (Note 14)	VIL	GND	-	0.5	V
High-Level Output Voltage(Note 15,16) IOUT=-40uA	VOH	(V+) x 0.8	-	(V+)	V
Low-Level Output Voltage IOUT=1.6mA (Note 15), 0.4mA (Note 16)	VOL	GND	-	0.4	V
Input Leakage Current (Note 17)				±10	uA

Note; 14. Pins RESET
15. Pins RCLK, RPDATA, RNDATA
16. Pins RLOS, RLOL
17. Except RESET

Fig. 4 Signal Rise and Fall Characteristics

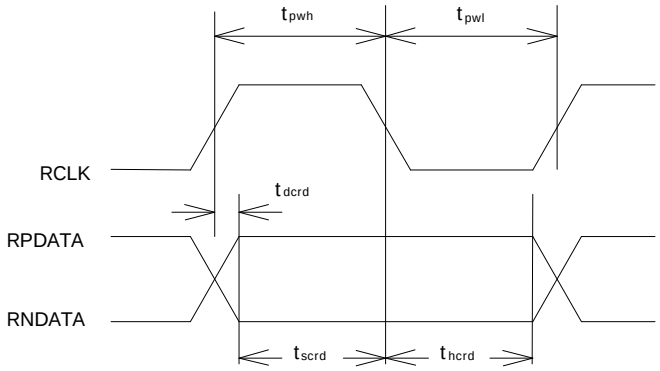


Fig. 5 Recovered Clock and Data Switching Characteristics

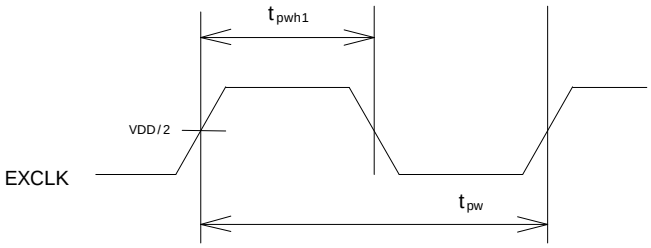


Fig. 6 EXCLK Duty Cycle Requirements

Application Circuit Example

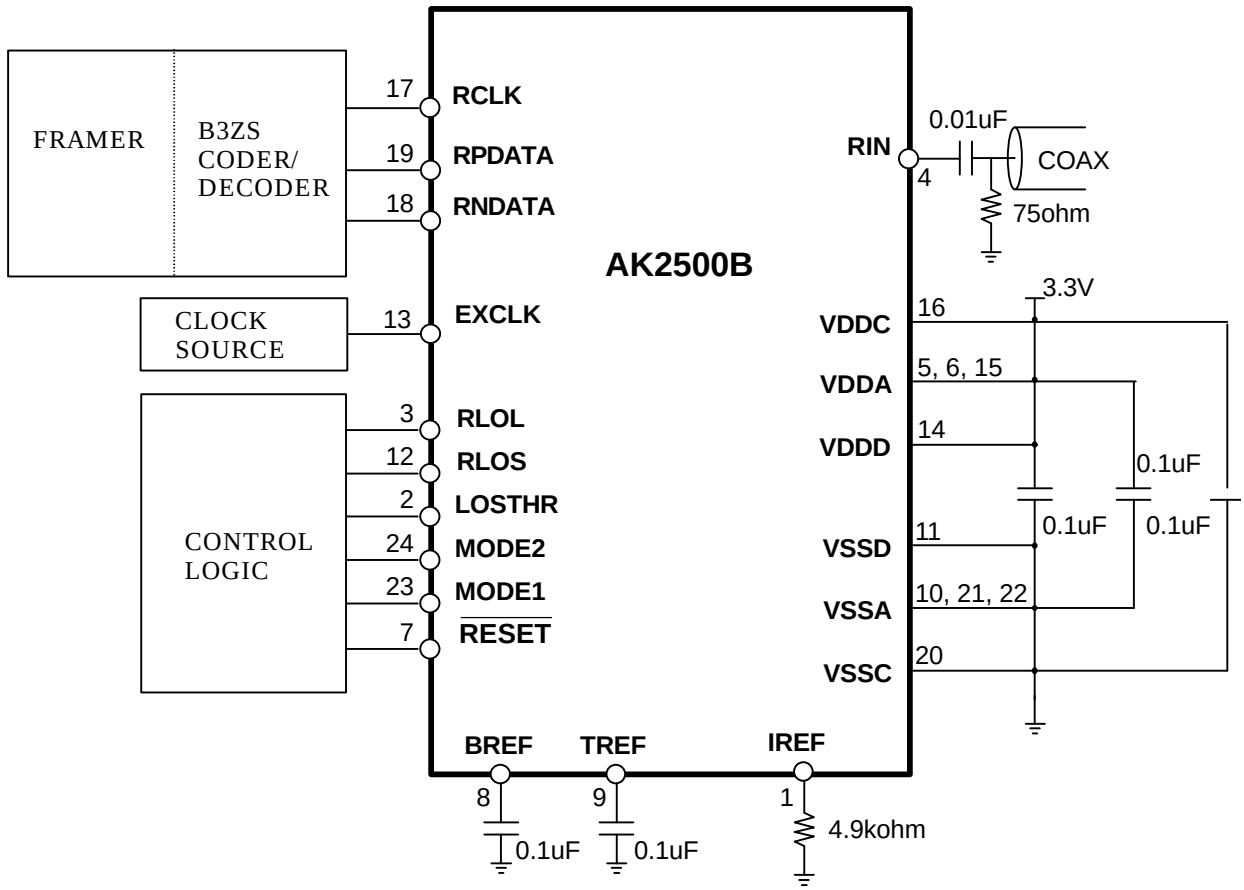


Fig. 7 Application circuit example

Board Layout Consideratons

The recommended power supply de-coupling circuit is illustrated in Figure 7. Good quality high-frequency, low lead-inductance capacitors should be used. If the performance of Jitter Tolerance or S/X is not good, please try to use smaller de-coupling capacitors such as 0.01uF. These performances are affected by the power supply noise which depends on the customer's board circuit and layout. All capacitors should be as close to the device as possible.

Marking

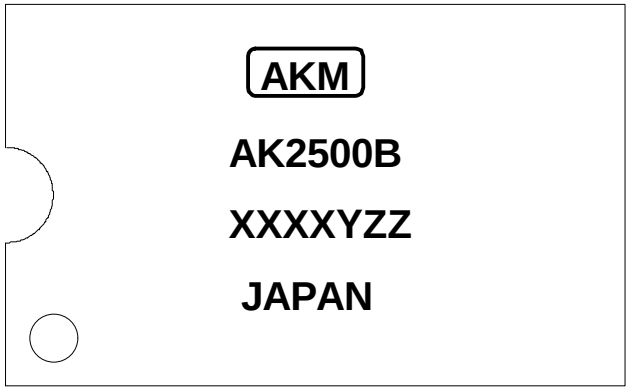
(1)Pin #1 indication

(2)Date Code: 7digits XXXXYZZ

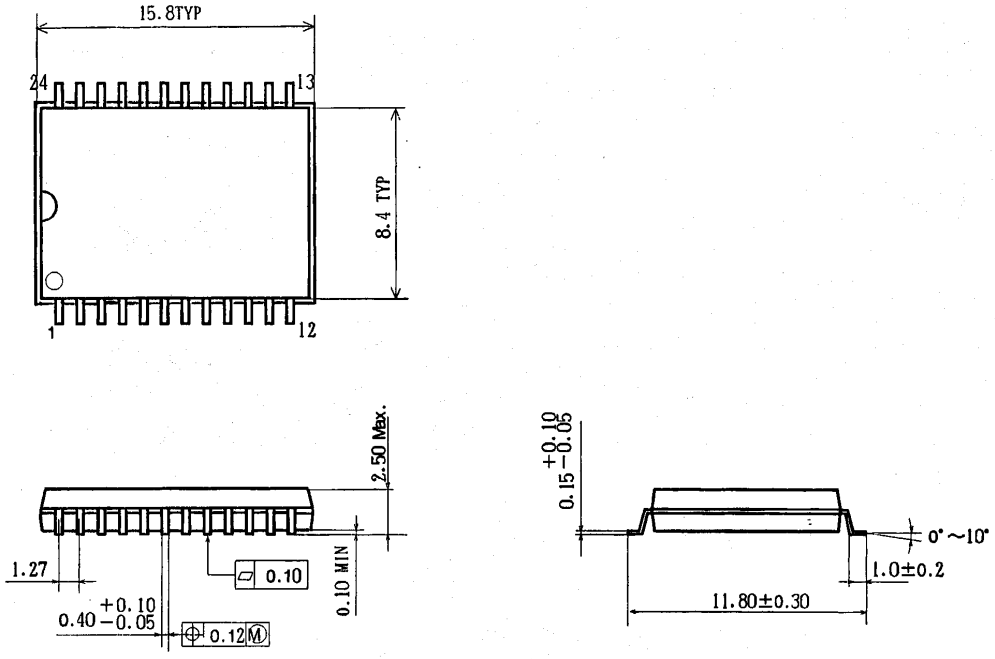
(3)Marketing Code: AK2500B

(4)Country of Origin: JAPAN

(5)Asahi Kasei Logo



Outline Dimensions



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