# AKM

# AK2548

# 7 channel E1 Transceiver

## FEATURE

- 7ch E1 transceiver
- Jitter Tolerance: Compliant with ITU-T G.823, I.431
- Transmitter Pulse Shape: Compliant with ITU-T G.703
- Loss of Signal Detection: Compliant with ITU-T G.775
- Return loss: Compliant with ETS 300 166
- Selectable Signal Polarity
- Local/Remote Loopback
- Parallel/Serial Microprocessor Interface
- Single 3.3V±5% Operation
- Low Power Consumption
- Pin-to-pin compatible with AK2546(7 channel T1 transceiver) except serial interface
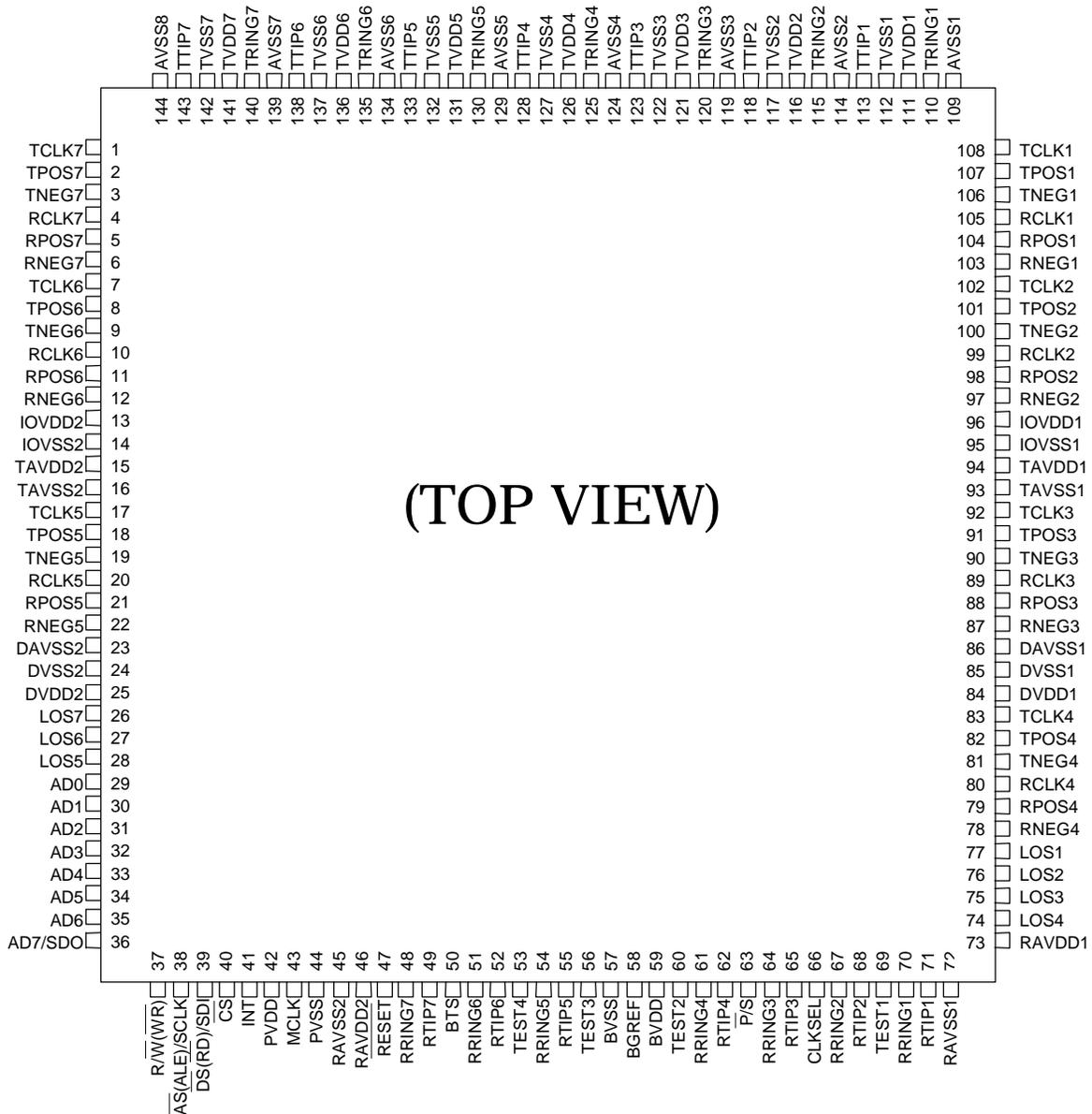- Small Plastic Package 144pin LQFP

## BLOCK DIAGRAM
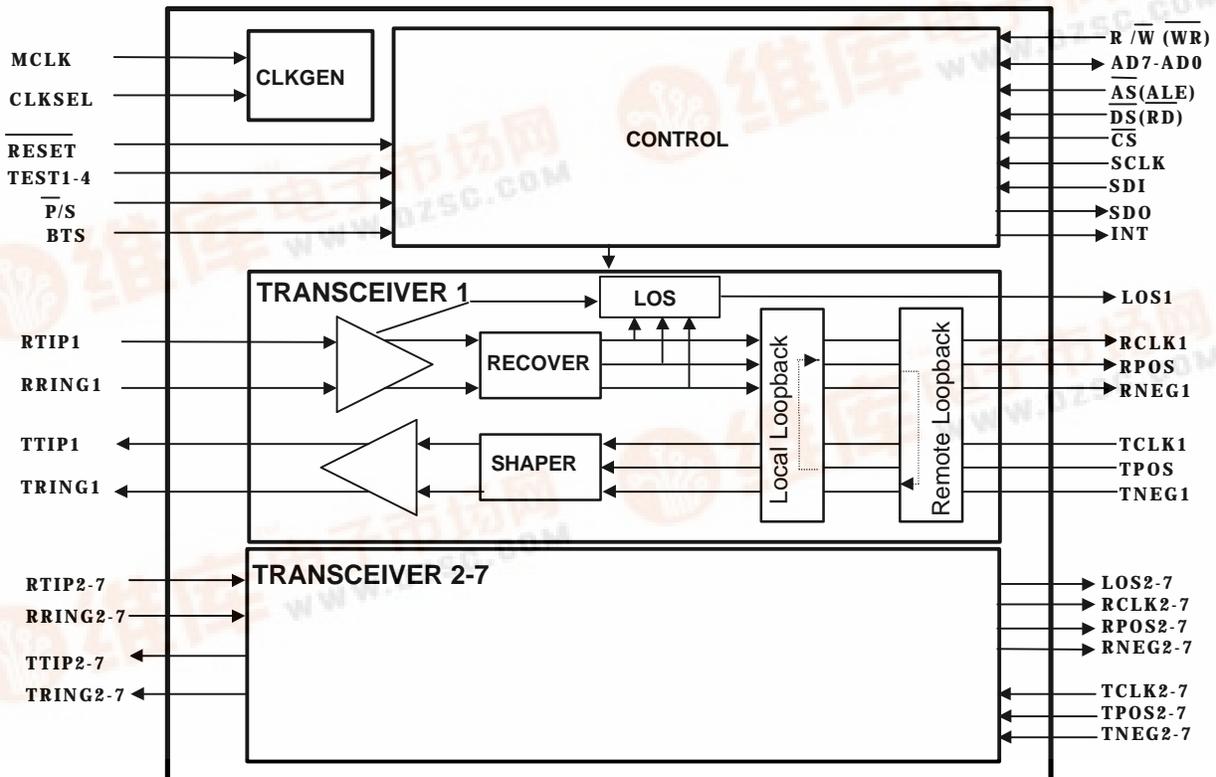


7 Channel E1 Transceiver Block Diagram

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## GENERAL   DESCRIPTION

The AK2548 is the 7 channel E1 transceiver for a SDH/SONET MUX, M13 MUX, etc.

It includes seven independent transmitters, clock and data recovery, LOS detector, control circuit in one LQFP-144 package which saves space, power consumption and the board design time. Internally generated transmit pulse provides the appropriate pulse shape.

## PIN ASSIGNMENTS

(TOP VIEW)

Left side pins (top to bottom):
- 1 TCLK7
- 2 TPOS7
- 3 TNEG7
- 4 RCLK7
- 5 RPOS7
- 6 RNEG7
- 7 TCLK6
- 8 TPOS6
- 9 TNEG6
- 10 RCLK6
- 11 RPOS6
- 12 RNEG6
- 13 IOVDD2
- 14 IOVSS2
- 15 TAVDD2
- 16 TAVSS2
- 17 TCLK5
- 18 TPOS5
- 19 TNEG5
- 20 RCLK5
- 21 RPOS5
- 22 RNEG5
- 23 DAVSS2
- 24 DVSS2
- 25 DVDD2
- 26 LOS7
- 27 LOS6
- 28 LOS5
- 29 AD0
- 30 AD1
- 31 AD2
- 32 AD3
- 33 AD4
- 34 AD5
- 35 AD6
- 36 AD7/SDO

Right side pins (top to bottom):
- 108 TCLK1
- 107 TPOS1
- 106 TNEG1
- 105 RCLK1
- 104 RPOS1
- 103 RNEG1
- 102 TCLK2
- 101 TPOS2
- 100 TNEG2
- 99 RCLK2
- 98 RPOS2
- 97 RNEG2
- 96 IOVDD1
- 95 IOVSS1
- 94 TAVDD1
- 93 TAVSS1
- 92 TCLK3
- 91 TPOS3
- 90 TNEG3
- 89 RCLK3
- 88 RPOS3
- 87 RNEG3
- 86 DAVSS1
- 85 DVSS1
- 84 DVDD1
- 83 TCLK4
- 82 TPOS4
- 81 TNEG4
- 80 RCLK4
- 79 RPOS4
- 78 RNEG4
- 77 LOS1
- 76 LOS2
- 75 LOS3
- 74 LOS4
- 73 RAVDD1

Top side pins (144 to 109, left to right):
- 144 AVSS8
- 143 TTIP7
- 142 TVSS7
- 141 TVDD7
- 140 TRING7
- 139 AVSS7
- 138 TTIP6
- 137 TVSS6
- 136 TVDD6
- 135 TRING6
- 134 AVSS6
- 133 TTIP5
- 132 TVSS5
- 131 TVDD5
- 130 TRING5
- 129 AVSS5
- 128 TTIP4
- 127 TVSS4
- 126 TVDD4
- 125 TRING4
- 124 AVSS4
- 123 TTIP3
- 122 TVSS3
- 121 TVDD3
- 120 TRING3
- 119 AVSS3
- 118 TTIP2
- 117 TVSS2
- 116 TVDD2
- 115 TRING2
- 114 AVSS2
- 113 TTIP1
- 112 TVSS1
- 111 TVDD1
- 110 TRING1
- 109 AVSS1

Bottom side pins (37 to 72, left to right):
- 37 R/W(WR)
- 38 AS(ALE)/SCLK
- 39 DS(RD)/SDI
- 40 CS
- 41 INT
- 42 PVDD
- 43 MCLK
- 44 PVSS
- 45 RAVSS2
- 46 RAVDD2
- 47 RESET
- 48 RRING7
- 49 RTIP7
- 50 BTS
- 51 RRING6
- 52 RTIP6
- 53 TEST4
- 54 RRING5
- 55 RTIP5
- 56 TEST3
- 57 BVSS
- 58 BGREF
- 59 BVDD
- 60 TEST2
- 61 RRING4
- 62 RTIP4
- 63 P/S
- 64 RRING3
- 65 RTIP3
- 66 CLKSEL
- 67 RRING2
- 68 RTIP2
- 69 TEST1
- 70 RRING1
- 71 RTIP1
- 72 RAVSS1

## PIN CONDITION

| Pin No. | Pin Name | I/O | Pin Type | AC Load | DC Load | Comments |
|---|---|---|---|---|---|---|
| 1 | TCLK7 | I | CMOS | | | |
| 2 | TPOS7 | I | CMOS | | | |
| 3 | TNEG7 | I | CMOS | | | |
| 4 | RCLK7 | O | CMOS | ≤15pF | | |
| 5 | RPOS7 | O | CMOS | ≤15pF | | |
| 6 | RNEG7 | O | CMOS | ≤15pF | | |
| 7 | TCLK6 | I | CMOS | | | |
| 8 | TPOS6 | I | CMOS | | | |
| 9 | TNEG6 | I | CMOS | | | |
| 10 | RCLK6 | O | CMOS | ≤15pF | | |
| 11 | RPOS6 | O | CMOS | ≤15pF | | |
| 12 | RNEG6 | O | CMOS | ≤15pF | | |
| 13 | IOVDD2 | I | Power | | | |
| 14 | IOVSS2 | I | Power | | | |
| 15 | TAVDD2 | I | Power | | | |
| 16 | TAVSS2 | I | Power | | | |
| 17 | TCLK5 | I | CMOS | | | |
| 18 | TPOS5 | I | CMOS | | | |
| 19 | TNEG5 | I | CMOS | | | |
| 20 | RCLK5 | O | CMOS | ≤15pF | | |
| 21 | RPOS5 | O | CMOS | ≤15pF | | |
| 22 | RNEG5 | O | CMOS | ≤15pF | | |
| 23 | DAVSS2 | I | Power | | | |
| 24 | DVSS2 | I | Power | | | |
| 25 | DVDD2 | I | Power | | | |
| 26 | LOS7 | O | CMOS | ≤15pF | | |
| 27 | LOS6 | O | CMOS | ≤15pF | | |
| 28 | LOS5 | O | CMOS | ≤15pF | | |
| 29 | AD0 | I/O | CMOS | ≤50pF | | |
| 30 | AD1 | I/O | CMOS | ≤50pF | | |
| 31 | AD2 | I/O | CMOS | ≤50pF | | |
| 32 | AD3 | I/O | CMOS | ≤50pF | | |
| 33 | AD4 | I/O | CMOS | ≤50pF | | |
| 34 | AD5 | I/O | CMOS | ≤50pF | | |
| 35 | AD6 | I/O | CMOS | ≤50pF | | |
| 36 | AD7/SDO | I/O | CMOS | ≤50pF | | |

| Pin No. | Pin Name | I/O | Pin Type | AC Load | DC Load | Comments |
|---|---|---|---|---|---|---|
| 37 | R/$\overline{\text{W}}$($\overline{\text{WR}}$) | I | CMOS | | | |
| 38 | $\overline{\text{AS}}$(ALE)/SCLK | I | CMOS | | | |
| 39 | $\overline{\text{DS}}$($\overline{\text{RD}}$)/SDI | I | CMOS | | | |
| 40 | $\overline{\text{CS}}$ | I | CMOS | | | |
| 41 | INT | O | Open drain | | | PMOS open drain |
| 42 | PVDD | I | Power | | | |
| 43 | MCLK | I | CMOS | | | |
| 44 | PVSS | I | Power | | | |
| 45 | RAVSS2 | I | Power | | | |
| 46 | RAVDD2 | I | Power | | | |
| 47 | $\overline{\text{RESET}}$ | I | CMOS | | | |
| 48 | RRING7 | I | Analog | | | |
| 49 | RTIP7 | I | Analog | | | |
| 50 | BTS | I | CMOS | | | |
| 51 | RRING6 | I | Analog | | | |
| 52 | RTIP6 | I | Analog | | | |
| 53 | TEST4 | I | CMOS | | | Note 1 |
| 54 | RRING5 | I | Analog | | | |
| 55 | RTIP5 | I | Analog | | | |
| 56 | TEST3 | I | CMOS | | | Note 1 |
| 57 | BVSS | I | Power | | | |
| 58 | BGREF | O | Analog | | 12kΩ | ±1% accuracy |
| 59 | BVDD | I | Power | | | |
| 60 | TEST2 | I | CMOS | | | Note 1 |
| 61 | RRING4 | I | Analog | | | |
| 62 | RTIP4 | I | Analog | | | |
| 63 | $\overline{\text{P}}$/S | I | CMOS | | | |
| 64 | RRING3 | I | Analog | | | |
| 65 | RTIP3 | I | Analog | | | |
| 66 | CLKSEL | I | CMOS | | | |
| 67 | RRING2 | I | Analog | | | |
| 68 | RTIP2 | I | Analog | | | |
| 69 | TEST1 | I | CMOS | | | Note 1 |
| 70 | RRING1 | I | Analog | | | |
| 71 | RTIP1 | I | Analog | | | |
| 72 | RAVSS1 | I | Power | | | |

| Pin No. | Pin Name | I/O | Pin Type | AC Load | DC Load | Comments |
|---------|----------|-----|----------|---------|---------|----------|
| 73 | RAVDD1 | I | Power | | | |
| 74 | LOS4 | O | CMOS | ≤15pF | | |
| 75 | LOS3 | O | CMOS | ≤15pF | | |
| 76 | LOS2 | O | CMOS | ≤15pF | | |
| 77 | LOS1 | O | CMOS | ≤15pF | | |
| 78 | RNEG4 | O | CMOS | ≤15pF | | |
| 79 | RPOS4 | O | CMOS | ≤15pF | | |
| 80 | RCLK4 | O | CMOS | ≤15pF | | |
| 81 | TNEG4 | I | CMOS | | | |
| 82 | TPOS4 | I | CMOS | | | |
| 83 | TCLK4 | I | CMOS | | | |
| 84 | DVDD1 | I | Power | | | |
| 85 | DVSS1 | I | Power | | | |
| 86 | DAVSS1 | I | Power | | | |
| 87 | RNEG3 | O | CMOS | ≤15pF | | |
| 88 | RPOS3 | O | CMOS | ≤15pF | | |
| 89 | RCLK3 | O | CMOS | ≤15pF | | |
| 90 | TNEG3 | I | CMOS | | | |
| 91 | TPOS3 | I | CMOS | | | |
| 92 | TCLK3 | I | CMOS | | | |
| 93 | TAVSS1 | I | Power | | | |
| 94 | TAVDD1 | I | Power | | | |
| 95 | IOVSS1 | I | Power | | | |
| 96 | IOVDD1 | I | Power | | | |
| 97 | RNEG2 | O | CMOS | ≤15pF | | |
| 98 | RPOS2 | O | CMOS | ≤15pF | | |
| 99 | RCLK2 | O | CMOS | ≤15pF | | |
| 100 | TNEG2 | I | CMOS | | | |
| 101 | TPOS2 | I | CMOS | | | |
| 102 | TCLK2 | I | CMOS | | | |
| 103 | RNEG1 | O | CMOS | ≤15pF | | |
| 104 | RPOS1 | O | CMOS | ≤15pF | | |
| 105 | RCLK1 | O | CMOS | ≤15pF | | |
| 106 | TNEG1 | I | CMOS | | | |
| 107 | TPOS1 | I | CMOS | | | |
| 108 | TCLK1 | I | CMOS | | | |

| Pin No. | Pin Name | I/O | Pin Type | AC Load | DC Load | Comments |
|---|---|---|---|---|---|---|
| 109 | AVSS1 | I | Power | | | |
| 110 | TRING1 | O | Analog | | | driver output |
| 111 | TVDD1 | I | Power | | | |
| 112 | TVSS1 | I | Power | | | |
| 113 | TTIP1 | O | Analog | | | driver output |
| 114 | AVSS2 | I | Power | | | |
| 115 | TRING1 | O | Analog | | | driver output |
| 116 | TVDD2 | I | Power | | | |
| 117 | TVSS2 | I | Power | | | |
| 118 | TTIP2 | O | Analog | | | driver output |
| 119 | AVSS3 | I | Power | | | |
| 120 | TRING3 | O | Analog | | | driver output |
| 121 | TVDD3 | I | Power | | | |
| 122 | TVSS3 | I | Power | | | |
| 123 | TTIP3 | O | Analog | | | driver output |
| 124 | AVSS4 | I | Power | | | |
| 125 | TRING4 | O | Analog | | | driver output |
| 126 | TVDD4 | I | Power | | | |
| 127 | TVSS4 | I | Power | | | |
| 128 | TTIP4 | O | Analog | | | driver output |
| 129 | AVSS5 | I | Power | | | |
| 130 | TRING5 | O | Analog | | | driver output |
| 131 | TVDD5 | I | Power | | | |
| 132 | TVSS5 | I | Power | | | |
| 133 | TTIP5 | O | Analog | | | driver output |
| 134 | AVSS6 | I | Power | | | |
| 135 | TRING6 | O | Analog | | | driver output |
| 136 | TVDD6 | I | Power | | | |
| 137 | TVSS6 | I | Power | | | |
| 138 | TTIP6 | O | Analog | | | driver output |
| 139 | AVSS7 | I | Power | | | |
| 140 | TRING7 | O | Analog | | | driver output |
| 141 | TVDD7 | I | Power | | | |
| 142 | TVSS7 | I | Power | | | |
| 143 | TTIP7 | O | Analog | | | driver output |
| 144 | AVSS8 | I | Power | | | |

Note 1)Should be connected to VSS externally.

## PIN FUNCTION

| Pin Name | I/O | Function | Comment |
|---|---|---|---|
| **E1 Transceiver** | | | |
| TTIP1-7 | O | Transmit Tip/Ring Output | |
| TRING1-7 | O | Bipolar output over transmit transformer | |
| TPOS1-7 | I | Transmit Positive/Negative Data Input | |
| TNEG1-7 | I | Input on the falling edge of TCLK | |
| TCLK1-7 | I | Transmit Clock Input | |
| RTIP1-7 | I | Receive Tip/Ring Input | |
| RRING1-7 | I | Bipolar Input over receive transformer | |
| RPOS1-7 | O | Receive Positive/Negative Data Output | |
| RNEG1-7 | O | Output on the falling edge of RCLK | |
| RCLK1-7 | O | Receive Clock Output recovered from receive data input | |
| LOS1-7 | O | Loss of signal output<br>Output "high" when detect loss of signal<br>LOSx output is not masked by MLOSx register. | |
| TVDD1-7 | | Positive Power Supply for the Transmit Driver | |
| TVSS1-7 | | Negative Power Supply for the Transmit Driver | |
| AVSS1-8 | | Analog ground . | |
| **Common Block** | | | |
| MCLK | I | 2.048/32.768MHz External Reference Clock Input | |
| $\overline{AS}$(ALE) | I | Address Select(Address Latch Enable) Input | |
| INT | O | Interrupt Output(PMOS open drain, should be tied to GND through a resistor), Active High, INT output goes "high" when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers. | |
| $\overline{DS}$($\overline{RD}$) | I | Data Strobe(Read Enable) Input | |
| R/$\overline{W}$ ($\overline{WR}$) | I | Read/Write(Write Enable) Input | |
| $\overline{CS}$ | I | Chip Select Input | |
| BTS | I | Bus Type Select Input<br>  BTS="H" : Motorola Mode<br>  BTS="L" : Intel Mode | |
| SCLK | I | Serial Clock Input | |
| SDI | I | Serial Data Input | |
| SDO | O | Serial Data Output | |
| AD0-AD7 | I/O | Address/Data Input/Output<br>Used for read/write internal registers. | |

| Pin Name | I/O | Function | Comment |
|---|---|---|---|
| **Common Block** | | | |
| CLKSEL | I | MCLK Select Input<br>  CLKSEL="H":2.048MHz<br>  CLKSEL="L":34.768MHz | |
| $\overline{P}$/S | I | Parallel/Serial Port Select<br>$\overline{P}$/S="H": Serial Port is selected<br>$\overline{P}$/S="L": Parallel Port is selected | |
| $\overline{RESET}$ | I | Reset Input<br>Active "Low" input pulse over 200ns initializes the internal circuit and forces RPOSx/RNEGx output "low" and LOSx output "high". | |
| TEST1,2,3,4 | I | Factory Use. Should be connected to VSS externally. | |
| TAVDD1,2 | | Positive Power Supply for the analog circuitry in the transmitters | |
| TAVSS1,2 | | Negative Power Supply for the analog circuitry in the transmitters | |
| RAVDD1,2 | | Positive Power Supply for the analog circuitry in the receivers | |
| RAVSS1,2 | | Negative Power Supply for the analog circuitry in the receivers | |
| DVDD1,2 | | Positive Power Supply for Digital | |
| DVSS1,2 | | Negative Power Supply for Digital | |
| DAVSS1,2 | | Ground for Digital | |
| IOVDD1,2 | | Positive Power Supply for I/O | |
| IOVSS1,2 | | Negative Power Supply for I/O | |
| BVDD | | Positive Power Supply for Reference Circuit | |
| BVSS | | Negative Power Supply for Reference Circuit | |
| PVDD | | Positive Power Supply for PLL | |
| PVSS | | Negative Power Supply for PLL | |
| BGREF | | Bandgap Reference Output.<br>$12k\Omega\pm1\%$ exeternal register should be connected across this pin and VSS. | |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| DC Supply | VDD | -0.3 | | 6.5 | V | |
| Input Voltage | VIN1 | -0.3 | | VDD+0.3 | V | Apply to except for RTIPx, RRINGx |
| | VIN2 | -3 | | VDD+0.3 | V | Apply to RTIPx, RRINGx |
| Input Current | IIN | | | 10 | mA | |
| Storage Temperature | Tstg | -55 | | 130 | ºC | |

Note) All voltages with respect to ground.

All negative voltage pins=0V.   VDD apply to all positive voltage pins.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | min | typ | max | Units | Condition |
|---|---|---|---|---|---|---|
| DC Supply | V+ | 3.135 | 3.3 | 3.465 | V | 3.3V±5% |
| Ambient Operating Temperature | Ta | -40 | 25 | +85 | ºC | |

Note) All voltages with respect to ground.

All negative voltage pins=0V.   VDD apply to all positive voltage pins.

## ELECTORICAL CHARACTERISTICS

### DC CHARACTERISTICS

| Parameter | | Symbol | min | typ | max | Units | Condition |
|---|---|---|---|---|---|---|---|
| Power Consumption(/ch) | 75Ω | PD | | 75 | 160 | mW | Note1 |
| | 120Ω | | | 70 | 147 | mW | |
| Digital High-Level Output Voltage | | VOH | 0.9VDD | | | V | IOH=-40µA |
| Digital Low-Level Output Voltage | | VOL | | | 0.4 | V | IOL=500µA |
| Digital High-Level Input Voltage | | VIH | 0.7VDD | | | V | |
| Digital Low-Level Input Voltage | | VIL | | | 0.3VDD | V | |
| Input Leak Current | | Ii | | | 10 | µA | |
| Output Current | | IOH | 1.0 | | | mA | INT pin |

Note1:   typ: 50% mark, Room temp., VDD 3.3V

max: 100% mark, Temp./VDD in all range

Not include any other load(ex. External pull up register) except lines.

## RECEIVER

Receiver characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%, VSS, GND=0V,Ta=-40~85ºC,

MCLK frequency: 2.048MHz±100ppm, 32.768MHz±100ppm.

Bipolar input frequency:2.048MHz±50ppm(reference input level: $2.37V_{0p}\pm10\%$@75Ωsystem,

$3V_{0p}\pm10\%$@120Ωsystem)

| Parameter | | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|---|
| Input Impedance | | | 5 | | | kΩ | |
| Sensitivity | | | -6 | | | dB | Note1 |
| Loss of Signal Threshold | 75Ω | | 0.28 | 0.4 | 0.55 | V | Note2 |
| | 120Ω | | 0.35 | 0.5 | 0.7 | V | |
| Allowable Consecutive Zeros before LOS | | | 170 | 175 | 180 | bits | |
| S/X tolerance | | | | | 12 | dB | Note3 |
| Generated Jitter | | | | 16 | | nspp | Note4 |
| Low pulse density immunity | | | 1/16 | | | Mark | |
| Jitter Tolerance | | ITU-T G.823 | | | | | |

Note1: Relative value to the reference level. Compare at 1.024MHz with All mark pattern.

Note2: Level at the line side of transformer. Loss of signal is logical OR between an analog loss of signal
monitors input level and a digital loss of signal check recovered data stream.

Note3: PN15 and AMI 1/4 Mark pattern input. Noise frequency is 1MHz.

Note4: PN15 pattern input.

### Jitter Tolerance(G.823)
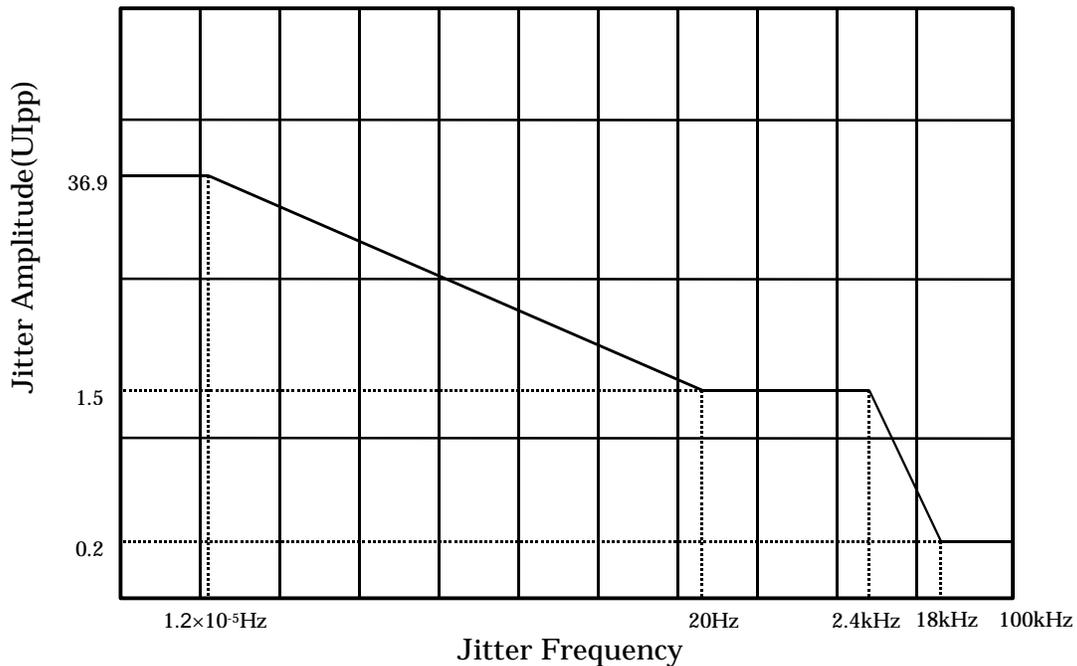
## TRANSMITTER

Transmitter characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%,VSS,GND=0V,Ta=-40~85°C, MCLK frequency:2.048MHz±100ppm, 32.768MHz±100ppm

| Parameter | | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|---|
| Output Pulse Shape | | | | | | | G.703 |
| Output Pulse Amplitude | 75Ω | | 2.14 | 2.37 | 2.60 | $V_{0p}$ | Note 1 |
| | 120Ω | | 2.7 | 3.0 | 3.3 | $V_{0p}$ | |
| Pulse Amplitude for a space | 75Ω | | -0.237 | | 0.237 | $V_{0p}$ | Note 1 |
| | 120Ω | | -0.3 | | 0.3 | $V_{0p}$ | |
| Output Pulse Imbalance | amplitudes | | -4 | | 4 | % | |
| | widths | | -4 | | 4 | % | |
| Output Jitter | 20Hz-100kHz | | | | 0.05 | UIpp | |
| Return Loss | | | | | | | |
| 51kHz-102kHz | | | 9 | | | dB | |
| 102kHz-2.048MHz | | | 15 | | | dB | |
| 2.048MHz-3.072MHz | | | 11 | | | dB | |

Note1: Turns Ratio, DCR and external resistors are recommended value. (P27)

### Pulse Mask Template (G.703)
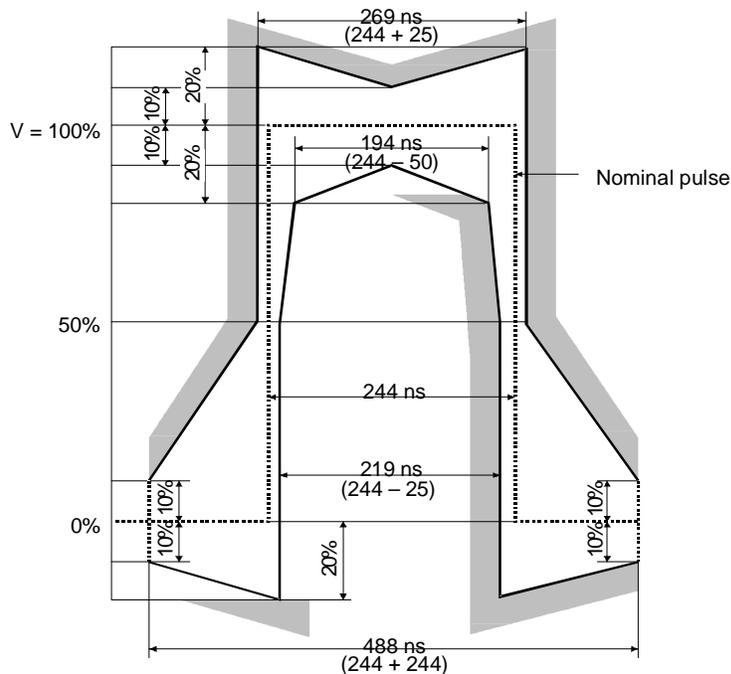


*Note* – V corresponds to the nominal peak value.

**Mask of the pulse at the 2048 kbit/s interface**

## AC CHARACTERISTICS(Clock/Data)

| Parameter | | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|---|
| Clock Frequency | MCLK | fci | 2.047795 | 2.048000 | 2.048204 | MHz | ±100ppm |
| | | | 32.76472 | 32.76800 | 32.77127 | MHz | |
| Clock Pulse Width | TCLK | $t_{pwhi}$ $t_{pwli}$ | | 244 | | ns | Refer to Fig.2 |
| Clock Pulse Width | RCLK | $t_{pwho}$ $t_{pwlo}$ | | 244 | | ns | Refer to Fig.1 |
| Duty Cycle | RCLK TCLK | | | 50 | | % | Note1 |
| Setup/Hold Time | RCLK RPOS RNEG | $t_{su1}$ $t_{h1}$ | 150 | | | ns | Refer to Fig.1 |
| Setup/Hold Time | TCLK TPOS TNEG | $t_{su2}$ $t_{h2}$ | 50 | | | ns | Refer to Fig.2 |
| Rise Time | RCLK RPOS RNEG | $t_r$ | | | 100 | ns | Refer to Fig.3 Note2 |
| Fall Time | TCLK TPOS TNEG | $t_f$ | | | 40 | ns | Refer to Fig.3 Note2 |

Note1) Duty Cycle:$(t_{pwho}/(\,t_{pwho}+t_{pwlo}))\times100\%$

Note2) Drive 15pF Load Capacitance
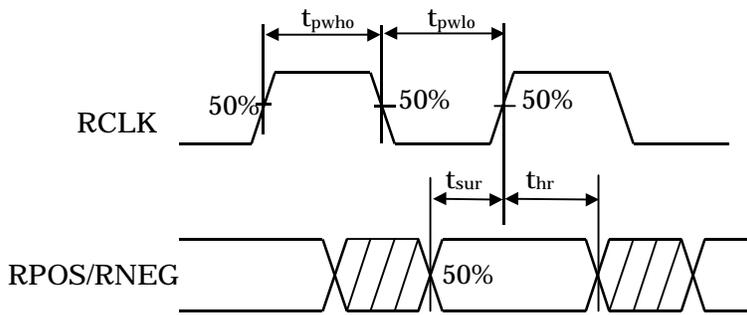
**Figure 1.   Receiver Timing**
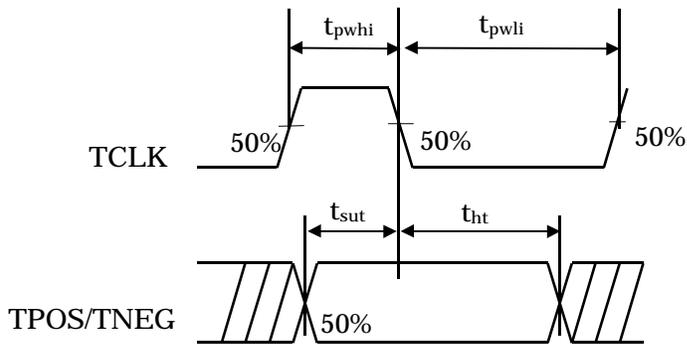
**Figure 2.   Transmitter Timing**
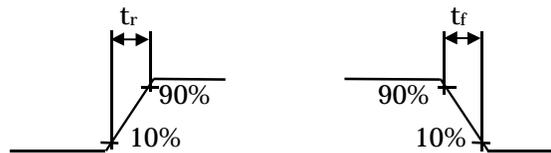
**Figure 3.   Rise and Fall Times**
**(RCLK,RPOS,RNEG,TCLK,TPOS,TNEG)**

## AC CHARACTERISTICS(Parallel Port)

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Read/Write Cycle | tcyc | 250 | | | ns | |
| **Motorola Mode** | | | | | | |
| Address Setup Time | t1 | 10 | — | — | ns | |
| Address Hold Time | t2 | 10 | — | — | ns | |
| $\overline{AS}$ to $\overline{DS}$ Delay Time | t3 | 20 | — | — | ns | |
| $\overline{DS}$ to $\overline{AS}$ Delay Time | t4 | 20 | — | — | ns | |
| Read Data Delay Time | t5 | — | — | 40 | ns | |
| Read Data Hold Time | t6 | — | — | 20 | ns | |
| R/$\overline{W}$ Setup Time | t7 | 10 | — | — | ns | |
| R/$\overline{W}$ Hold Time | t8 | 10 | — | — | ns | |
| $\overline{CS}$ Setup Time | t9 | 10 | — | — | ns | |
| $\overline{CS}$ Hold Time | t10 | 15 | — | — | ns | |
| $\overline{DS}$ to Write Data Setup Time | t11 | 40 | — | — | ns | |
| $\overline{DS}$ to Write Data Hold Time | t12 | 20 | — | — | ns | |
| $\overline{DS}$ Pulse Width | t13 | 100 | — | — | ns | |
| $\overline{AS}$ Pulse Width | t14 | 20 | — | — | ns | |
| Address Invalid to $\overline{DS}$ Delay Time | t15 | 0 | — | — | ns | |
| **Intel Mode** | | | | | | |
| Address Setup Time | t21 | 10 | — | — | ns | |
| Address Hold Time | t22 | 10 | — | — | ns | |
| ALE to $\overline{WR}$ Delay Time | t23 | 20 | — | — | ns | |
| $\overline{WR}$ to ALE Delay Time | t24 | 20 | — | — | ns | |
| $\overline{RD}$ to ALE Delay Time | t25 | 20 | — | — | ns | |
| Read Data Delay Time | t26 | — | — | 40 | ns | |
| Read Data Hold Time | t27 | — | — | 20 | ns | |
| $\overline{CS}$ Setup Time | t28 | 10 | — | — | ns | |
| $\overline{CS}$ Hold Time | t29 | 15 | — | — | ns | |
| $\overline{DS}$ to Write Data Setup Time | t30 | 40 | — | — | ns | |
| $\overline{DS}$ to Write Data Hold Time | t31 | 20 | — | — | ns | |
| $\overline{RD}$ Pulse Width | t32 | 100 | — | — | ns | |
| $\overline{WR}$ Pulse Width | t33 | 100 | — | — | ns | |
| ALE Pulse Width | t34 | 20 | — | — | ns | |
| Address Invalid to $\overline{RD}$ Delay Time | t35 | 0 | — | — | ns | |

Notes) CL= 50pF on AD0-AD7.   All of the timing is specified at 50%VDD.
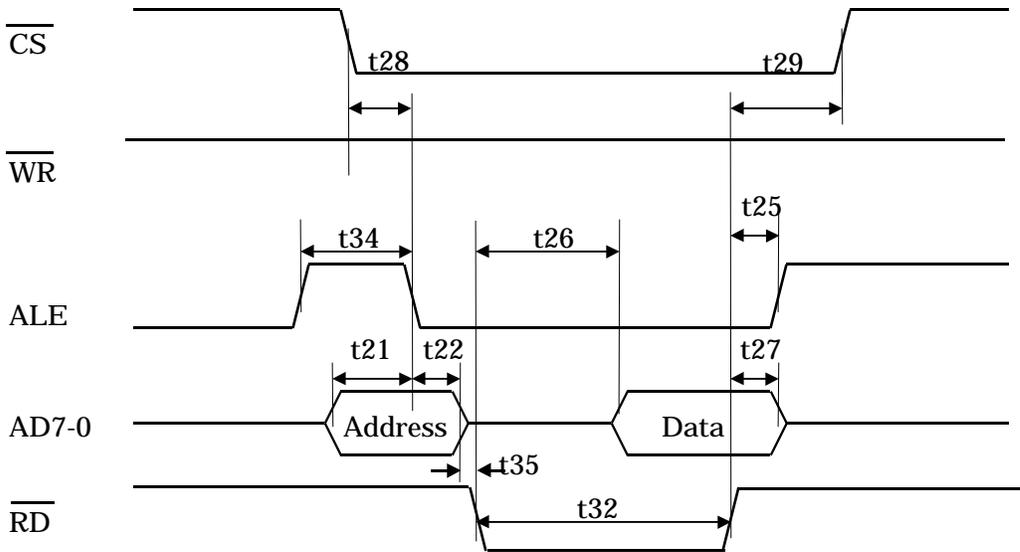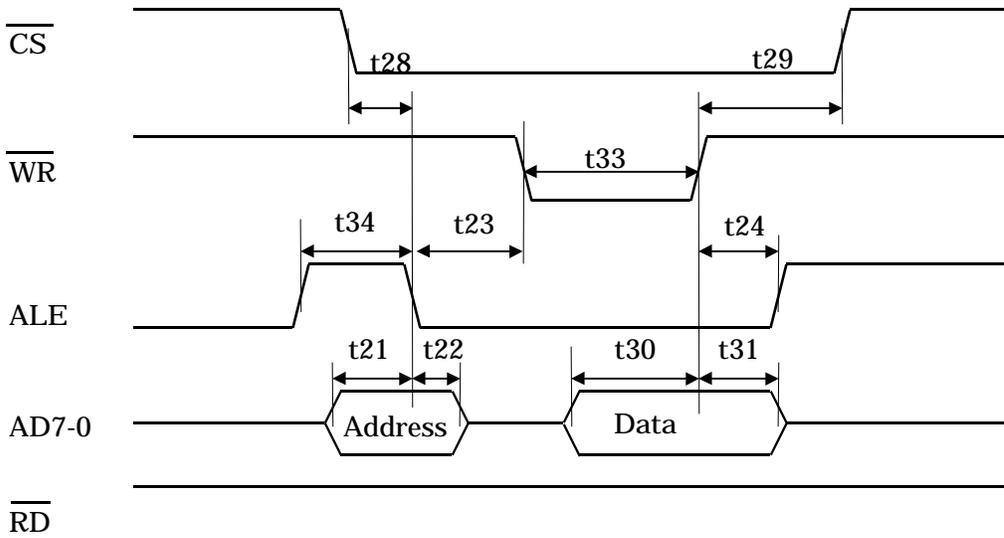
**Motorola Mode(READ)**
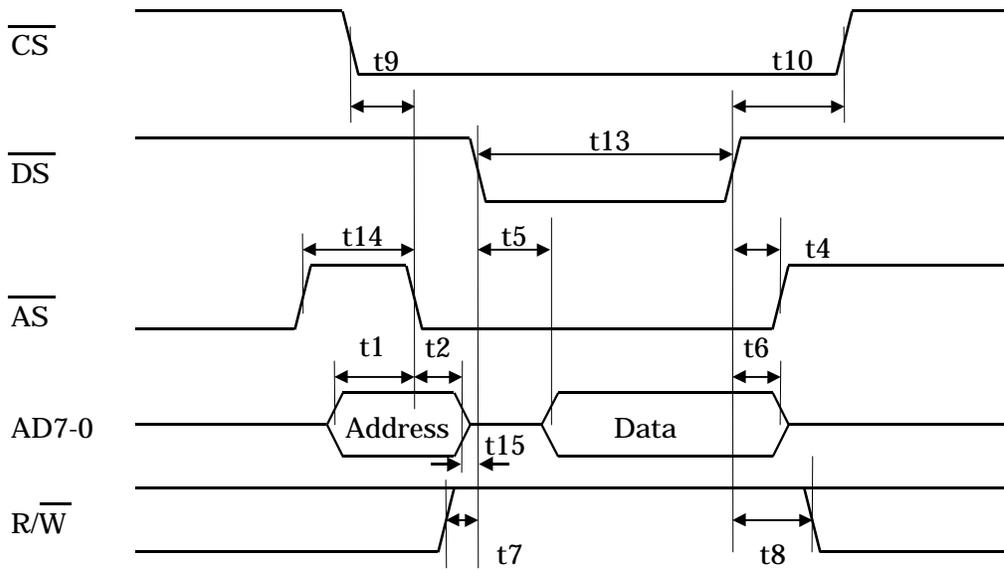


**Motorola Mode(WRITE)**
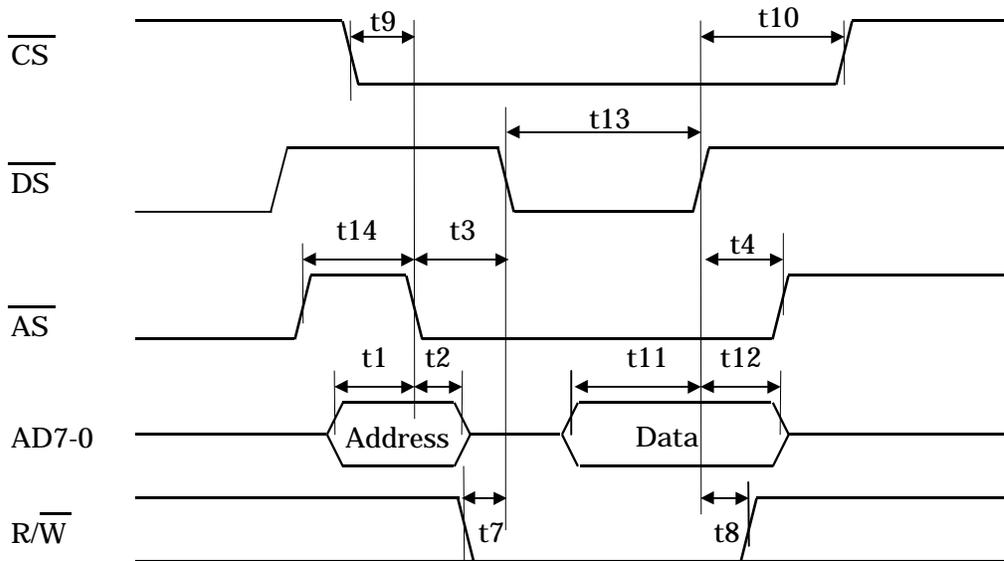
**Intel Mode(READ)**



**Intel Mode(WRITE)**

## AC CHARACTERISTICS(Serial Port)

| Parameter | Symbol | min | typ | max | Units | Condition |
|---|---|---|---|---|---|---|
| SDI Setup Time | tp1 | 25 | — | — | ns | |
| SDI Hold Time | tp2 | 25 | — | — | ns | |
| SCLK Low Time | tp3 | 100 | — | — | ns | |
| SCLK High Time | tp4 | 100 | — | — | ns | |
| SCLK Rise Time | tp5 | — | — | 15 | ns | |
| SCLK Fall Time | tp6 | — | — | 15 | ns | |
| CS Setup Time | tp7 | 20 | — | — | ns | |
| CS Hold Time | Tp8 | 20 | — | — | ns | |
| CS Inactive Time | tp9 | 100 | — | — | ns | |
| SCLK to SDO Valid | tp10 | — | — | 40 | ns | |
| CS to SDO High Z | tp11 | — | — | 40 | Ns | |

Notes) CL= 50pF.    All of the timing is specified at 50%VDD.

## Serial Port Input Timing
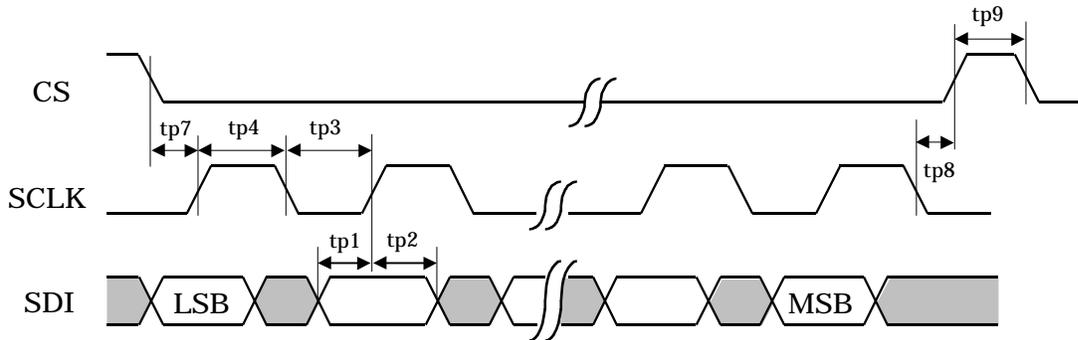


## Serial Port Output Timing
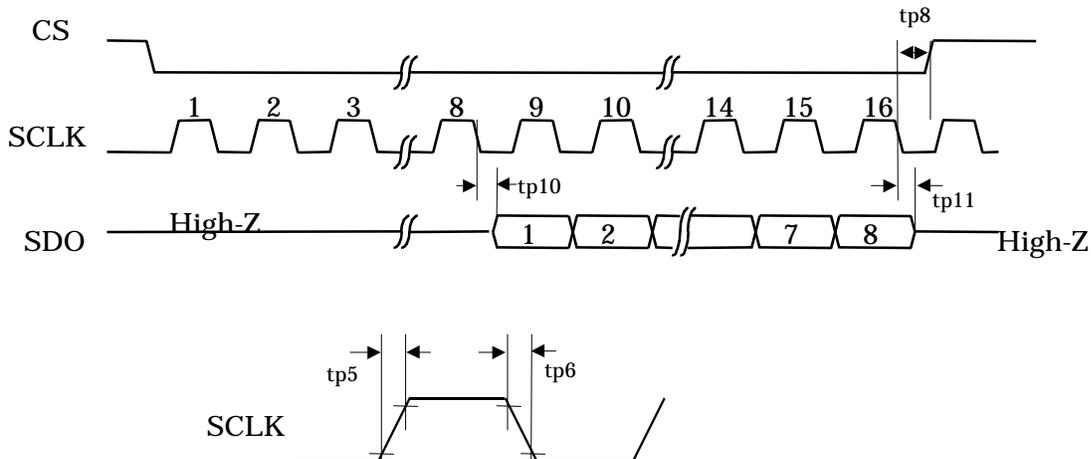
## REGISTER DESCRIPTION

**REGISTER MAP**

*A7-A4="0"

| Address | | | | Function | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | Bit7 <br> \<AD7\> | Bit6 <br> \<AD6\> | Bit5 <br> \<AD5\> | Bit4 <br> \<AD4\> | Bit3 <br> \<AD3\> | Bit2 <br> \<AD2\> | Bit1 <br> \<AD1\> | Bit0 <br> \<AD0\> |
| **Status Register (READ ONLY)** | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | LOS7 <br> (1) | LOS6 <br> (1) | LOS5 <br> (1) | LOS4 <br> (1) | LOS3 <br> (1) | LOS2 <br> (1) | LOS1 <br> (1) | 0 |
| 0 | 0 | 0 | 1 | LOTC7 <br> (1) | LOTC6 <br> (1) | LOTC5 <br> (1) | LOTC4 <br> (1) | LOTC3 <br> (1) | LOTC2 <br> (1) | LOTC1 <br> (1) | LOMC <br> (1) |
| **Mask Control Register (WRITE/READ)** | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | MLOS7 <br> (1) | MLOS6 <br> (1) | MLOS5 <br> (1) | MLOS4 <br> (1) | MLOS3 <br> (1) | MLOS2 <br> (1) | MLOS1 <br> (1) | RDEN <br> (0) |
| 0 | 0 | 1 | 1 | MLOTC7 <br> (1) | MLOTC6 <br> (1) | MLOTC5 <br> (1) | MLOTC4 <br> (1) | MLOTC3 <br> (1) | MLOTC2 <br> (1) | MLOTC1 <br> (1) | MLOMC <br> (1) |
| **Channel Control Register (WRITE/READ)** | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Reserved | TAOS1 <br> (0) | EC1 <br> (0) | RLOOP1 <br> (0) | LLOOP1 <br> (0) | POLN1 <br> (1) | MSK1 <br> (1) | PD1 <br> (1) |
| 0 | 1 | 1 | 1 | Reserved | TAOS2 <br> (0) | EC2 <br> (0) | RLOOP2 <br> (0) | LLOOP2 <br> (0) | POLN2 <br> (1) | MSK2 <br> (1) | PD2 <br> (1) |
| 1 | 0 | 0 | 0 | Reserved | TAOS3 <br> (0) | EC3 <br> (0) | RLOOP3 <br> (0) | LLOOP3 <br> (0) | POLN3 <br> (1) | MSK3 <br> (1) | PD3 <br> (1) |
| 1 | 0 | 0 | 1 | Reserved | TAOS4 <br> (0) | EC4 <br> (0) | RLOOP4 <br> (0) | LLOOP4 <br> (0) | POLN4 <br> (1) | MSK4 <br> (1) | PD4 <br> (1) |
| 1 | 0 | 1 | 0 | Reserved | TAOS5 <br> (0) | EC5 <br> (0) | RLOOP5 <br> (0) | LLOOP5 <br> (0) | POLN5 <br> (1) | MSK5 <br> (1) | PD5 <br> (1) |
| 1 | 0 | 1 | 1 | Reserved | TAOS6 <br> (0) | EC6 <br> (0) | RLOOP6 <br> (0) | LLOOP6 <br> (0) | POLN6 <br> (1) | MSK6 <br> (1) | PD6 <br> (1) |
| 1 | 1 | 0 | 0 | Reserved | TAOS7 <br> (0) | EC7 <br> (0) | RLOOP7 <br> (0) | LLOOP7 <br> (0) | POLN7 <br> (1) | MSK7 <br> (1) | PD7 <br> (1) |

*Other address is reserved.

* Initial value is in ( ).

* "\<\>" show I/O pin name.   Address A0-A3 should be input via AD0-AD3 pins.

**STATUS REGISTER**

| Symbol | Description |
|---|---|
| LOSx (x=1 to 7) | Loss of signal alarm for channel x. Read only register. When the loss of signal or the loss of MCLK are detected, LOSx goes High. |
| LOTCx (x=1 to 7) | Loss of TCLK alarm for channel x. Read only register. When the loss of TCLKx is detected, LOTCx goes High. |
| LOMC | Loss of MCLK alarm. Read only register. When the loss of MCLK is detected, LOMC and LOSx go High. |

**MASK CONTROL REGISTER**

| Symbol | Description |
|---|---|
| MLOSx (x=1 to 7) | Mask loss of signal alarm for channel x. MLOSx is active-high to prevent LOSx from setting INT output "high". It is possible to read LOSx register regardless of the status of MLOSx. Initial value is "high". |
| MLOTCx (x=1 to 7) | Mask loss of TCLK alarm for channel x . MLOTCx is active-high to prevent LOTCx from setting INT output "high". It is possible to read LOTCx register regardless of the status of MLOTCx. Initial value is "high". |
| MLOMC | Mask loss of MCLK alarm. MLOMC is active-high to prevent LOMC from setting INT output "high". It is possible to read LOMC register regardless of the status of MLOMC. Initial value is "high". Note) Please refer to "Loss of MCLK theory of operation". (P25) |

**CHANNEL CONTROL REGISTER**

| Symbol | Description |
|---|---|
| RLOOPx/ LLOOPx | Loopback mode of channel x is activated through the setting of these register as shown below in Table 1. |
| POLNx | TIPx/RINGx output polarity is controlled by this register as shown below in Table 2. Initial value is "high". |
| PDx | PDx is active-high to set the corresponding transceiver in power down mode. TTIPx and TRINGx go "low". LOSx goes "high" in power down mode. Initial value is "high". |
| MSKx | MSKx is active-high to prevent LOSx or LOTCx from setting INT output "high". Initial value is "high". |
| RDEN | RDEN is active-high to prevent RCLK, RPOS, and RNEG output from forcing to "low" or "high" by the detection of Loss of signal. Initial value is "low". |
| TAOSx | TAOS is active-high to output all one's signal from TTIPx and TRINGx. All one's signal synchronized with TCLK. When TCLK is lost, the signal synchronized with MCLK. |
| ECx | Application is selected by this register in Table 3. Initial value is low. |

**Table 1. Loopback mode Select**

| RLOOPx | LLOOPx | Function |
|:---:|:---:|:---|
| 0 | 0 | Normal                          (Initial value) |
| 0 | 1 | Local Loop back |
| 1 | 0 | Remote Loop back |
| 1 | 1 | Inhibited |

**Table 2. TIPx/RINGx Polarity Control**

| POLNx | POSx/NEGx | TIPx/RINGx |
|:---:|:---:|:---:|
| 1 | 0 | space |
|   | 1 | mark |
| 0 | 0 | mark |
|   | 1 | space |

**Table 3 Equalizer Control**

| ECx | Application |
|:---:|:---|
| 0 | E1-Coax(75$\Omega$)                    (Initial value) |
| 1 | E1-Twisted Pair(120$\Omega$) |

## OUTPUT CONTROL

* : don't care

LOS: LOSx output and LOSx register

### Reset, Loss of MCLK, Power down

| RESET | MCLK | PD | TAOS | Loopback | | POLN | RDEN | TCLK | Receive | TTIP | RCLK | RPOS | LOS |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | Local | Remote | | | | Signal | TRING | | RNEG | |
| 0 | * | * | * | * | * | * | * | * | * | 0 | 0 | 0 | 1 |
| 1 | loss | * | * | * | * | 1 | * | * | * | 0 | 0 | 0 | 1 |
| 1 | loss | * | * | * | * | 0 | * | * | * | 0 | 0 | 1 | 1 |
| 1 | clocked | 1 | * | * | * | 1 | * | * | * | 0 | 0 | 0 | 1 |
| 1 | clocked | 1 | * | * | * | 0 | * | * | * | 0 | 0 | 1 | 1 |

### Normal Operation(RESET=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive | TTIP | RCLK | RPOS | LOS |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | Local | Remote | | | | signal | TRING | | RNEG | |
| 0 | 0 | 0 | 1 | * | Clocked | in | TPOS TNEG | RCLK | RTIP RRING | 0 |
| 0 | 0 | 0 | 1 | 0 | Clocked | loss | TPOS TNEG | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | * | Loss | in | 0 | RCLK | RTIP RRING | 0 |
| 0 | 0 | 0 | 1 | 0 | Loss | loss | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | Clocked | loss | TPOS TNEG | RCLK | RTIP RRING | 1 |
| 0 | 0 | 0 | 1 | 1 | Loss | loss | 0 | RCLK | RTIP RRING | 1 |
| 0 | 0 | 0 | 0 | * | Clocked | in | TPOS TNEG | RCLK | RTIP RRING | 0 |
| 0 | 0 | 0 | 0 | 0 | Clocked | loss | TPOS TNEG | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | * | Loss | in | 0 | 0RCLK | RTIP RRING | 0 |
| 0 | 0 | 0 | 0 | 0 | Loss | loss | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | clocked | loss | TPOS TNEG | RCLK | RTIP RRING | 1 |
| 0 | 0 | 0 | 0 | 1 | loss | loss | 0 | RCLK | RTIP RRING | 1 |

## Normal Operation($\overline{\text{RESET}}$=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive | TTIP | RCLK | RPOS | LOS |
|------|-------|--------|------|------|------|---------|------|------|------|-----|
| | Local | Remote | | | | signal | TRING | | RNEG | |
| 1 | 0 | 0 | 1 | * | clocked | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 0 | 1 | 0 | clocked | loss | All Mark | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | * | loss | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 0 | 1 | 0 | loss | loss | All Mark | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | clocked | loss | All Mark | RCLK | RTIP RRING | 1 |
| 1 | 0 | 0 | 1 | 1 | loss | loss | All Mark | RCLK | RTIP RRING | 1 |
| 1 | 0 | 0 | 0 | * | clocked | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 0 | 0 | 0 | clocked | loss | All Mark | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | * | loss | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 0 | 0 | 0 | loss | loss | All Mark | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | clocked | loss | All Mark | RCLK | RTIP RRING | 1 |
| 1 | 0 | 0 | 0 | 1 | loss | loss | All Mark | RCLK | RTIP RRING | 1 |

## Remote Loopback(RESET=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive signal | TTIP TRING | RCLK | RPOS RNEG | LOS |
|---|---|---|---|---|---|---|---|---|---|---|
| | Local | Remote | | | | | | | | |
| 0 | 0 | 1 | 1 | * | * | in | RTIP RRING | RCLK | RTIP RRING | 0 |
| 0 | 0 | 1 | 1 | 0 | * | loss | RTIP RRING | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | * | loss | RTIP RRING | RCLK | RTIP RRING | 1 |
| 0 | 0 | 1 | 0 | * | * | in | RTIP RRING | RCLK | RTIP RRING | 0 |
| 0 | 0 | 1 | 0 | 0 | * | loss | RTIIP RRING | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | * | loss | RTIP RRING | RCLK | RTIP RRING | 1 |

## Remote Loopback(RESET=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive signal | TTIP TRING | RCLK | RPOS RNEG | LOS |
|---|---|---|---|---|---|---|---|---|---|---|
| | Local | Remote | | | | | | | | |
| 1 | 0 | 1 | 1 | * | * | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 1 | 1 | 0 | * | loss | All Mark | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | * | loss | All Mark | RCLK | RTIP RRING | 1 |
| 1 | 0 | 1 | 0 | * | * | in | All Mark | RCLK | RTIP RRING | 0 |
| 1 | 0 | 1 | 0 | 0 | * | loss | All Mark | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | * | loss | All Mark | RCLK | RTIP RRING | 1 |

## Local Loopback($\overline{\text{RESET}}$=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive | TTIP | RCLK | RPOS | LOS |
|---|---|---|---|---|---|---|---|---|---|---|
| | Local | Remote | | | | signal | TRING | | RNEG | |
| 0 | 1 | 0 | 1 | * | clocked | in | TPOS TNEG | TCLK (Note) | TPOS TNEG | 0 |
| 0 | 1 | 0 | 1 | * | clocked | loss | TPOS TNEG | TCLK (Note) | TPOS TNEG | 1 |
| 0 | 1 | 0 | 1 | * | loss | in | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | * | loss | loss | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | * | clocked | in | TPOS TNEG | TCLK (Note) | TPOS TNEG | 0 |
| 0 | 1 | 0 | 0 | * | clocked | loss | TPOS TNEG | TCLK (Note) | TPOS TNEG | 1 |
| 0 | 1 | 0 | 0 | * | loss | in | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | * | loss | loss | 0 | 0 | 1 | 1 |

Note) The phase satisfy receive output timing.

## Local Loopback($\overline{\text{RESET}}$=1, MCLK:clocked, PD=0)

| TAOS | Loopback | | POLN | RDEN | TCLK | Receive | TTIP | RCLK | RPOS | LOS |
|---|---|---|---|---|---|---|---|---|---|---|
| | Local | Remote | | | | signal | TRING | | RNEG | |
| 1 | 1 | 0 | 1 | * | clocked | in | All Mark | TCLK (Note) | TPOS TNEG | 0 |
| 1 | 1 | 0 | 1 | * | clocked | loss | All Mark | TCLK (Note) | TPOS TNEG | 1 |
| 1 | 1 | 0 | 1 | * | loss | in | All Mark | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | * | loss | loss | All Mark | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | * | clocked | in | All Mark | TCLK (Note) | TPOS TNEG | 0 |
| 1 | 1 | 0 | 0 | * | clocked | loss | All Mark | TCLK (Note) | TPOS TNEG | 1 |
| 1 | 1 | 0 | 0 | * | loss | in | All Mark | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | * | loss | loss | All Mark | 0 | 1 | 1 |

Note) The phase satisfy receive output timing.

---
**THEORY OF OPERATION**
---

## Loss of signal

Loss of signal in channel x is reported by setting LOSx register "high".

The receiver will indicate loss of signal upon receiving 175 consecutive zeros or detecting input level being below the threshold(ALOS).

LOSx returns to "low" when the received signal returns to 12.5% ones density and not include 100 consecutive zeros.

When Loss of Signal is detected in channel x, LOSx register is set "high" and LOSx pin becomes "high".   When LOSx is set "high", interrupt will be issued on INT pin if MLOSx is "low". LOSx pin becomes high regardless of MLOSx status. MLOSx is active-high and masks LOSx interrupt. LOSx register represents the current status of received signal regardless of the status of the MLOSx status.

## Loss of TCLK

Loss of TCLKx is reported by setting LOTCx "high". When LOTCx is set "high", INT output becomes "high" if MLOTCx is "low". Even if TCLK return to normal quickly, LOTCx remain "high" for 126us.   MLOTCx is active-high and masks LOTCx interrupt.   LOTCx represents the current status of TCLKx and can be read regardless of the status of the MLOTCx status.

When Loss of TCLKx is detected, TTIPx/TRINGx will be forced to "0".

## Loss of MCLK

Loss of MCLK is reported by setting LOMC "high". When LOMC goes "high", INT output becomes "high" if MLOMC is "low".   Even if MCLK return to normal quickly, LOMC remain "high" for 126us.   MLOMC is active-high and masks LOMC interrupt.   LOMC represents the current status of MCLK and can be read regardless of MLOMC status.   When the loss of MCLK is detected, LOSx register and LOSx pin goes "high" at the same time.   Therefore all MLOSx register must be set to "high" to prevent loss of MCLK from setting INT output.

## INT output

INT output goes "high" when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.

**Local Loopback**

In Local Loopback mode, TPOSx,TNEGx,TCLKx signals are looped back to RPOSx, RNEGx, RCLKx output. RTIPx,RRINGx inputs are ignored but loss of signal detection is active. The transmitter in channel x outputs TTIPx,TRINGx normally.

**Remote Loopback**

In Remote Loopback mode, RTIPx/RRINGx signals are looped back to TTIPx/TRINGx output. The receiver in channel x output RPOSx,RNEGx,RCLKx normally and detect loss of signal. TPOSx,TNEGx,TCLKx inputs are ignored. When TAOSx is "high", all mark signal is output to TTIPx/TRINGx.

**Interface**

Interface to control/status register is selected by $\overline{P}$/S pin. When $\overline{P}$/S is set to "low", parallel interface is selected. When $\overline{P}$/S is set to "high", serial interface is selected.

**Parallel Interface**

Bus type(Intel/Motorola) is selected by BTS pin.

When BTS is set to "high", Motorola mode is selected. When BTS is set to "low", Intel mode is selected.

**Serial Interface**

The timing of serial interface is shown below.
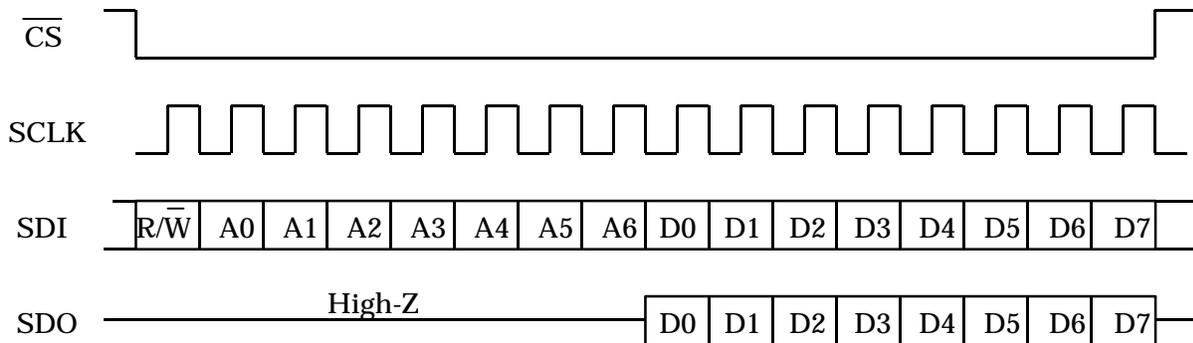


$R/\overline{W}$=1: read

$R/\overline{W}$=0: write

**RECOMMENDED EXTERNAL CIRCUIT**

**Transmit Circuit**
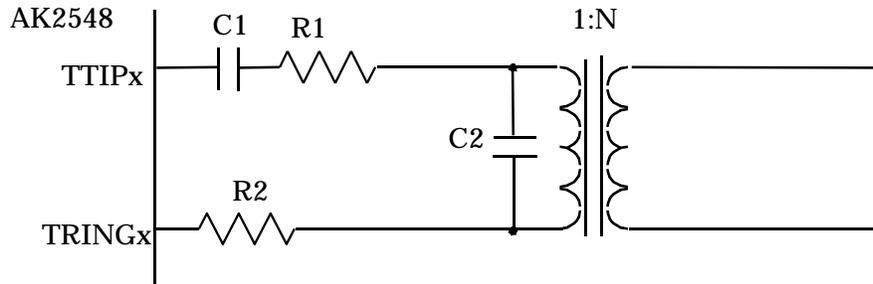


| | 75Ω | 120Ω |
|---|---|---|
| Trans Rate | 1:2 | 1:2.2 |
| R1.R2 | 8.2Ω±1% | 9.1Ω±1% |
| C1 | 1uF | 1uF |
| C2 | 470pF | 470pF |

**Received Circuit**
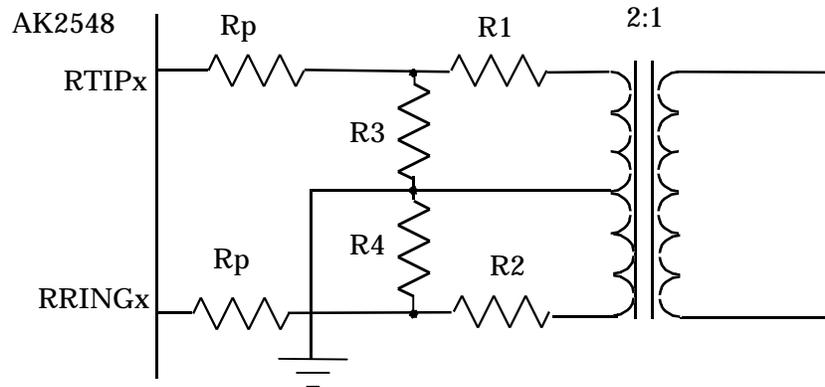


| | 75Ω | 120Ω |
|---|---|---|
| R1,R2 | 20Ω | 82Ω |
| R3,R4 | 130Ω | 160Ω |
| Rp | 100Ω | |

*Rp is protection resistance against surge.

Rp is used for surge current limiting. (ITU-T K.41)

**Recommended Transformer Specification**

| | | Turns Ratio (Typ) | Primary Inductance (Min) | Leakage Inductance (Max) | Interwinding Capacitance (Max) | DCR (Max) | |
|---|---|---|---|---|---|---|---|
| | | | | | | pri | sec |
| Tx | 75Ω | 1:2 | 720uH | 0.3uH | 30pF | 0.6Ω | 1.2Ω |
| | 120Ω | 1:2.2 | 720uH | 0.3uH | 30pF | 0.6Ω | 1.3Ω |
| Rx | | 1:2 | 1.2mH | 0.3uH | 30pF | 0.6Ω | 1.2Ω |

### Reference current circuit

To determine input reference current, connect 12kΩ±1% resistor.

AK2548

BGREF

R1

R1=12kΩ±1%
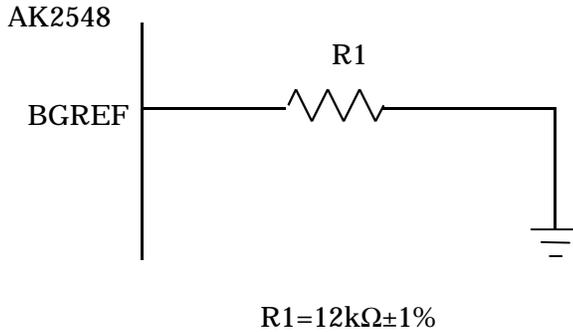
### Power Supply

To attenuate the power supply noise, connect capacitors between VDD and VSS respectively.

The value of the capacitance AK2548 need depend on the condition of the power supply line.

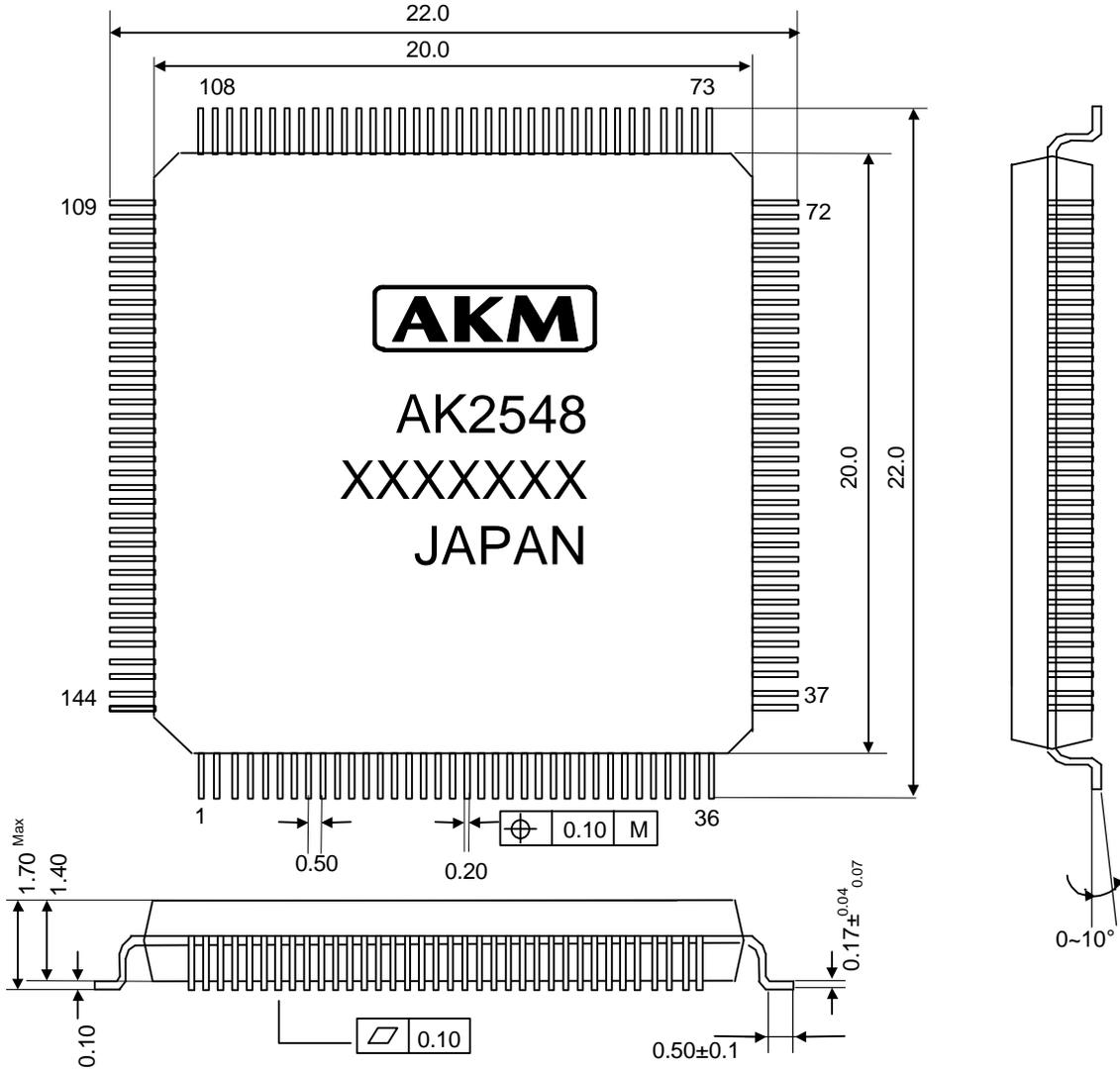Please decide the value of the capacitance after your evaluation.

AK2548

VDD

C1
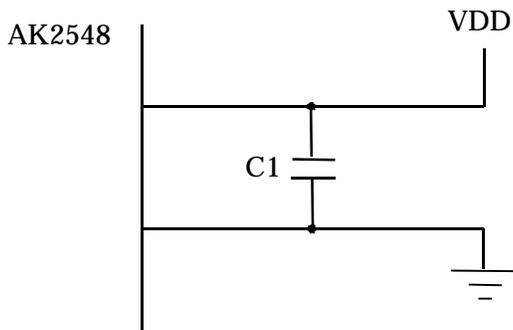
| Pin name | C1 |
|---|---|
| RAVDD1-RAVSS1, RAVDD2-RAVSS2, BVDD-BVSS, TAVDD1-TAVSS1, TAVDD2-TAVSS2 | 1uF |
| TVDD1-TVSS1, TVDD2-TVSS2, TVDD3-TVSS3, TVDD4-TVSS4, TVDD5-TVSS5, TVDD6-TVSS6, TVDD7-TVSS7, IOVDD1-IOVSS1, IOVDD2-IOVSS2, DVDD1-DVSS1, DVDD2-DVSS2, PVDD-PVSS | 0.01uF |

## PACKAGE

**144pin LQFP**

**OUTPUT DIMENSIONS**

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