



AK4309B

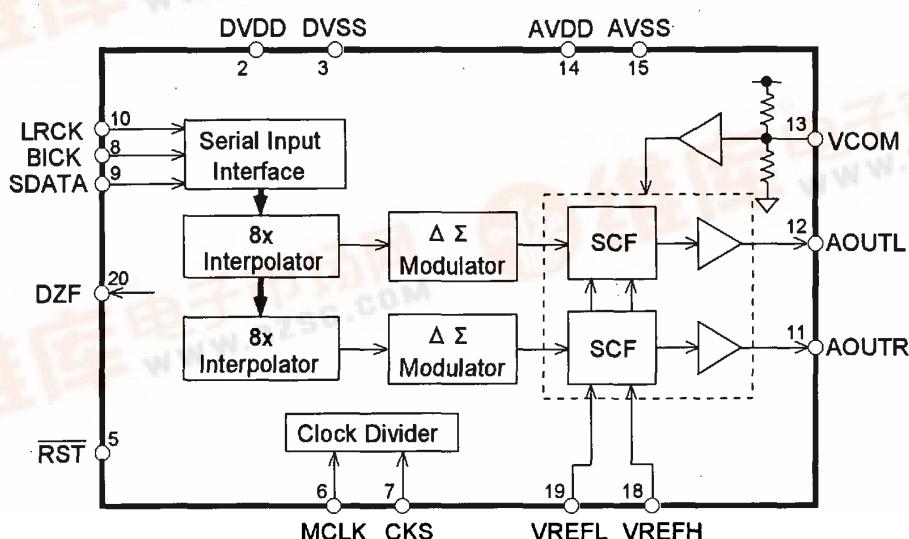
16Bit SCF DAC for Multimedia

General Description

The AK4309B is a 1bit stereo DAC for multimedia audio systems. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4309B, the loss of accuracy from clock jitter is also improved by using SCF techniques for on-chip post filter. The AK4309B includes continuous time filter with single end output and does not need any external parts. The master clock can be either 256fs or 384fs, supporting various audio environment.

Features

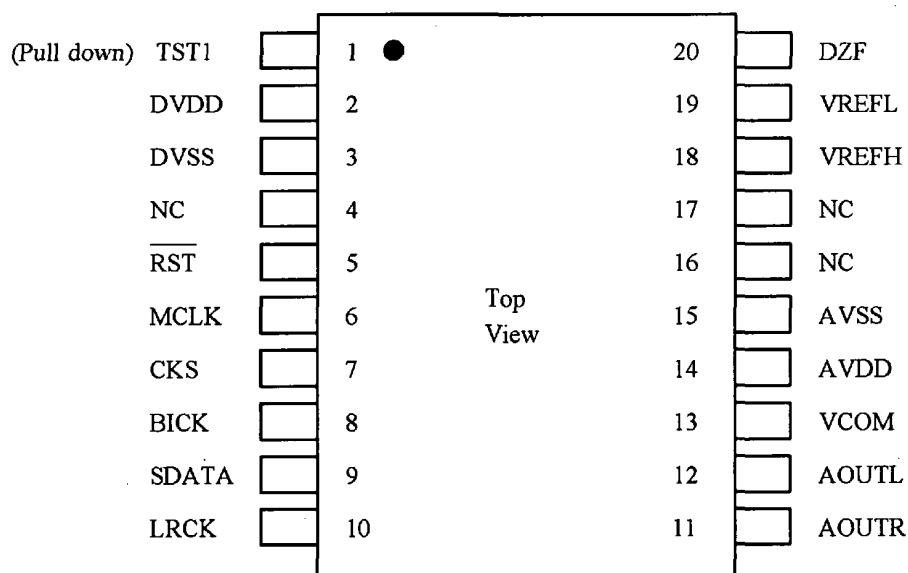
- Sampling Rate Ranging from 8kHz to 50kHz
- On chip Perfect filtering
 - 8 times FIR Interpolator
 - 2nd order SCF and CTF
 - Total Response: ± 0.5 dB at 20kHz
- On chip Buffer with Single End Output
- Master Clock: 256fs or 384fs
- High Tolerance to Clock Jitter
- TTL Level Digital Interface
- THD+N: -84dB
- Dynamic Range: 90dB
- Output Level: 3.4Vpp
- Power Supply: 5V $\pm 10\%$
- Low Power Dissipation: 80mW at 5V
- Small Package: 20pin SSOP
- Pin Compatible with AK4310/4309A



■ Ordering Guide

AK4309BVM -10~+70°C 20pin SSOP(0.65mm pitch)
 AKD4309B Evaluation Board
 (AK4309B's board is the same as AK4310's)

■ Pin Layout



■ Compatibility with AK4310/09A

Parameter	AK4310	AK4309A	AK4309B
Power Supply	3~5.5V	4.5~5.5V	4.5~5.5V
Digital I/F level	CMOS	TTL	TTL
DR	92dB	91dB	90dB
Output Voltage	2.8Vpp	3.4Vpp	3.4Vpp
Click Noise	High	Middle	Low
Function of Pin 4	<u>PD</u>	<u>PD</u>	NC
Package	24SSOP	24SSOP	20SSOP

PIN/FUNCTION			
No.	Pin Name	I/O	Function
1	TST1	I	Test Pin (Pull-down pin) Must be left floating or tied to DVSS.
2	DVDD	-	Digital Power Supply Pin
3	DVSS	-	Digital Ground Pin
4	NC	-	No Connection
5	<u>RST</u>	I	Reset Pin When at "L", the AK4309B is in power-down mode and is held in reset. The AK4309B should always be reset upon power-up.
6	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin. The fs is selected by CKS pin.
7	CKS	I	Master Clock Select Pin "L": MCLK=256fs, "H": MCLK=384fs
8	BICK	I	Serial Bit Input Clock Pin This clock is used to latch SDATA.
9	SDATA	I	Serial Data Input Pin 2's complement MSB-first data is input on this pin.
10	LRCK	I	L/R Clock Pin This input determines which channel is currently being input on the Serial Data Input pin, SDATA. "H": Lch, "L": Rch
11	AOUTR	O	Rch analog output pin
12	AOUTL	O	Lch analog output pin
13	VCOM	O	Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
14	AVDD	-	Analog Power Supply Pin
15	AVSS	-	Analog Ground Pin
16	NC	-	No Connection
17	NC	-	No Connection
18	VREFH	I	"H" Voltage Reference Input Pin The differential Voltage between VREFH and VREFL inputs set the analog output range. The VREFH pin is normally connected to AVDD and the VREFL pin is connected to AVSS. A 0.1uF ceramic capacitor should be as near to both pins.
19	VREFL	I	"L" Voltage Reference Input Pin
20	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".

* NC pins are not bonded internally.

ABSOLUTE MAXIMUM RATINGS				
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(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	DVDD-AVDD	VDA	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	± 10	mA
Input Voltage		VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1 . All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS					
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(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog (Note 2)	AVDD	4.5	5.0	5.5	V
	Digital	DVDD	4.5	5.0	AVDD	V
Voltage Reference(VREFH) (Note 3)		VREF	3.0	-	AVDD	V

Notes: 2 . AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.

3 . Analog output voltage scales with the voltage of VREFH at VREFL=AVSS.

AOUT(typ.@0dB)=3.4Vpp*VREFH/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS				
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($T_a=25^\circ C$; AVDD,DVDD=5.0V; VREFH=AVDD,VREFL=AVSS; $f_s=44.1\text{kHz}$; Signal Frequency=1kHz;
Measurement Bandwidth=10Hz~20kHz; $R_L \geq 10\text{k}\Omega$; unless otherwise specified)

Parameter	min	typ	max	Units
Resolution		16		Bits
Dynamic Characteristics (Note 4)				
THD+N (0dB Output)		-84	-79	dB
Dynamic Range (-60dB Output, A weight)	85	90		dB
S/N (A weight)	85	90		dB
Interchannel Isolation(1kHz)	80	90		dB
DC Accuracy				
Interchannel Gain Mismatch		0.15	0.3	dB
Gain Drift (Note 5)		60	-	ppm/ $^\circ C$
DC Accuracy				
Output Voltage (Note 6)	3.23	3.4	3.57	Vpp
Load Resistance	10			$\text{k}\Omega$
Power Supplies				
Power Supply Current				
Normal Operation ($\overline{\text{RST}} = \text{"H"}$)				
AVDD		13	18	mA
DVDD		3	5	mA
Power-Down-Mode ($\overline{\text{RST}} = \text{"L"}$)				
AVDD+DVDD (Note 7)		10	50	uA
Power Dissipation (AVDD+DVDD)				
Normal Operation		80	115	mW
Power-Down-Mode (Note 7)		50	250	uW
Power Supply Rejection (Note 8)		50		dB

Notes: 4 . Measured by AD725C(SHIBASOKU). Averaging mode. Refer to the eva board manual.

5 . The voltage on VREFH pin is held +5V externally.

6 . Full-scale voltage(0dB). Output voltage scales with the voltage of VREH-VREFL.

$$A_{\text{OUT}}(\text{typ.}@0\text{dB})=3.4\text{Vpp}*(\text{VREFH}-\text{VREFL})/5.$$

7 . Power Dissipation in the power-down mode is applied with no external clocks
(MCLK,BICK,LRCK held "H" or "L").

8 . PSR is applied to AVDD,DVDD with 1kHz, 100mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS					
Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband -0.2dB (Note 9) -6.0dB	PB	0 -	22.05	20.0 -	kHz kHz
Stopband (Note 9)	SB	24.3			kHz
Passband Ripple	PR			±0.05	dB
Stopband Attenuation	SA	41			dB
Group Delay (Note 10)	GD	-	14.5	-	1/fs
Digital Filter + SCF + CTF					
Frequency Response 0~20.0kHz		-	±0.5	-	dB

Note: 9 . The passband and stopband frequencies scale with fs.

For example, PB=0.4535*fs(@-0.2dB), SB=0.55*fs.

10 . The calculating delay time which occurred by digital filtering. This time is from setting the 16bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS					
Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-100A)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100A)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	uA

(Ta=25°C; AVDD,DVDD=4.5~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-100A)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100A)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	uA

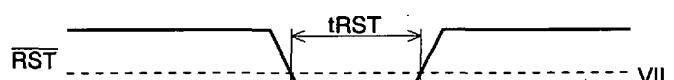
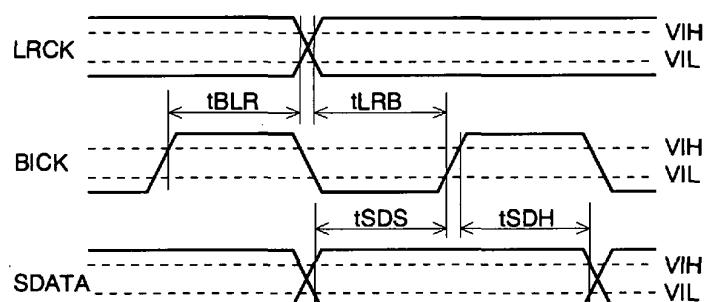
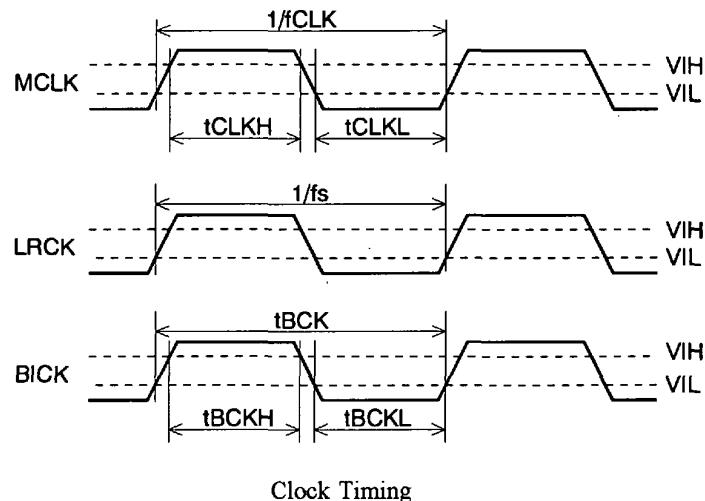
SWITCHING CHARACTERISTICS					
(Ta=25°C; AVDD,DVDD=4.5~5.5V; CL=20pF)					
Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
256fs:	fCLK	2.048		12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.072		19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK					
Frequency	fs	8	44.1	50	kHz
Duty Cycle	Duty	45		55	kHz
Serial Interface Timing					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
BICK rising to LRCK edge (Note 11)	tBLR	50			ns
LRCK Edge to BICK rising (Note 11)	tLRB	50			ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Reset Timing					
RST Pulse Width (Note 12)	tRST	150			ns

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
256fs:	fCLK	2.048		12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.072		19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK					
Frequency	fs	8	44.1	50	kHz
Duty Cycle	Duty	45		55	kHz
Serial Interface Timing					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
BICK rising to LRCK edge (Note 11)	tBLR	50			ns
LRCK Edge to BICK rising (Note 11)	tLRB	50			ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Reset Timing					
RST Pulse Width (Note 12)	tRST	150			ns

Notes: 11 . BICK rising edge must not occur at the same time as LRCK edge.

12 . The AK4309B can be reset by bringing $\overline{\text{RST}}$ "L" to "H" only upon power up.

■ Timing Diagram



OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4309B are MCLK, LRCK, BICK. The master clock(MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCLK is determined by the sampling rate (LRCK), CKS pin. Table 1 illustrates corresponding clock frequencies. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Refer to Figure 1 .

All external clocks(MCLK,BICK,LRCK) should always be present whenever the AK4309B is in normal operation mode(RST="H"). If these clocks are not provided, the AK4309B may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4309B should be in the power-down mode(RST ="L"). After exiting reset at power-up etc., the AK4309B is in power-down mode until MCLK and LRCK are input.

Clock	frequency
LRCK (fs)	8k~50kHz
BICK	~64fs
MCLK	CKS="L"
	256fs
MCLK	CKS="H"
	384fs

Table 1 . System Clocks

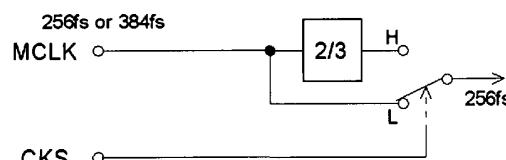


Figure 1 . MCLK divider

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. A serial data is MSB-first, 2's compliment format and is latched by the rising edge of BICK.

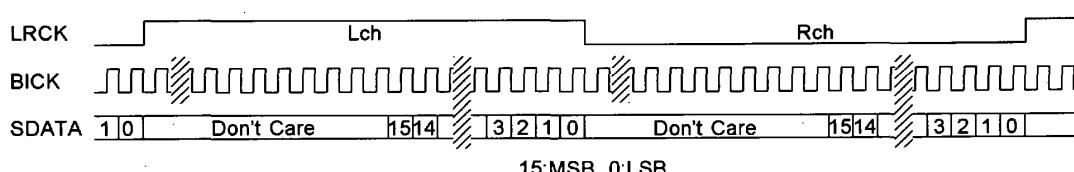


Figure 2 . Data Input Timing

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

■ System Reset

The AK4309B should be reset once by bringing RST "L" upon power-up. The AK4309B is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4309B is in power-down mode until LRCK is input.

SYSTEM DESIGN

Figure 3 shows the system connection diagram. An evaluation board[AKD4310] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

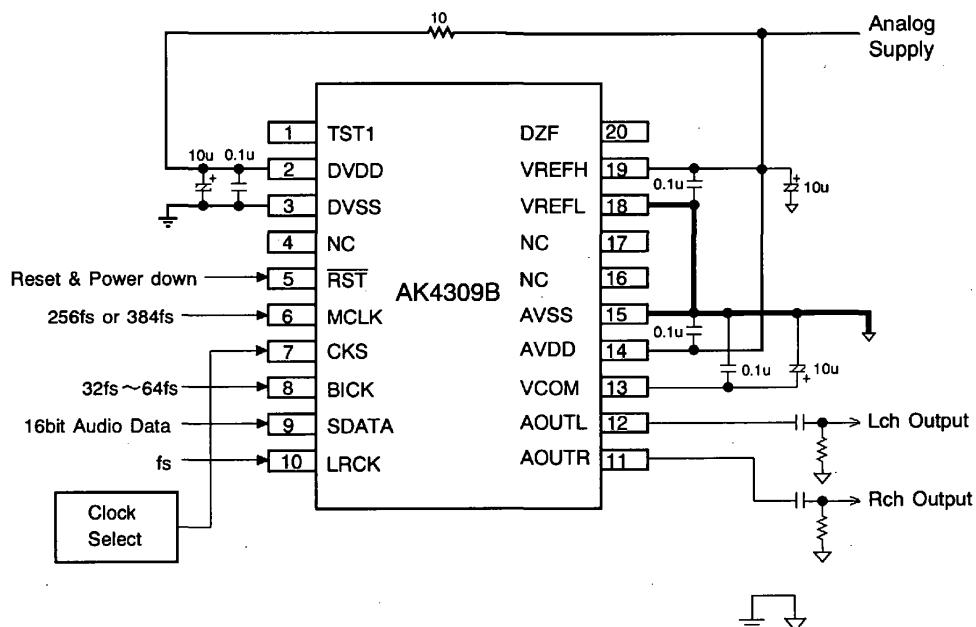


Figure 3 . Typical Connection Diagram

Notes:

- LRCK=fs, BICK≥32fs, MCLK=256fs at CKS="L", MCLK=384fs at CKS="H".
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- The capacitor value on VCOM depends on low frequency noise level of power supply.

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor as shown in Figure 3 . Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is connected to AVSS with a $0.1\mu F$ ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor of around $10\mu F$ in parallel with a $0.1\mu F$ ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4309B.

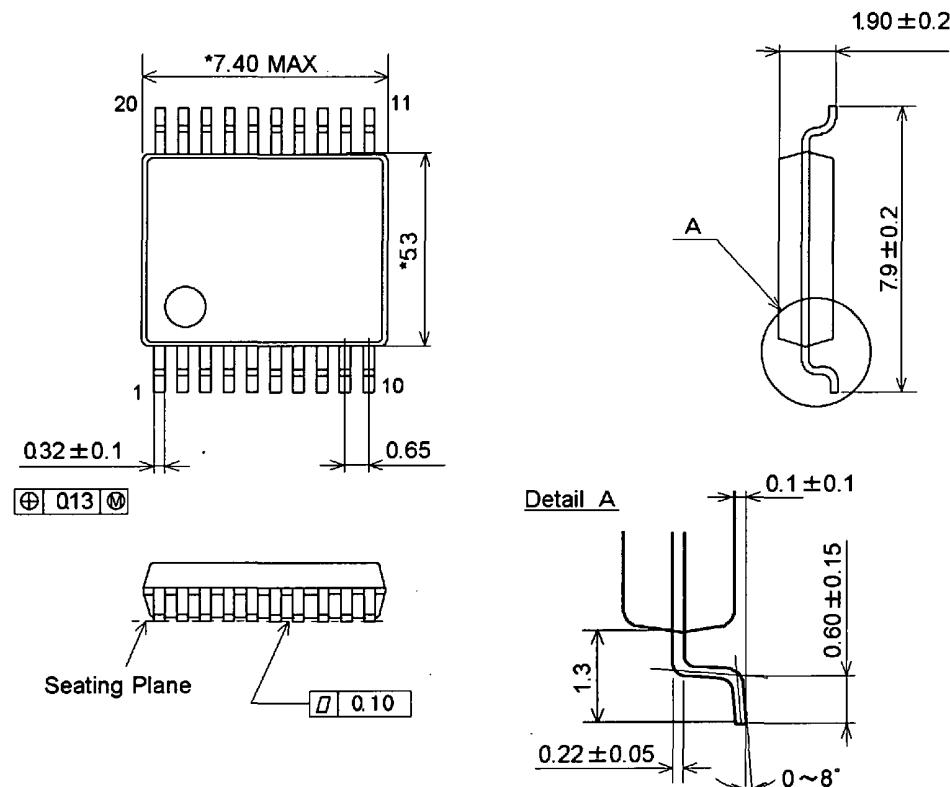
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 3.4Vpp. AC coupling capacitors of larger than $1\mu F$ are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

● 20pin SSOP (Unit: mm)

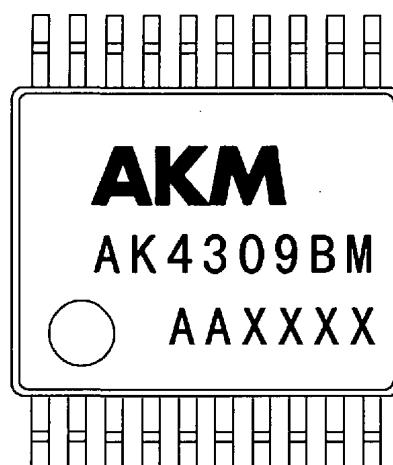


NOTE: Dimension ** does not include mold flash.

■ Package & Lead frame material

Package molding compound : Epoxy
 Lead frame material : Cu
 Lead frame surface treatment : Solder plate

MARKING



Contents of AAXXXX

AA: Lot#

XXXX: Date Code

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