AKD4523

Evaluation board Rev.A for AK4523

General description

AKD4523 is an evaluation board for audio codec, AK4523. A/D converter and D/A converter can be evaluated separately in addition to loopback mode(A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards(AKD4319, AKD4320, AKD4321 and AKD4324) directly. The AKD4523 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards(AKD5391/2, AKD5330 and AKD5351/2). Therefore, it is easy to evaluate the D/A section. The AKD4523 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector

■ **Ordering guide**

AKD4523 --- Evaluation board of AK4523

Function

- ☐ On-Board analog input buffer circuit
- ☐ On-board clock generator
- ☐ Compatible with the following 2 types of interface
  - 1)Direct interface with AKM's A/D and D/A converter, direct interface with a signal generator(AKD43XX) by 10pin Header
  - 2)DIR/DIT with optical input/output
- ☐ A BNC connector for an external clock input

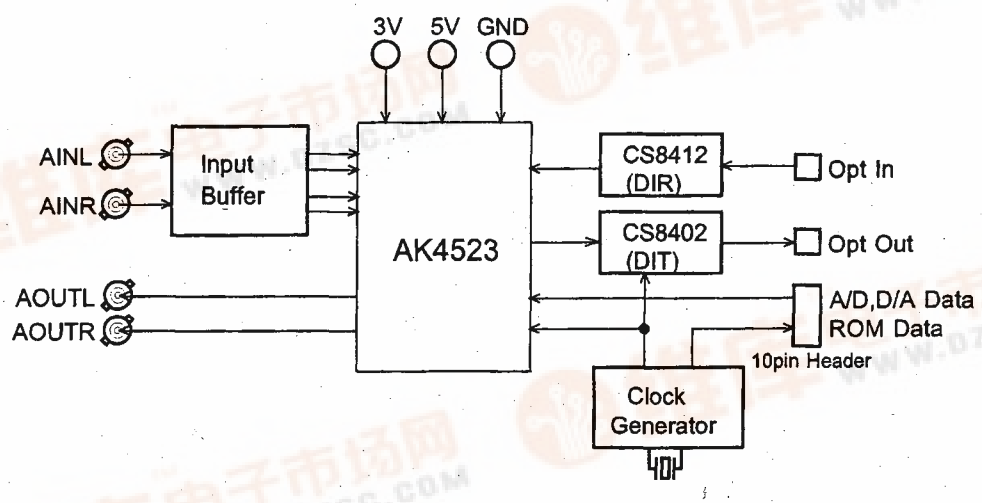
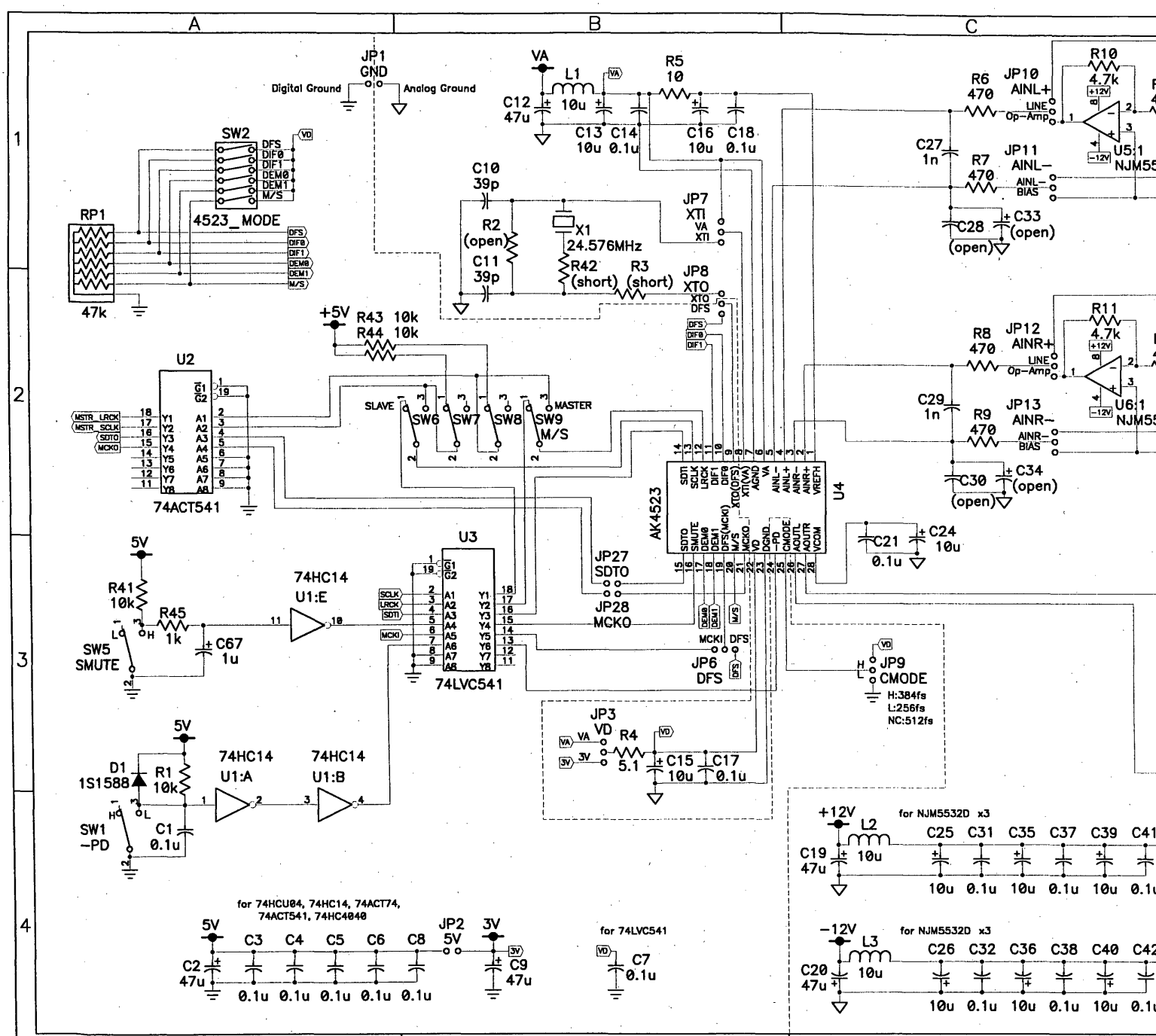
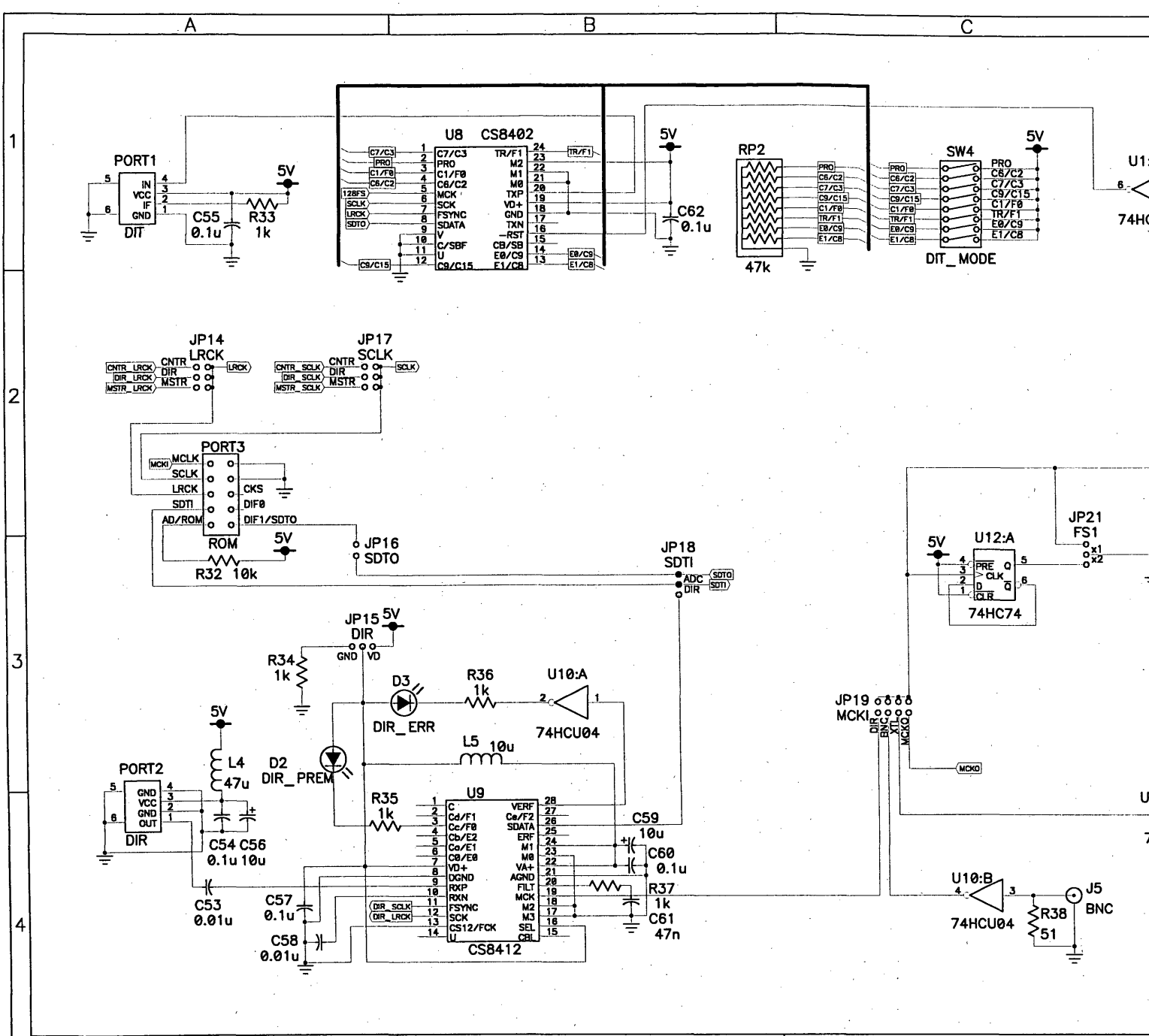


Figure 1. AKD4523 Block Diagram


A
B
C
1
2
3
4
JP1
GND
Digital Ground
Analog Ground
VA
L1
10u
C12
47u
C13
10u
C14
0.1u
R5
10
C16
10u
C18
0.1u
SW2
DFS
DIF0
DIF1
DEM0
DEM1
M/S
4523_MODE
RP1
47k
C10
39p
R2
(open)
C11
39p
X1
24.576MHz
R42
(short)
R3
(short)
JP7
XTI
JP8
XTO
DFS
+5V
R43 10k
R44 10k
U2
74ACT541
MSTR_LRCK
MSTR_SCLK
SDTO
MCKO
SLAVE
SW6
SW7
SW8
SW9
M/S
MASTER
U4
AK4523
SDTI
SCLK
LRCK
DIF1
DIF0
DEM1
DFS(MCKI)
M/S
MCKO
VD
DGND
-PD
CMODE
AOUTL
AOUTR
VCOM
XTO(DFS)
XTI(VA)
AGND
VA
AINL-
AINL+
AINR-
AINR+
VREFH
C21
0.1u
C24
10u
5V
R41
10k
R45
1k
SW5
SMUTE
C67
1u
74HC14
U1:E
U3
74LVC541
JP27
SDTO
JP28
MCKO
MCKI
DFS
JP6
DFS
JP9
CMODE
H:384fs
L:256fs
NC:512fs
JP3
VD
R4
5.1
C15
10u
C17
0.1u
D1
1S1588
R1
10k
C1
0.1u
SW1
-PD
74HC14
U1:A
74HC14
U1:B
R6
470
JP10
AINL+
LINE
Op-Amp
R10
4.7k
+12V
-12V
U5:1
NJM55
C27
1n
R7
470
JP11
AINL-
AINL-
BIAS
C28
(open)
C33
(open)
R8
470
JP12
AINR+
R11
4.7k
U6:1
C29
1n
R9
470
JP13
AINR-
C30
(open)
C34
(open)
+12V
L2
C19
47u
10u
for NJM5532D x3
C25
C31
C35
C37
C39
-12V
L3
C20
47u
C26
C32
C36
C38
C40
for 74HCU04, 74HC14, 74ACT74,
74ACT541, 74HC4040
5V
JP2
5V
3V
C2
47u
C3
C4
C5
C6
C8
C9
47u
0.1u
for 74LVC541
C7
0.1u


A
B
C
1
2
3
4
PORT1
IN
VCC
IF
GND
DIT
C55
0.1u
R33
1k
5V
U8 CS8402
C7/C3
PRO
C1/F0
C6/C2
128FS
SCLK
LRCK
SDTO
C9/C15
PRO
M2
M1
M0
TXP
VD+
GND
TXN
-RST
CB/SB
E0/C9
E1/C8
TR/F1
C62
0.1u
RP2
47k
SW4
DIT_MODE
JP14
LRCK
JP17
SCLK
CNTR
DIR
MSTR
PORT3
MCLK
SCLK
LRCK
SDTI
AD/ROM
CKS
DIF0
DIF1/SDTO
ROM
R32 10k
JP16
SDTO
JP18
SDTI
ADC
DIR
JP15
DIR
GND
VD
R34
1k
D3
DIR_ERR
R36
1k
U10:A
74HCU04
L5 10u
D2
DIR_PREM
PORT2
L4
47u
C54 C56
0.1u 10u
C53
0.01u
R35
1k
U9
C57
0.1u
C58
0.01u
C59
10u
C60
0.1u
R37
1k
C61
47n
CS8412
JP21
FS1
x1
x2
U12:A
74HC74
JP19
MCKI
MCKO
U10:B
74HCU04
J5
BNC
R38
51

■ Analog Inputs

The ADC inputs are differential and internally biased to the common voltage(VA/2) with 30k Ω (typ) resistance. The signal can be input from either positive or negative input, and the input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. The AK4523 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative full scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

1. In case of Full-Differential Inputs (default)

Non-inverted and inverted signal are input to AK4523 via inverted op-amp. Since gain of 1st op-amp is 0.24, maximum ampletude of the input signal can be about 4 times larger than spec of AK4523.

[JP10, JP12]	: Op-amp	C28, C30, C33, C34	: None
[JP11]	: AINL-	C27, C29	: 1nF
[JP13]	: AINR-		

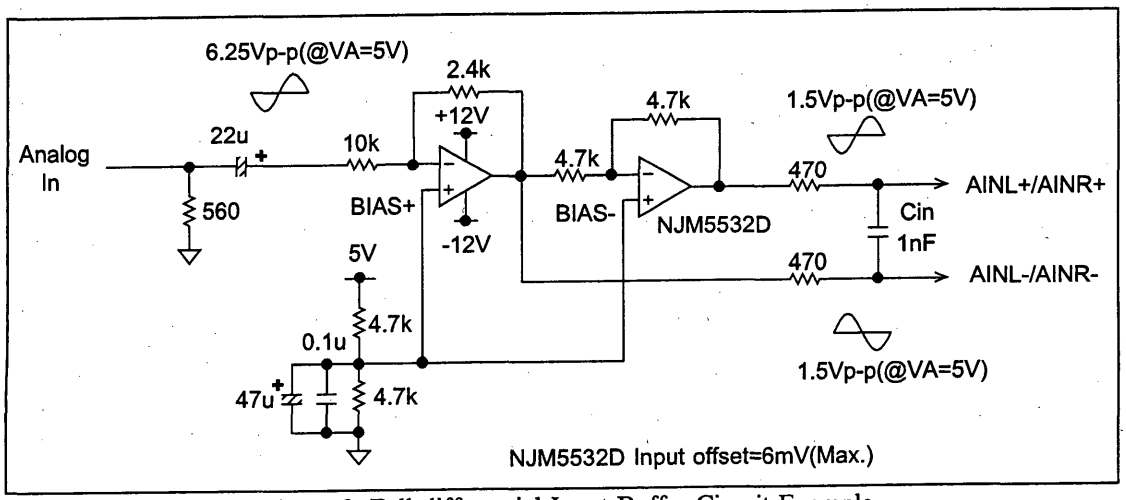


Figure 2. Full-differential Input Buffer Circuit Example

2. In case of Single-ended Input (bias voltage input)

In case of worrying Idle Tone Level, adds offset from external and moves it outside the audio band frequency. The difference between bias voltage of Op-amp and bias voltage(VA/2) of internal device results in the offset. Two inverted op-amps are connected on the evaluation board, however, do not need 2nd op-amp. In this case, if inverted op-amp is input to AINL- or AINR- pin, can be corresponded with polarity. Since gain of 1st op-amp is 0.24, maximum ampletude of the input signal can be about 4 times larger than spec of AK4523.

[JP10, JP12]	: Op-amp	C28, C30, C33, C34	: None
[JP11]	: BIAS	C27, C29	: 1nF
[JP13]	: BIAS		

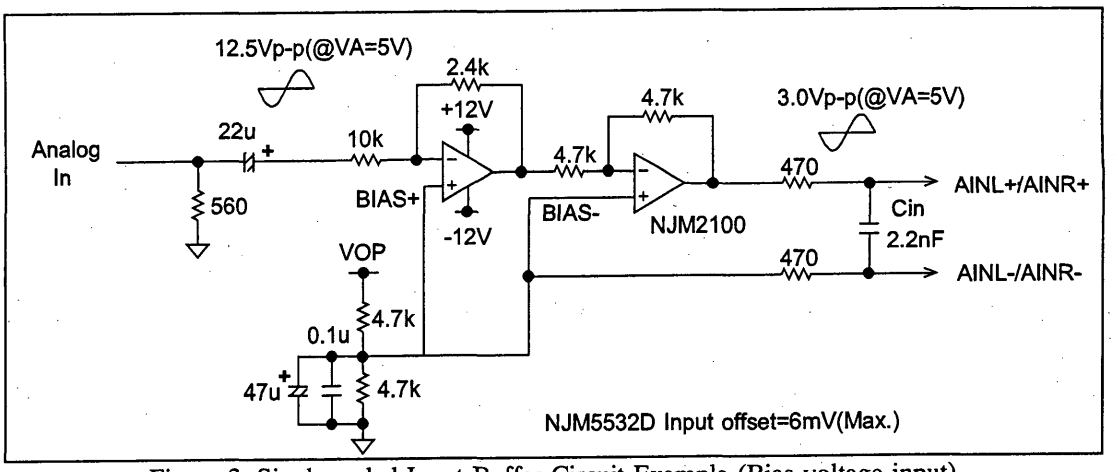


Figure 3. Single-ended Input Buffer Circuit Example (Bias voltage input)

3. In case of Single-ended Input (no input bias)

Analog signal is directly input from BNC connector and this case can reduce the part of input buffer circuit. In case of comparing Full-differential Input circuit(Figure 2.) or Single-ended Input circuit (Figure 3.) with no input buffer circuit shown in Figure 4., external mute should be taken enough time as "pop" noise is large at reset.

[JP10, JP12]	: LINE	C28, C30	: 0.1uF
[JP11]	: BIAS	C33, C34	: 4.7uF
[JP13]	: BIAS	C27, C29	: 2.2nF

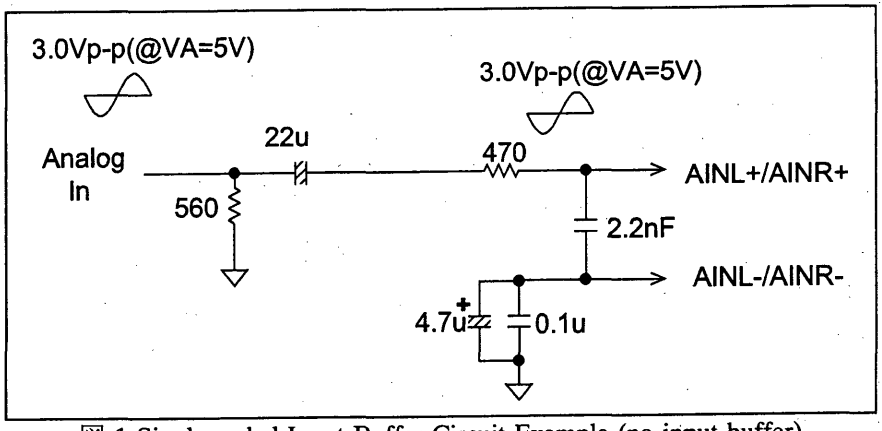


図 1 Single-ended Input Buffer Circuit Example (no input buffer)

■ Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.
DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

1. Output via non-inverted op-amp

Gain=6dB.

[JP25, JP26] : Op-amp

2. Output directly

[JP25, JP26] : LINE

■ Grounding and Power Supply Decoupling of AK4523

The AK4523 requires careful attention to power supply and grounding arrangements. VA pin and VD pin are usually supplied from analog supply in system. Alternatively if VA pin and VD pin are supplied separately, the power up sequence is not critical. AGND pin and DGND pin of the AK4523 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4523 as possible, with the small value ceramic capacitor being the nearest.

■ Voltage Reference Inputs of AK4523

The differential Voltage between VREFH pin and AGND pin sets the analog input/output range. VREFH pin is normally connected to VA pin with a 0.1uF ceramic capacitor. VCOM pin is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4523.

■ Operation sequence

① **Set up the power supply lines.**

[VA]	(red)	= 4.5 ~ 5.5V	(VA of AK4523)
[3V]	(orange)	= 2.7 ~ 5.5V	(VD of AK4523)
[5V]	(red)	= 3.5 ~ 5.5V	(Power supply to digital interface)
[+12V]	(orange)	= 12 ~ 15V	(Op-amp)
[-12V]	(blue)	= -12 ~-15V	(Op-amp)
[AGND]	(black)	= 0V	(AGND,DGND of AK4523 and Ground of analog interface)
[DGND]	(black)	= 0V	(Ground of digital interface)

Each supply line should be distributed from the power supply unit.

1. VD of AK4523 and Power supply to digital interface
   - In case of separated [JP2] : open
   - In case of common [JP2] : short
2. VA and VD of AK4523
   - In case of separated [JP3] : 3V
   - In case of common [JP3] : VA
3. Analog ground (includes AGND and DGND of AK4523) and digital ground
   - In case of separated [JP1] : open
   - In case of common [JP1] : short

② **Set up the evaluation modes and jumper pins.** (See p.7 ~)
There are many jumper pins to cover many evaluation mode. Please take care of setting.

③ **Set up the DIP-SW.**
SW2 : Set up AK4523 (See p.10)
SW4 : Set up CS8402 (See p.11)
(Upper side is "ON" and lower side is "OFF".)

④ **Power on.**
The AK4523 should be reset once bringing $\overline{PD}$ (SW1)"L" upon power-up.

■ Evaluation modes and jumper pins

Applicable Evaluation Mode

① Loopback mode (Default)
② Evaluation of D/A using ideal sine wave generated by ROM data.
③ Evaluation of D/A using A/D converted data
④ Evaluation of D/A using DIR(Optical Link)
⑤ Evaluation of A/D usingUsing D/A converted data
⑥ Evaluation of A/D DIT(Optical Link)
⑦ All interface signals including master clock are fed externally.

※① and ⑥ can be evaluated at the same time by the same set up.

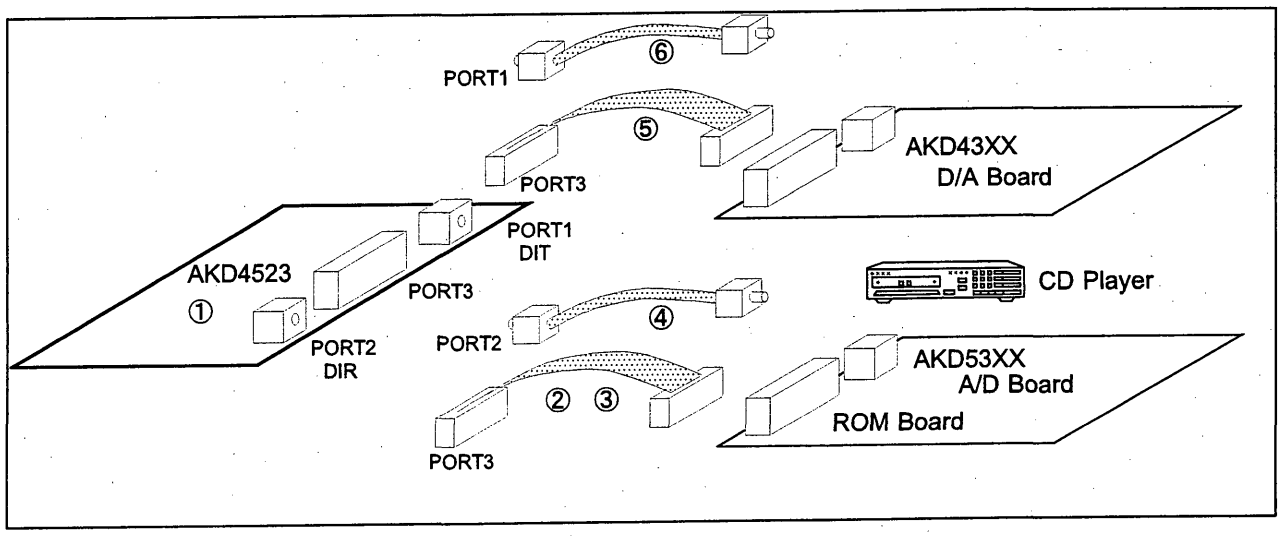


Figure 4. Wiring cables corresponded some evaluation modes

① **Loopback mode** (Default)
Nothing should be connected to PORT2, PORT3. If master clock is supplied from X2 in slave mode, set-up of each jumper switches is as follows. If supplied from except for X2, see Table 2.(p.9). In master mode, see Table 1.(p.8).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: ADC
[JP19] (MCKI)	: XTL	[JP17] (SCLK)	: ADC
[JP24] (XTE)	: open	[JP18] (SDTI)	: ADC

② **Evaluation of D/A using A/D converted data from ideal sine wave generated by ROM data**
Digital signals generated by AKD43XX are used. PORT3 is used for the interface with AKD43XX. Master clock is sent from AKD4523 to AKD43XX and SCLK, LRCK, SDATA are sent from AKD43XX to AKD4523. Nothing should be connected to PORT2. If master clock is supplied from X2, set-up of each jumper switches is as follows. If supplied from except for X2, see Table 2.(p.9). Set slave mode (see p.8 Table 1.).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: open
[JP19] (MCKI)	: XTL	[JP17] (SCLK)	: open
[JP24] (XTE)	: open	[JP18] (SDTI)	: open

③ **Evaluation of D/A using A/D converted data**

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391/2, AKD5330 and AKD5352/1) with PORT3. Master clock, SCLK, LRCK and SDATA are sent from A/D board to AKD4523. Nothing should be connected to PORT2. Set slave mode (see p.8 Table 1.).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: open
[JP19] (MCKI)	: open	[JP17] (SCLK)	: open
[JP24] (XTE)	: short	[JP18] (SDTI)	: open

④ **Evaluation of D/A using DIR (Optical Link)**

PORT2 is used. DIR generates MCLK, SCLK LRCK and SDATA from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT3. CS8412(DIR) needs the operating voltage of VD+≧ 3.2V. Set slave mode (see p.8 Table 1.).

[JP15] (DIR)	: VD	[JP14] (LRCK)	: DIR
[JP19] (MCKI)	: DIR	[JP17] (SCLK)	: DIR
[JP24] (XTE)	: short	[JP18] (SDTI)	: DIR

⑤ **Evaluation of A/D using D/A converted data**

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards (AKD4319, AKD4320 AKD4321 and AKD4324) with PORT3. Nothing should be connected to PORT2. If master clock is supplied from X2 in slave mode, set-up of each jumper switches is as follows. If supplied from except for X2, see Table 2.(p.9). In master mode, see Table 1.(p.8).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: ADC
[JP19] (MCKI)	: XTL	[JP17] (SCLK)	: ADC
[JP24] (XTE)	: open	[JP18] (SDTI)	: ADC

⑥ **Evaluation of A/D using DIT (Optical Link)**

PORT1 is used. DIT generates SDATA from received data and which is output through optical connector (TOTX174). It is possible to connect AKM's evaluation boards (AKD4319, AKD4320, AKD4321 and AKD4324), digital-amplifier and etc. Nothing should be connected to PORT2, PORT3. This set-up is same as that of ①. CS8402(DIT) needs the operating voltage of VD+≧ 3.2V. SW5 should be kept "H" during normal operation. If master clock is supplied from X2 in slave mode, set-up of each jumper switches is as follows. If supplied from except for X2, see Table 2.(p.9). In master mode, see Table 1. (p.8).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: ADC
[JP19] (MCKI)	: XTL	[JP17] (SCLK)	: ADC
[JP24] (XTE)	: open	[JP18] (SDTI)	: ADC

⑦ **All interfacing signals including master clock are fed externally.**

Under the following set-up, all external signals needed for the AK4523 to operate could be fed through PORT3. Set slave mode (see p.8 Table 1.).

[JP15] (DIR)	: GND	[JP14] (LRCK)	: open
[JP19] (MCKI)	: open	[JP17] (SCLK)	: open
[JP24] (XTE)	: short	[JP18] (SDTI)	: open

■ Master / Slave mode set-up

	Master mode	Slave mode (default)
SW2-6(M/S)	ON	OFF
SW6,7,8,9	Master	Slave
JP14, JP17	MSTR	See above

Table 1. Master / Slave mode set-up

■ Selection of master clock

	Internal clock (X1)	External clock (X2,J5,PORT2)
JP7	XTI	VA
JP8	XTO	DFS
JP6	DFS	MCKI

Table 2. Selection of master clock

Master clock is X2 at default.

■ Master clock set-up

		SW2 DFS	JP9 CMODE	JP21 FS1	JP22 FS2
Normal Speed	256fs	OFF	L	x1	x1
	512fs	OFF	open	x2	x1
Double Speed	128fs	ON	L	x1	x1/2
	256fs	ON	open	x1	x1

(default)

Table 3. Master clock set-up

In master mode, 128fs set-up cannot used.

■ SCLK set-up

SCLK can be selected 64fs or 32fs by JP23(SCLK). In master mode, set 64fs. SCLK is 64fs at default.

■ Other jumpers set-up

[JP27, JP27] : short (always)
[JP16] : open (always)

■ The function of the toggle SW.

[SW1] : Resets the AK4523. Keep "H" during normal operation.
[SW5] : Initiates soft mute cycle of AK4523. If this switch goes "H", soft mute cycle is initiated. Keep "L" during normal operation.
[SW3] : Resets the CS8402. "L" resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "H" during normal operation.
(Upper-side is "H" and lower-side is "L".)

■ The indication content for LED.

[D3] : Monitors VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.
[D2] : Indicates whether the input data of CS8412 is pre-emphasized or not. LED turns on when the data is pre-emphasized.

■ DIP switch set-up

[SW3] : This switch sets up the operation mode of the AK4523.
Confirm the set-up of the DIP-SW before evaluation starts.
Refer to AK4523 data-sheet about detail information. ON means "H" and OFF, "L".
Since formats of CS8402, CS8412 are fixed IIS(I2S), set DIF1,0 ON if use them.

No.	PIN	ON	OFF	default
1	DFS	Double Speed	Normal Speed	OFF
2	DIF0	Serial Data Interface Format Mode (See Table 5.)		ON
3	DIF1			ON
4	DEM0	De-emphasis filter control (See Table 6.)		ON
5	DEM1			OFF
6	M/S	Master mode	Slave mode	OFF

Table 4. Set-up of SW2(4523_MODE)

Mode	DIF1	DIF0	SDTO(ADC)	SDTI(DAC)	L/R	SCLK	
0	OFF	OFF	20bit, MSB justified	16bit, LSB justified	H/L	64fs, 32fs	
1	OFF	ON	20bit, MSB justified	20bit, LSB justified	H/L	64fs	
2	ON	OFF	20bit, MSB justified	20bit, MSB justified	H/L	64fs	
3	ON	ON	IIS(I2S)	IIS(I2S)	L/H	64fs, 32fs	(default)

Table 5. Serial Data Interface Format Mode

DFS	DEM1	DEM0	Mode	
OFF	OFF	OFF	44.1kHz	
OFF	OFF	ON	OFF	(default)
OFF	ON	OFF	48kHz	
OFF	ON	ON	32kHz	
ON	OFF	OFF	OFF	
ON	OFF	ON	OFF	
ON	ON	OFF	OFF	
ON	ON	ON	OFF	

Table 6. De-emphasis filter control

[SW4] : This switch sets the C-bit of CS8402. (Default is the consumer mode)
This set-up does not affect the evaluation of the AK4523. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=0	Professional mode, C0=1
2,3	$\overline{C6}$,$\overline{C7}$	C6,C7 - Sampling frequency
	1 1	00 - Not indicated. Receiver default to 48kHz.
	1 0	01 - 48kHz
	0 1	10 - 44.1kHz
	0 0	11 - 32kHz
4	$\overline{C9}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to
	0	2-channel mode.
		0100 - Stereophonic.
5	$\overline{C1}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Non-audio
6	TRNPT	Transparent mode * CS8402 is CRE
	0	Normal mode
	1	Transparent mode
8,7	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no
	1 0	emphasis with manual override enabled.
	0 1	100 - None
	0 0	110 - 50/15usec
		111 - CCITT J.17

Table 7. DIP switch set-up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
2	$\overline{C2}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
3	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
4	$\overline{C15}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
6,5	FC1,FC0	C24,C25,C26,C27- Sampling frequency
	0 0	0000 - 44.1kHz
Default	0 1	0100 - 48kHz
	1 0	1100 - 32kHz
	1 1	0000 - 44.1kHz, CD mode
8,7	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 8. DIP switch set-up of CS8402 (Consumer mode)

AK4523 Measurement Results

[Measurement Condition]

- Measurement unit : ROHDE & SCHWARZ, UPD04
- MCLK : 256fs
- BCLK : 64fs
- Bit : 20bit
- fs : 44.1kHz
- Power Supply : VA=5V, VD=5V/3V
- Interface : DIT/DIR
- Temperature : Room

1. A/D Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	92.2 dB	92.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	96.7 dB	96.9 dB
		20kLPF, A-weight	100.5 dB	100.7 dB
	1kHz, -60dB	20kLPF	96.7 dB	96.9 dB
		20kLPF, A-weight	100.0 dB	100.2 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.0 dB	97.3 dB
		20kLPF, A-weight	101.0 dB	101.1 dB

4. D/A Output

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	90.6 dB	90.7 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.1 dB
		20kLPF, A-weight	100.4 dB	100.5 dB
	1kHz, -60dB	20kLPF	97.1 dB	97.2 dB
		20kLPF, A-weight	100.6 dB	100.5 dB
S/N	1kHz, 0dB / "0"data IN	20kLPF	97.2 dB	97.3 dB
		20kLPF, A-weight	100.6 dB	100.6 dB

[Measurement Condition]
- Measurement unit : Audio Precision System two
- MCLK : 256fs
- BCLK : 64fs
- Bit : 20bit
- fs : 44.1kHz
- Power Supply : VA=5V, VD=5V/3V
- Interface : DIT/DIR
- Temperature : Room

1. A/D Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	94.7 dB	94.9 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.1 dB
		20kLPF, A-weight	99.8 dB	100.0 dB
	1kHz, -60dB	20kLPF	97.0 dB	97.2 dB
		20kLPF, A-weight	99.7 dB	100.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.1 dB	97.2 dB
		20kLPF, A-weight	100.1 dB	100.1 dB

2. A/D Output (Single-ended inputs with external bias, refer to Figure 3.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	80.8 dB	82.2 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.2 dB
		20kLPF, A-weight	99.8 dB	100.0 dB
	1kHz, -60dB	20kLPF	97.1 dB	97.4 dB
		20kLPF, A-weight	99.7 dB	100.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.3 dB	97.5 dB
		20kLPF, A-weight	100.1 dB	100.5 dB

3. A/D Output (Single-ended inputs without external bias, refer to Figure 4.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	79.7 dB	81.2 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.1 dB	97.3 dB
		20kLPF, A-weight	99.9 dB	100.2 dB
	1kHz, -60dB	20kLPF	97.2 dB	97.5 dB
		20kLPF, A-weight	100.2 dB	100.4 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.2 dB	97.6 dB
		20kLPF, A-weight	100.3 dB	100.6 dB

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	91.4 dB	91.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.0 dB
		A-weight	99.6 dB	99.6 dB
	1kHz, -60dB	20kLPF	97.0 dB	97.0 dB
		A-weight	99.5 dB	99.6 dB
S/N	1kHz,	20kLPF	97.0 dB	97.1 dB
	0dB / "0"data IN	A-weight	99.6 dB	99.7 dB

5. A/D→D/A Loopback Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	89.3 dB	89.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.5 dB	96.7 dB
S/N	1kHz, 0dB/GND IN	20kLPF	93.9 dB	93.9 dB
		A-weight	96.7 dB	96.7 dB

6. A/D→D/A Loopback Output (Single-ended inputs with external bias, refer to Figure 3.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	79.1 dB	80.3 dB
Dynamic Range	1kHz, -20dB	20kLPF	94.0 dB	94.0 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.4 dB	96.7 dB
S/N	1kHz, 0dB/GND IN	20kLPF	94.0 dB	94.1 dB
		A-weight	96.8 dB	96.9 dB

7. A/D→D/A Loopback Output (Single-ended inputs without external bias, refer to Figure 4.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	78.2 dB	79.4 dB
Dynamic Range	1kHz, -20dB	20kLPF	94.0 dB	94.1 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	94.0 dB	94.1 dB
		A-weight	96.9 dB	97.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	93.9 dB	94.0 dB
		A-weight	96.8 dB	97.0 dB

AK4523 ADC part

Conditions :

AVDD = DVDD = 5.0V

fs = 44.1kHz, MCLK = 256fs, BICK = 64fs,

Measurement unit = ROHDE & SCHWARZ UPD04

Interface = DIT

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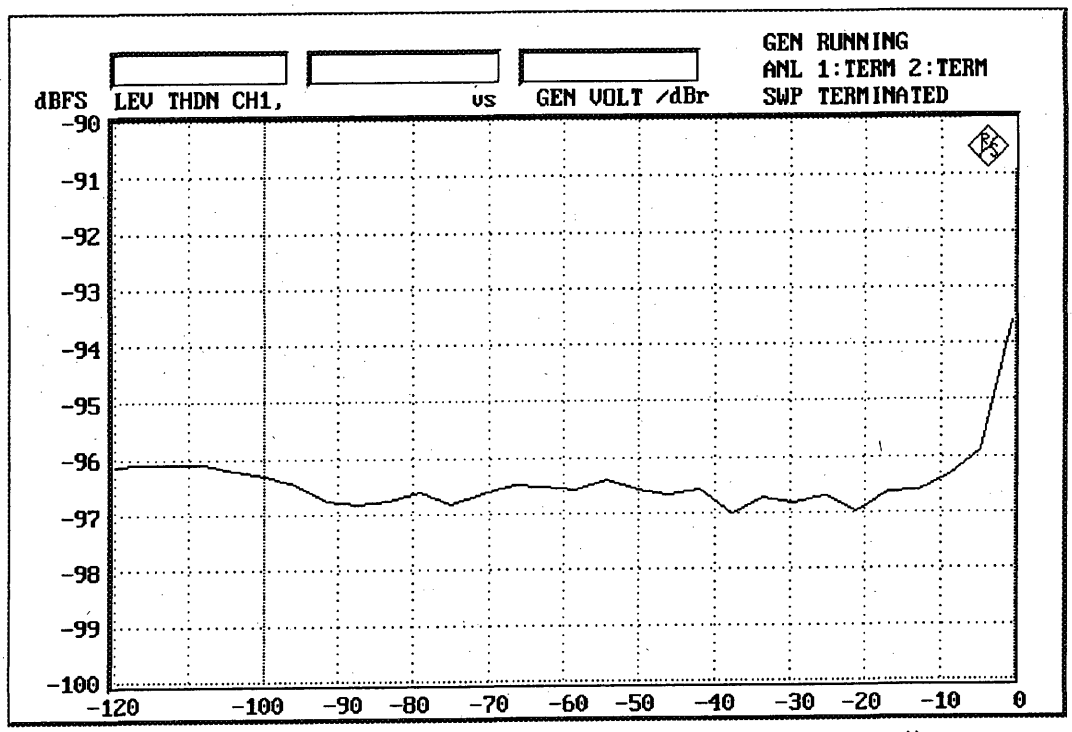


Figure 34 : THD+N vs. Input level (fin : 1kHz (Full-differential input))

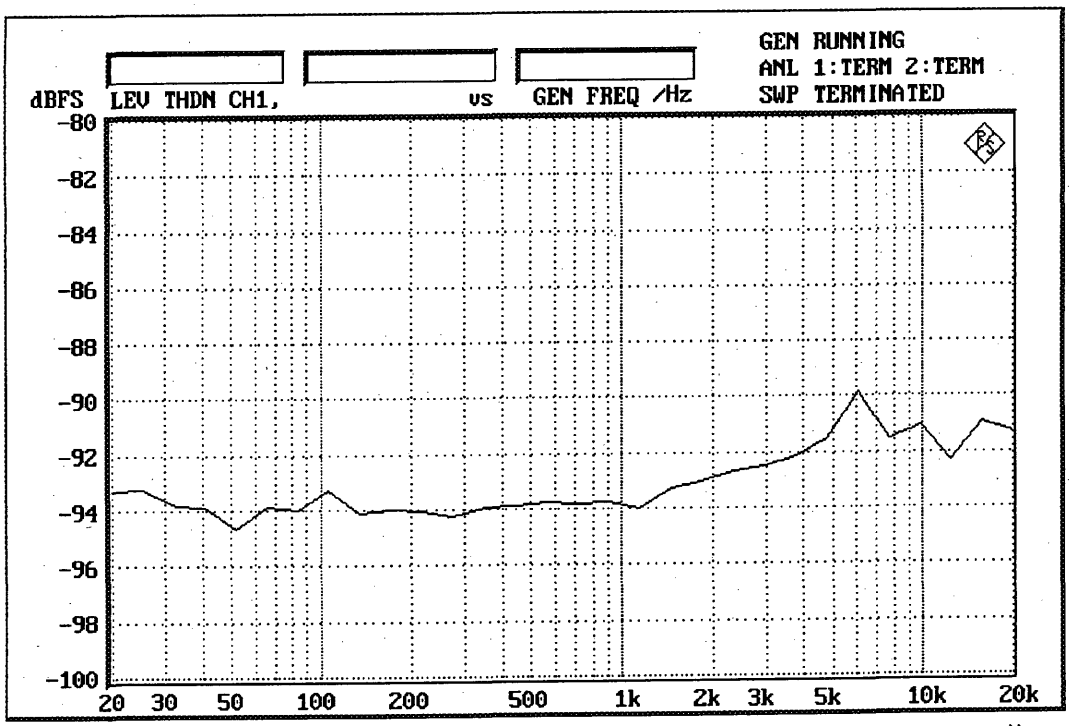


Figure 35 : THD+N vs. Input frequency (input level : −0.5dBFS (Full-differential input))

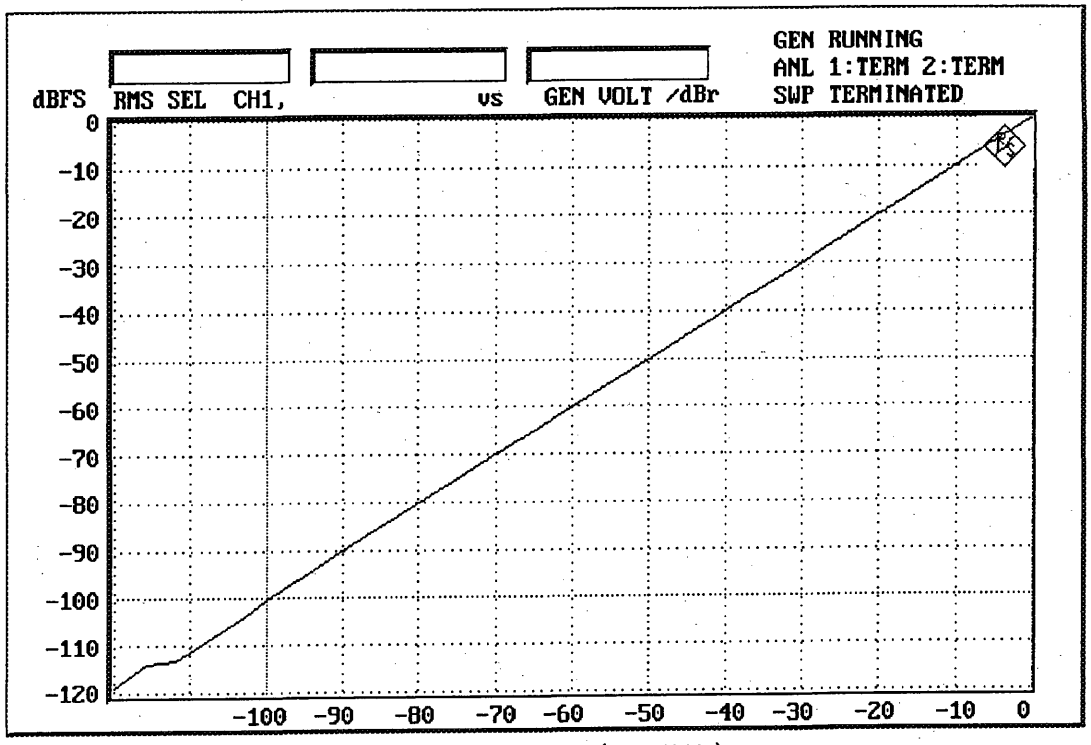


Figure 36 : Linearity (fin : 1kHz)

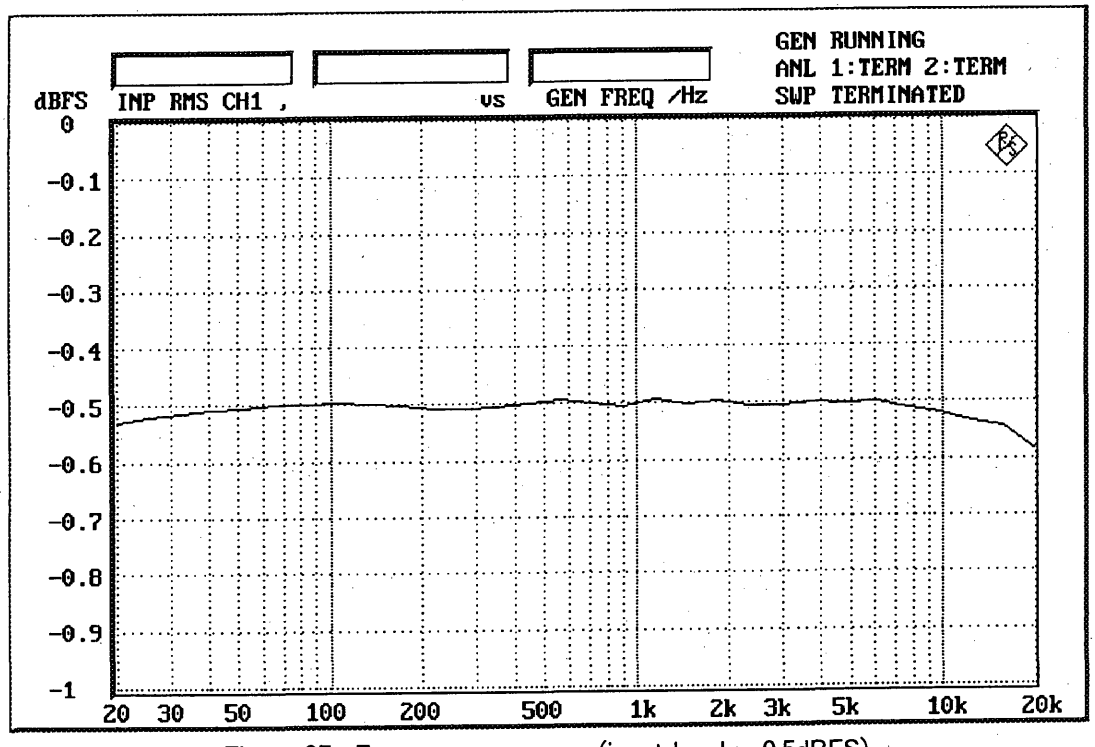


Figure 37 : Frequency response (input level : −0.5dBFS)

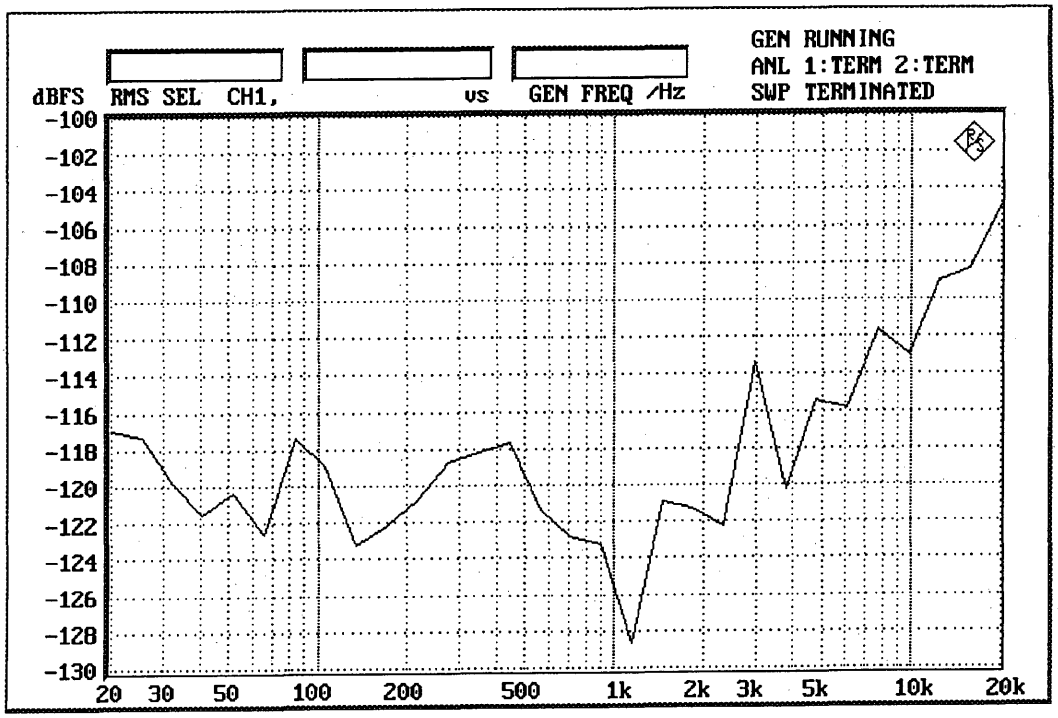


Figure 38 : Cross talk

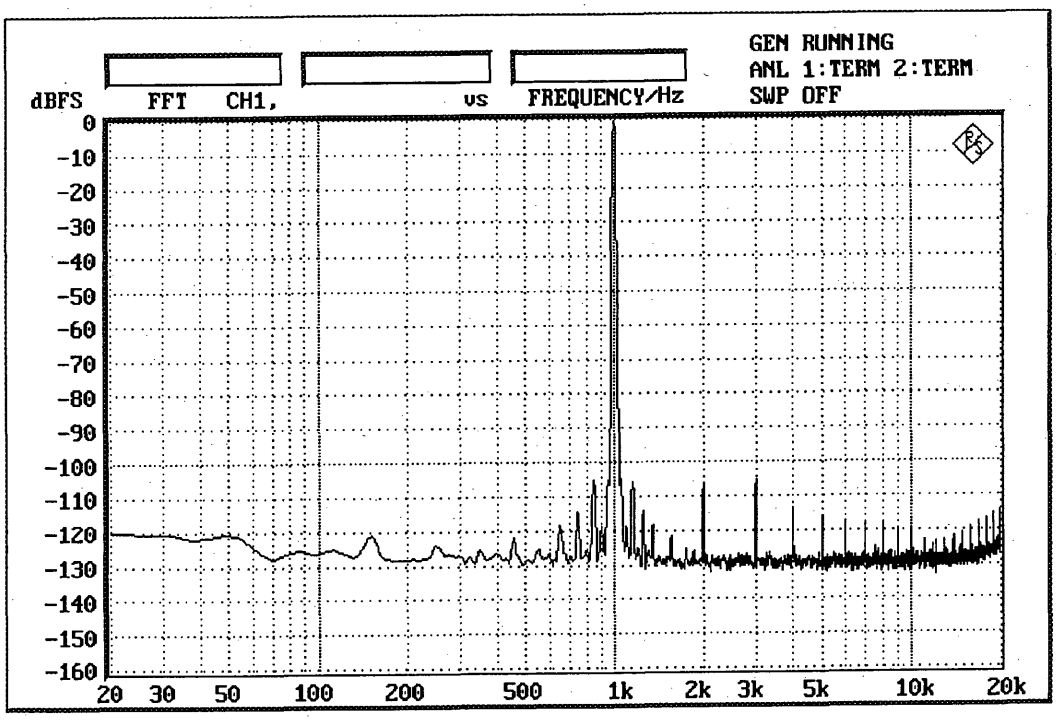


Figure 39 : FFT (Full-differential input : 1kHz, -0.5dBFS ;
FFT points : 8192, averaging : 10)

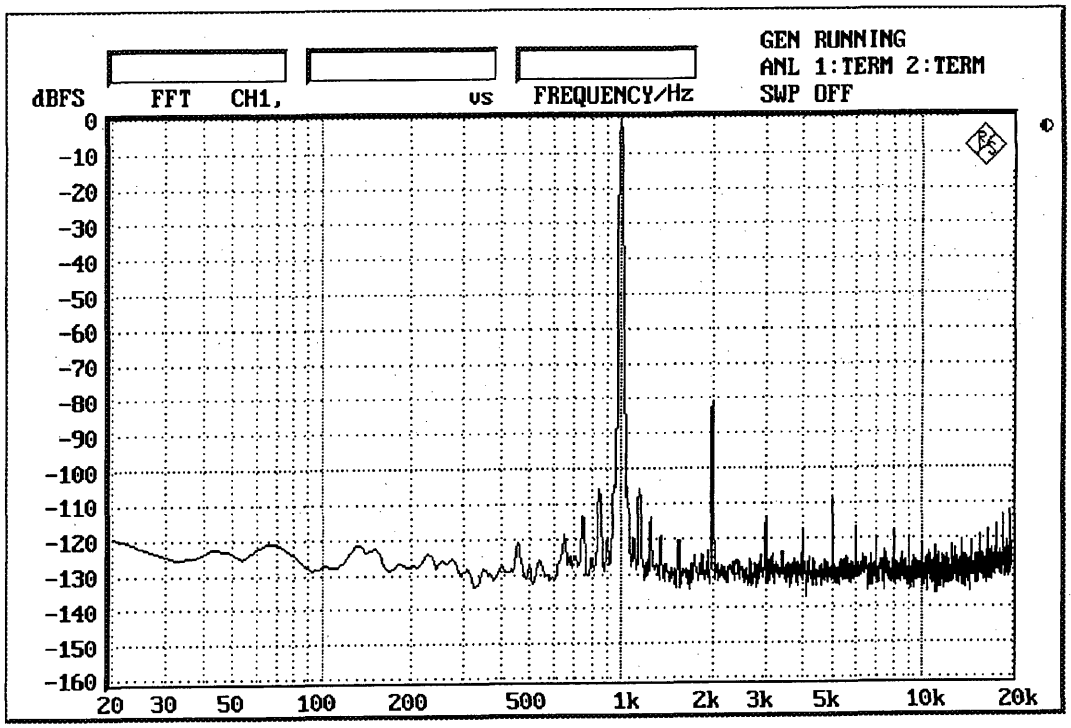


Figure 40 : FFT (Single-ended input(bias input) : 1kHz, -0.5dBFS ;
FFT points : 8192, averaging : 10)

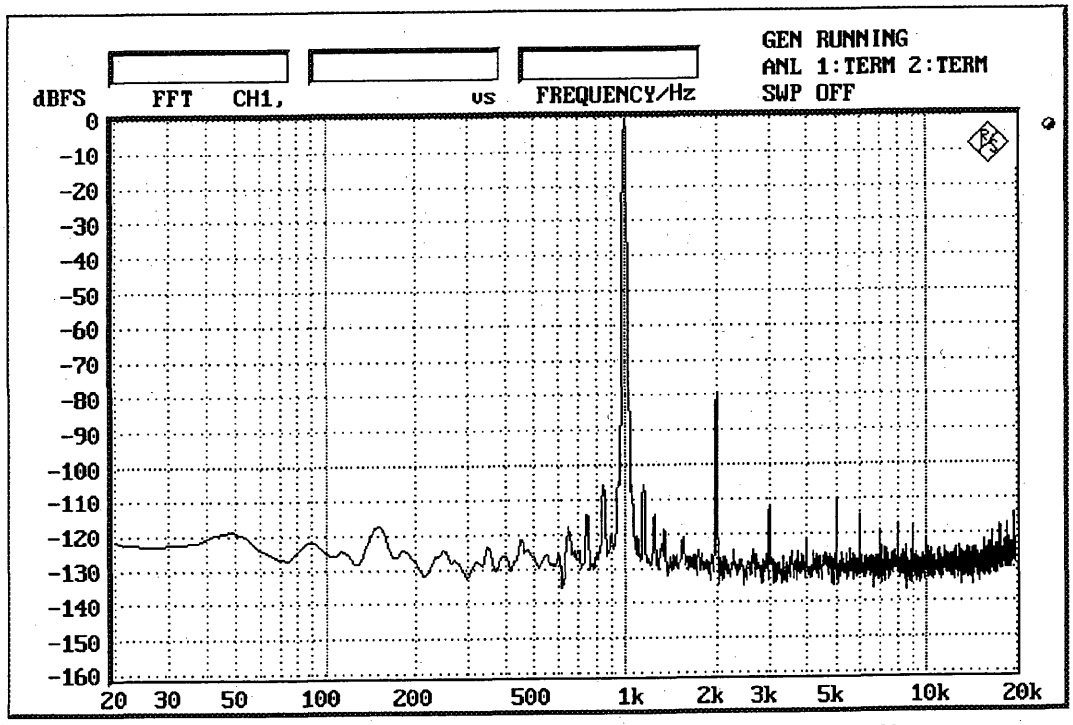


Figure 41 : FFT (Single-ended input (no bias) : 1kHz, -0.5dBFS ;
FFT points : 8192, averaging : 10)

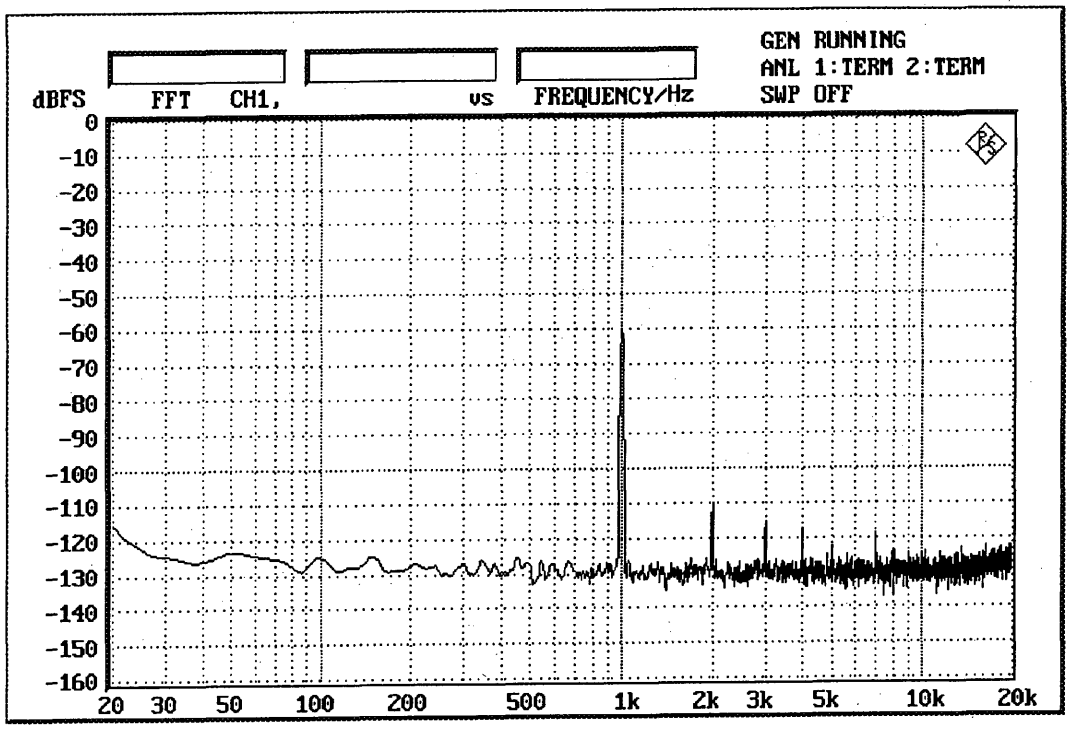


Figure 42 : FFT (Full-differential input : 1kHz, −60dBFS ;
FFT points : 8192, averaging : 10)

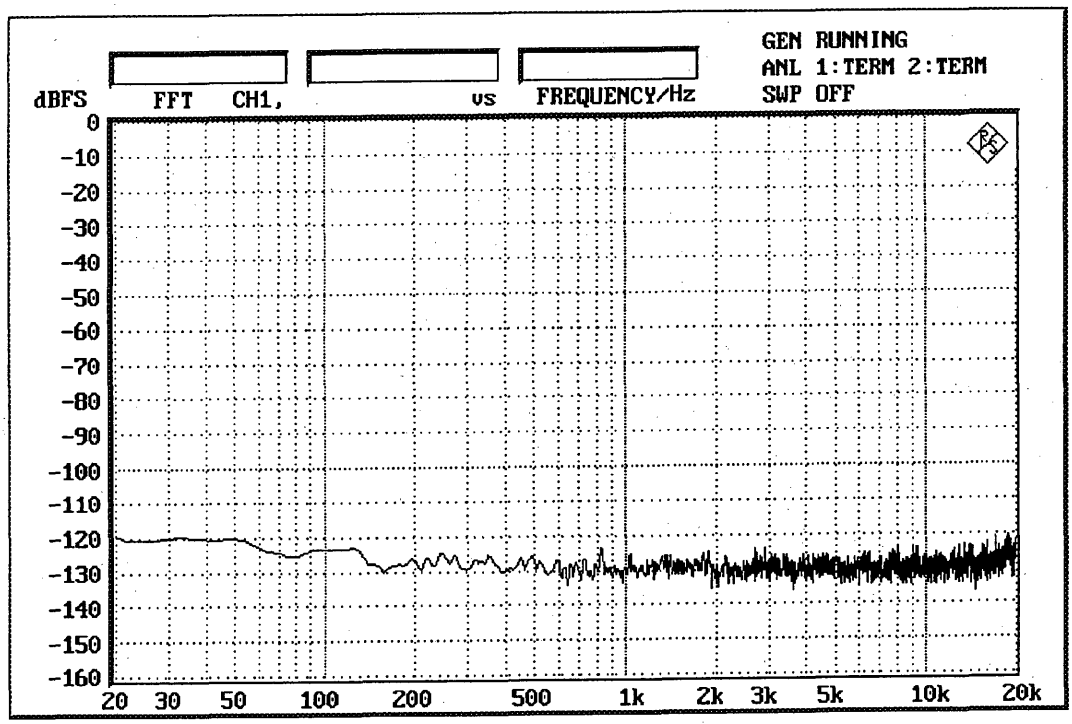


Figure 43 : FFT (noise floor ;
FFT points : 8192, averaging : 10)

AK4523 DAC part

Conditions :

AVDD = DVDD = 5.0V

fs = 44.1kHz, MCLK = 256fs, BICK = 64fs,

Measurement unit = ROHDE & SCHWARZ UPD04

Interface = DIR

Contents :

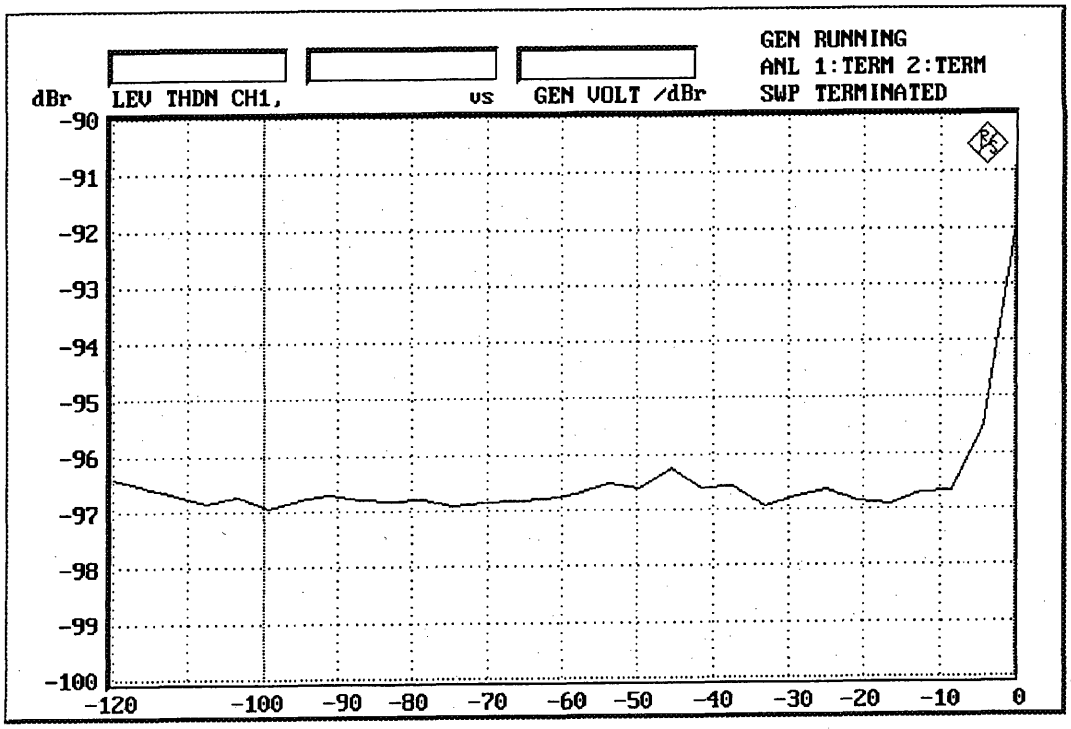


Figure 44 : THD+N vs. Input level (fin : 1kHz)

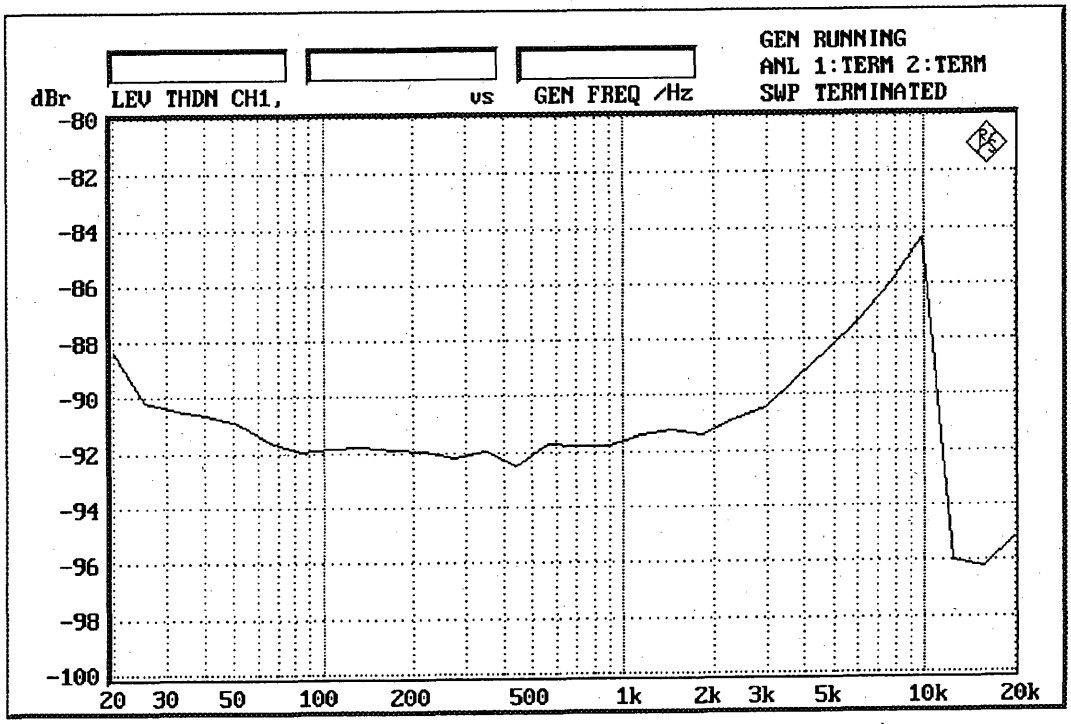


Figure 45 : THD+N vs. Input frequency (input level : 0dBFS)

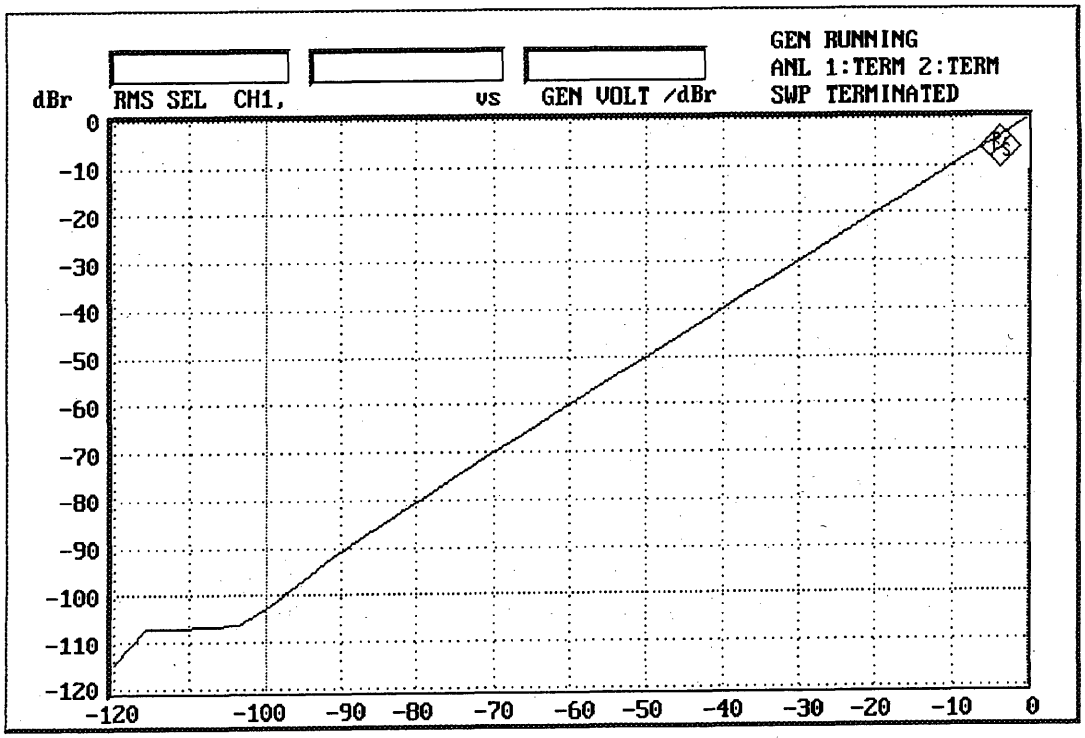


Figure 46 : Linearity (fin : 1kHz)

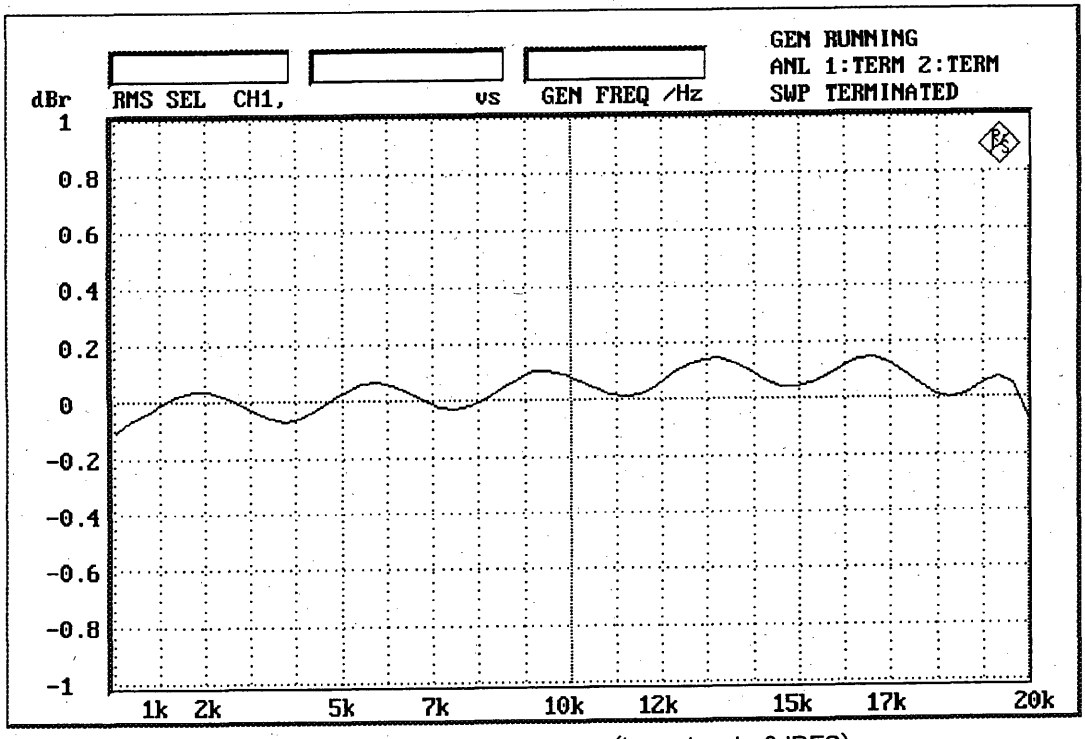


Figure 47 : Frequency response (input level : 0dBFS)

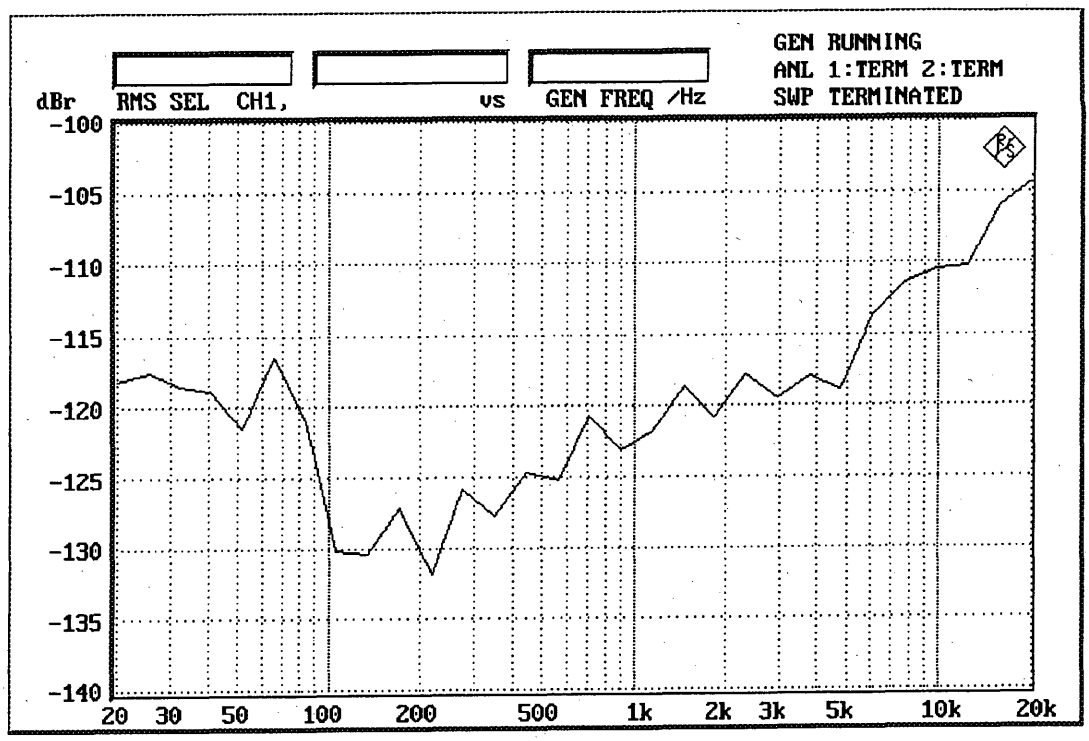


Figure 48 : Cross talk

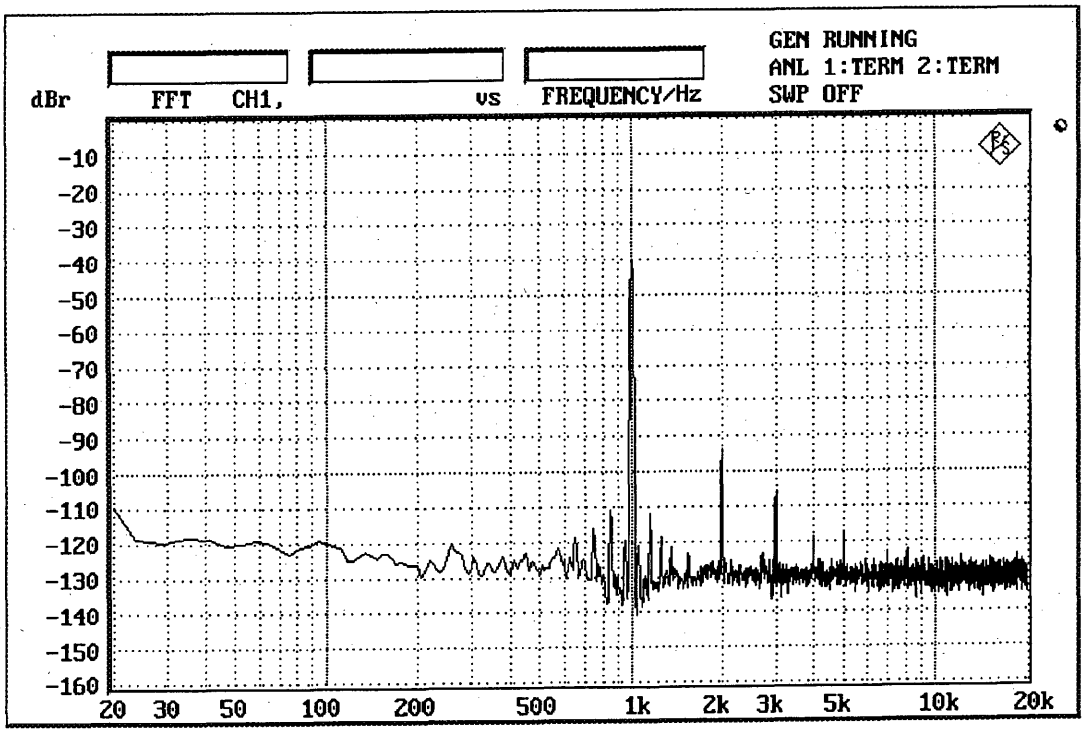


Figure 49 : FFT (input signal : 1kHz, 0dBFS ;

FFT points : 8192, averaging : 10, 30dBFS Notch filter : on)

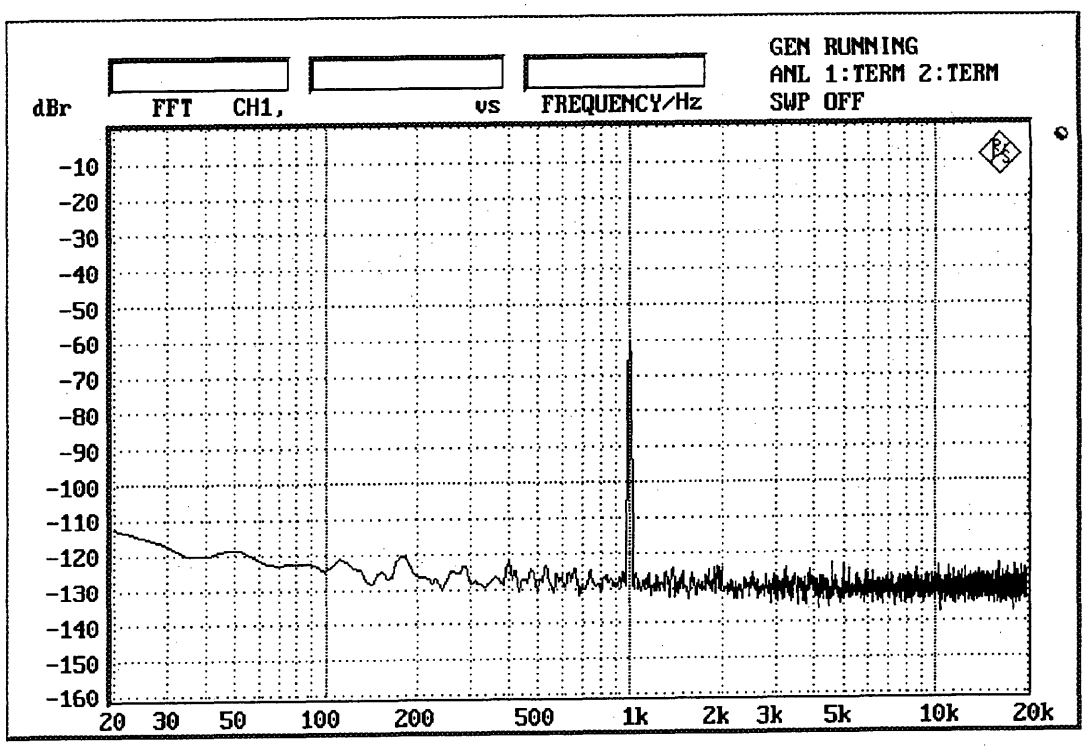


Figure 50 : FFT (input signal : 1kHz, −60dBFS ;
FFT points : 8192, averaging : 10, 30dBFS Notch filter : off)

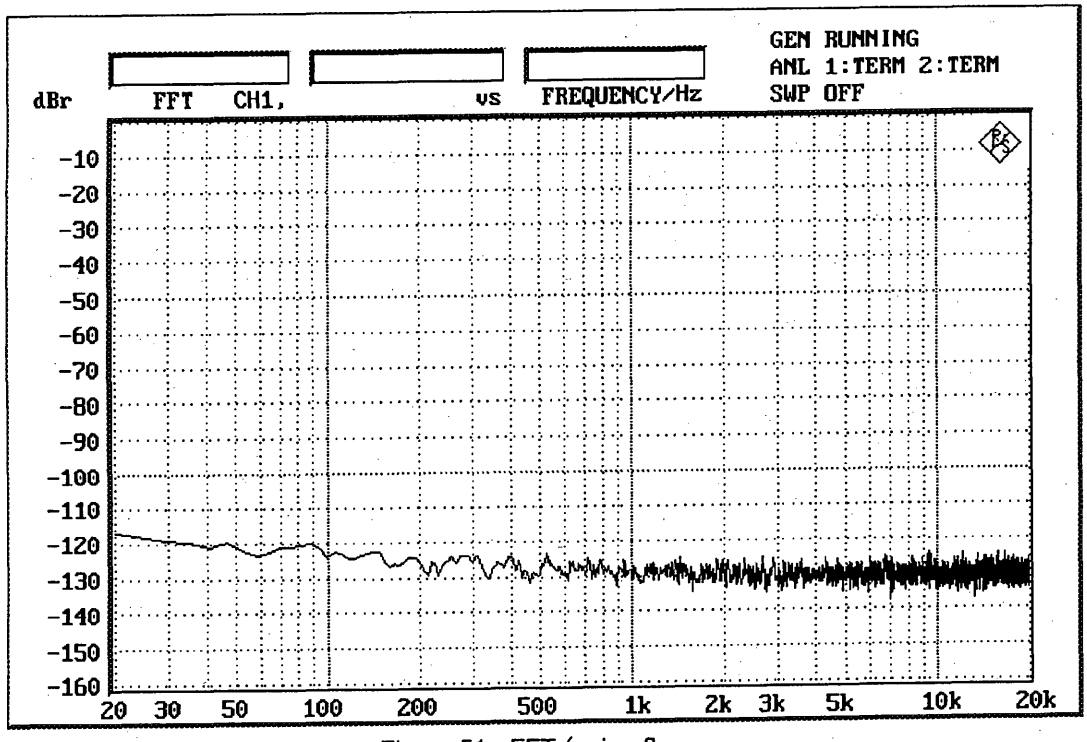


Figure 51 : FFT (noise floor ;
FFT points : 8192, averaging : 10, 30dBFS Notch filter : off)

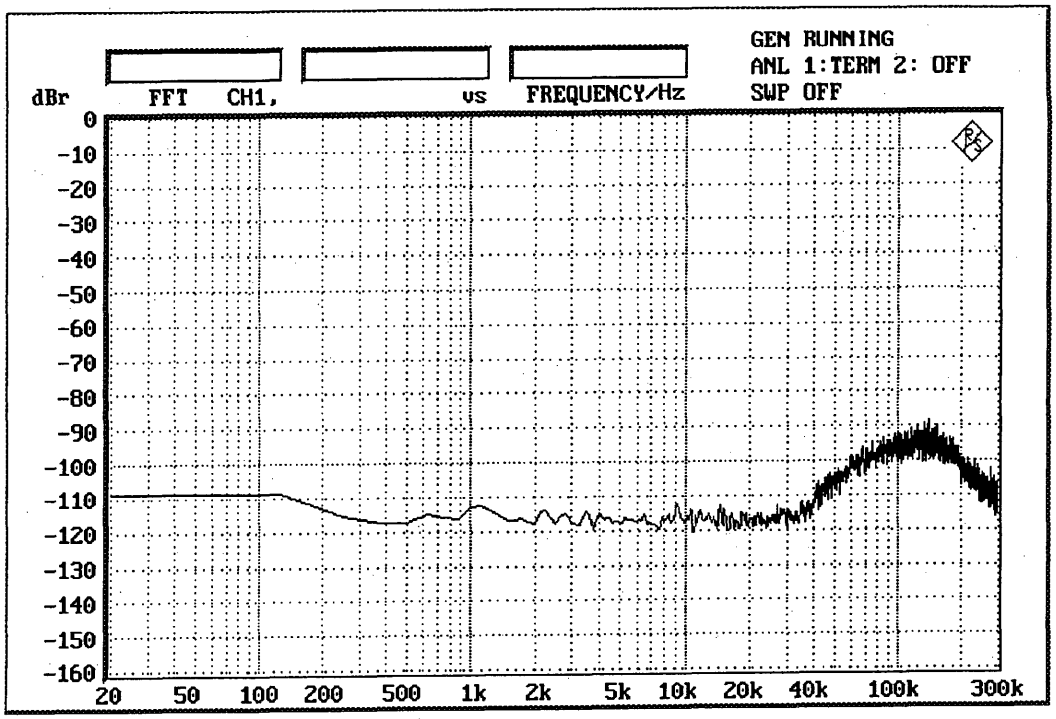
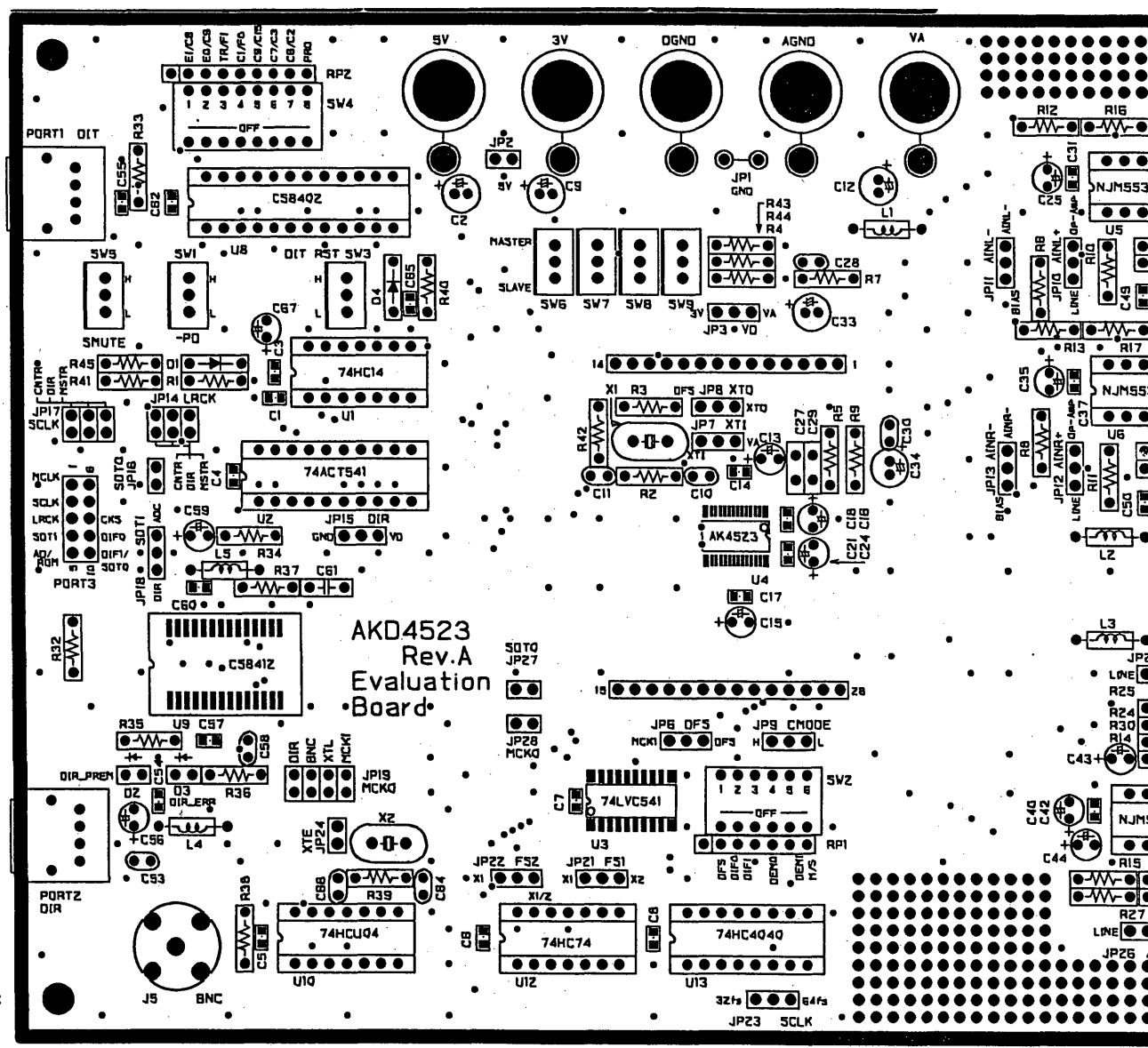


Figure 52 : FFT (out-of-band noise ~300kHz ;
FFT points : 8192, averaging : 10)


AKD4523
Rev.A
Evaluation
Board
5V
3V
DGND
AGND
VA
PORT1 DIT
PORT2 DIR
PORT3
SMUTE
-PD
DIT RST SW3
JP14 LRCK
JP17 SCLK
JP18
JP19 MCKO
JP15 DIR
JP7 XTI
JP8 XTO
JP6 DFS
JP9 CMODE
JP22 FS2
JP21 FS1
JP23 SCLK
JP24 XTE
JP1 GND
JP2
JP3 VD
JP10 AINL+
JP11 AINL-
JP12 AINR+
JP13 AINR-
JP27 SDTO
JP28 MCKO
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
RP1
U1
U2
U3
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U6
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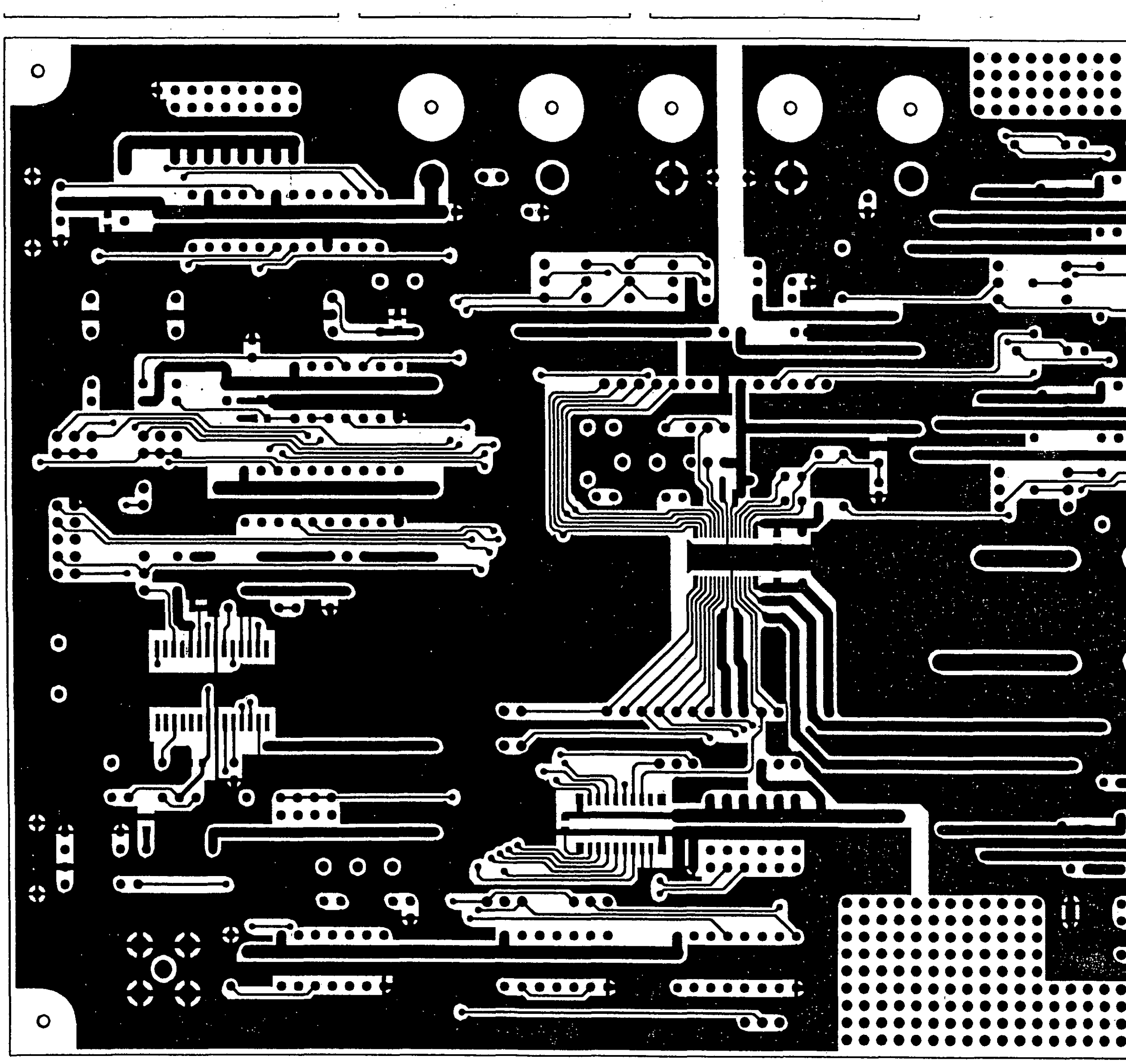
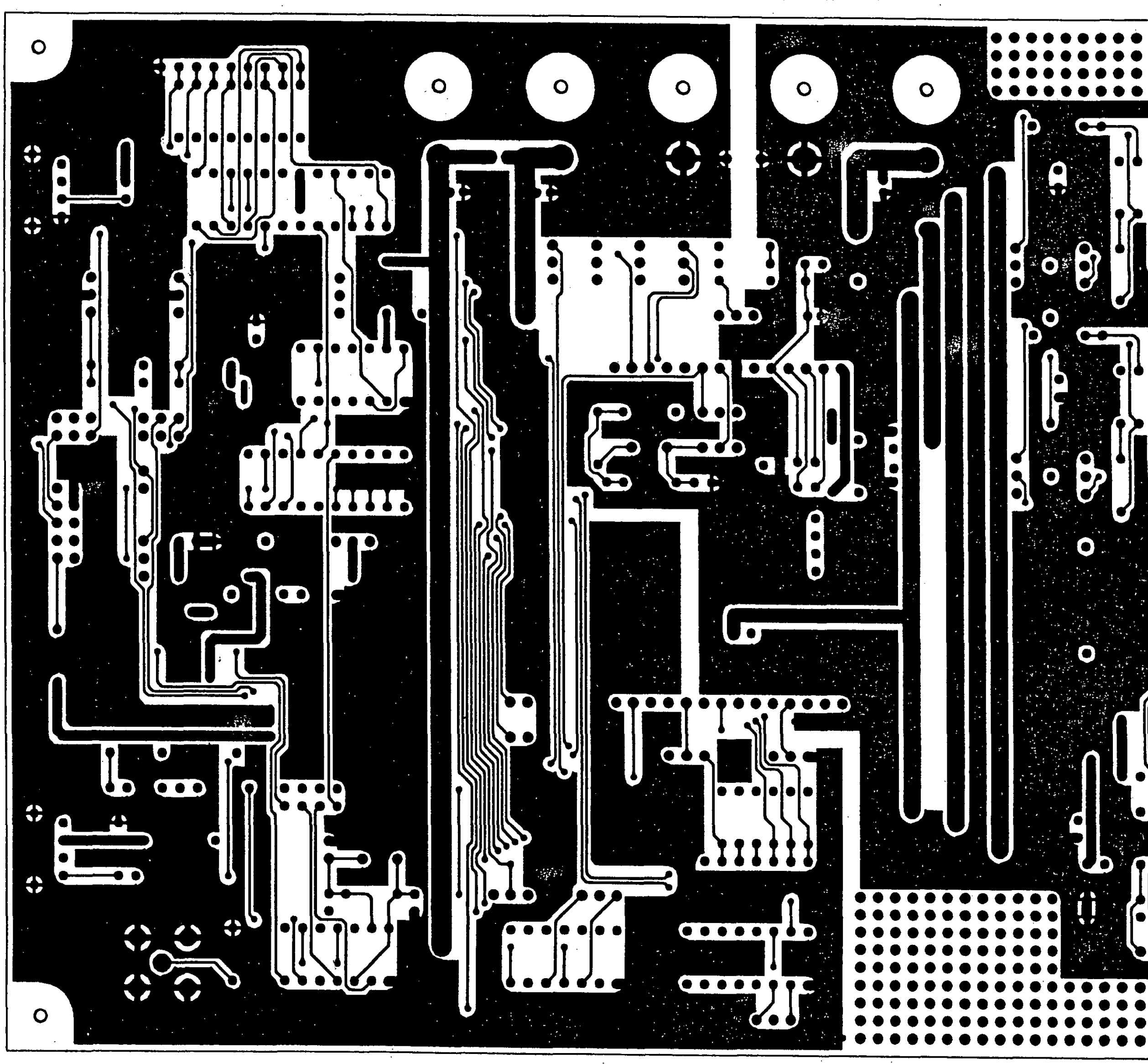
J5 BNC





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