AK8850
NTSC Digital Video Decoder

General Description

The AK8850 decodes NTSC composite video, S-Video and Component Video signals (525/625) into digital formats. Digital output conforms to ITU-R BT.601 and ITU-R BT.656* YCrCb specifications. The AK8850 outputs a control signal to generate clocks synchronized with either Horizontal Sync or Vertical Sync signals. Its clock rate is 27 MHz.

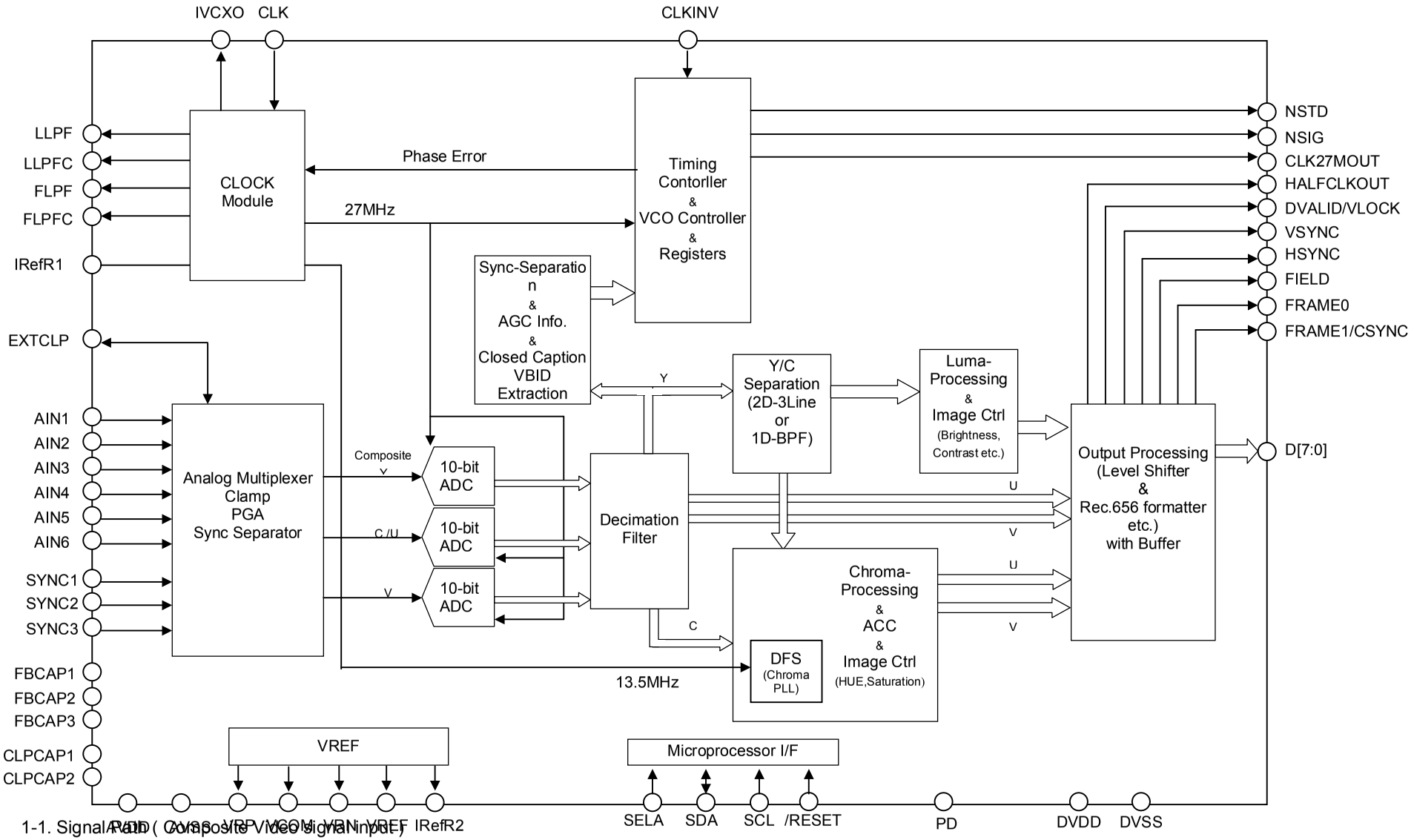
An encoded VBID Closed Caption signal can be extracted from the video signal and sent to an external pin on the AK8850.

Features

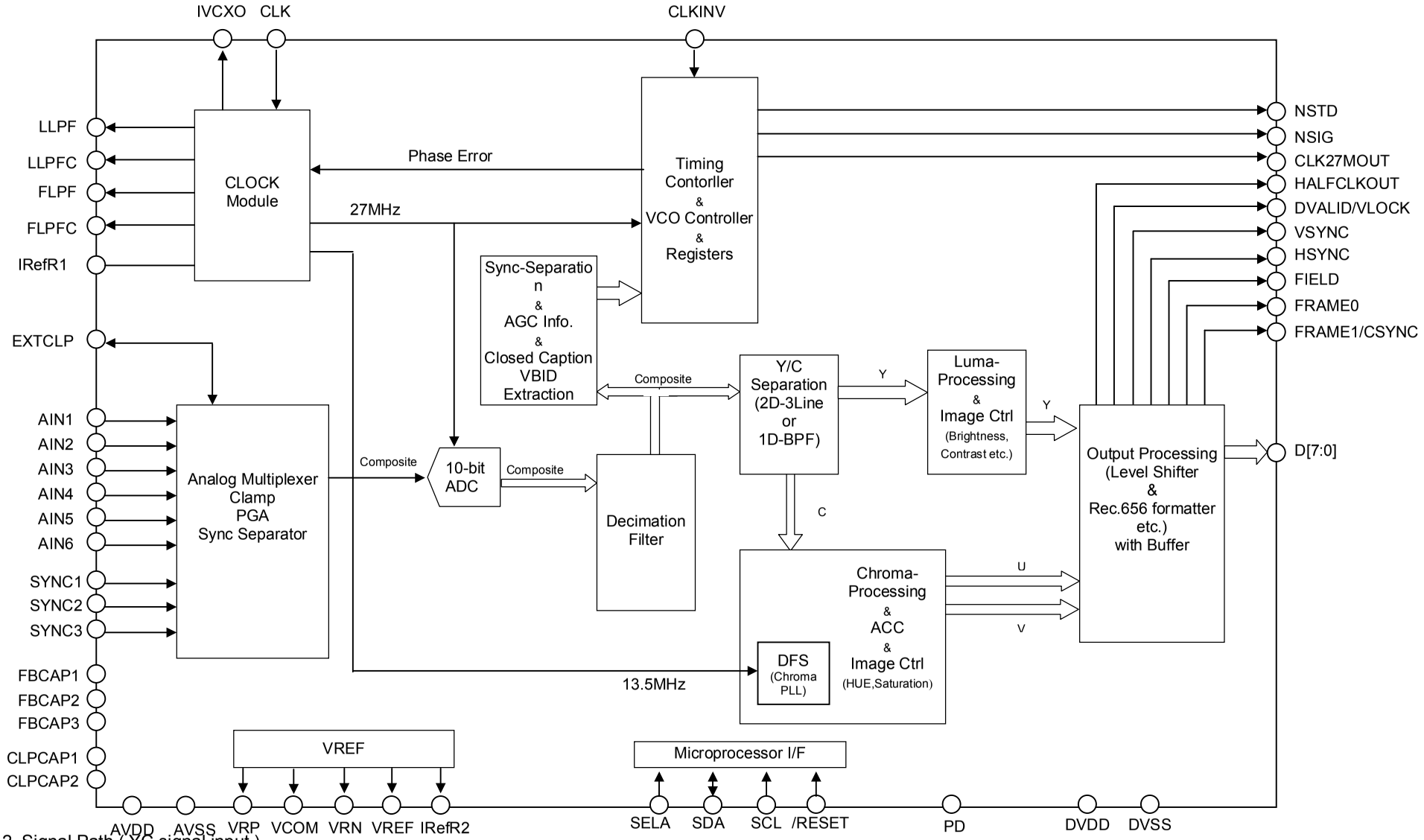
- NTSC-M Composite signal and S-Video signal decoder
- Component Video decoder for 525 / 625 systems (Betacam,MII,EBU N10)
- On-chip triple 10-Bit ADCs (27 MHz operation)
- On-chip Programmable Gain Amp (PGA), ranging from 0 dB to 12 dB in 0.1 dB / steps
- Input-synchronized clock is generated by an external VCXO
- Sub-Carrier generation by Digital Synthesizer (DFS)
- Auto Color Control (ACC)
- Auto Gain Control (AGC)
- Adaptive 3-line Y-C separation
- ITU-R BT.656 format output (4:2:2 8-Bit parallel output with EAV / SAV)
- NTSC Closed Caption signal decoding function
- VBID Program condition decoding function
- WSS Program condition decoding function
- Video Aspect Signal decoding function on Line 16 and Line 279
- Sleep function
- 6–channel Analog inputs
- I2C Control
- 3.3 V CMOS
- 100-Pin LQFP package

note: * ITU-R BT.656 spec may not be satisfied, as it is dependent upon input signal quality.

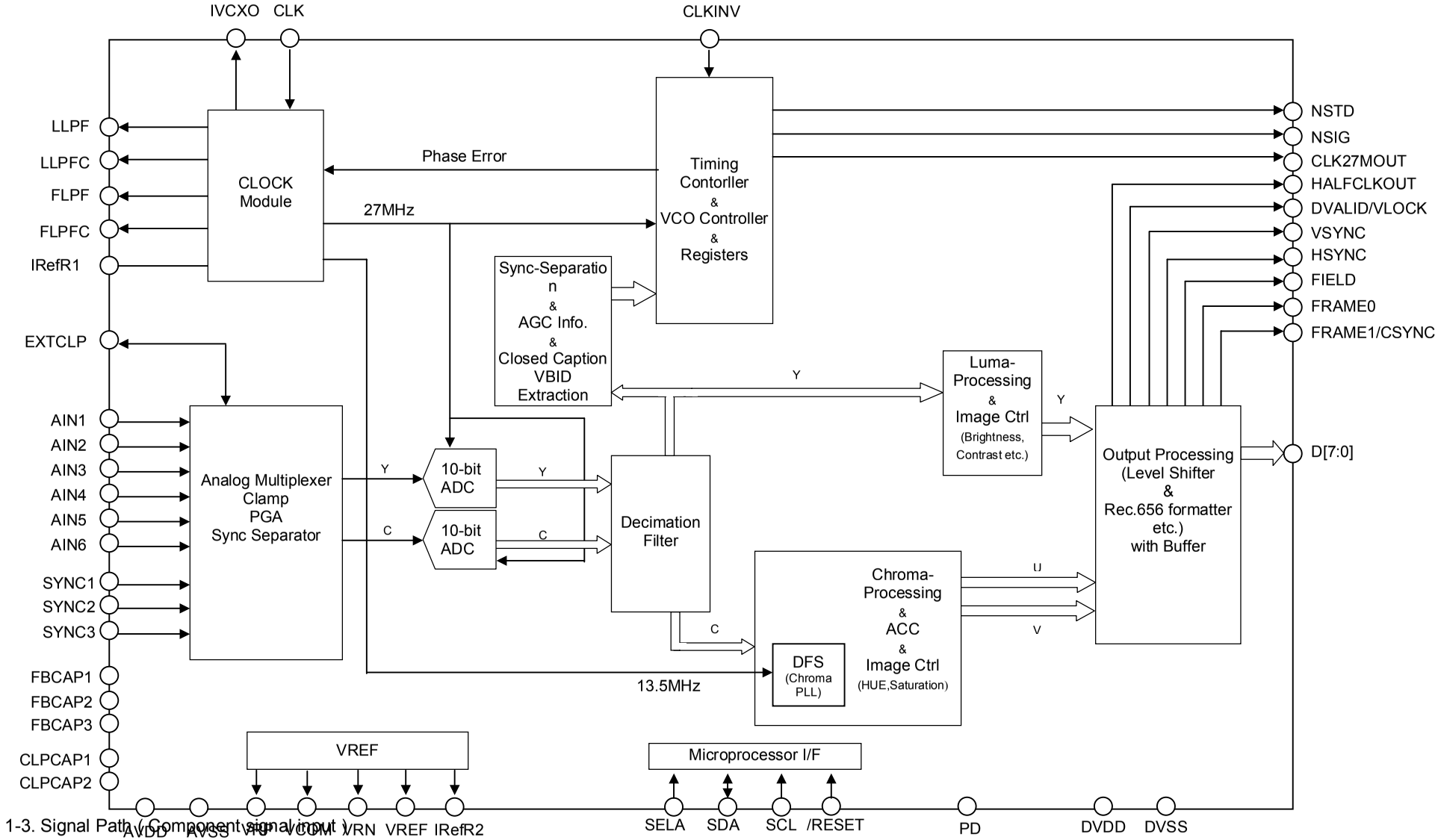
1. Functional Block Diagram



1-1. Signal Path (Composite Video Signal Input)

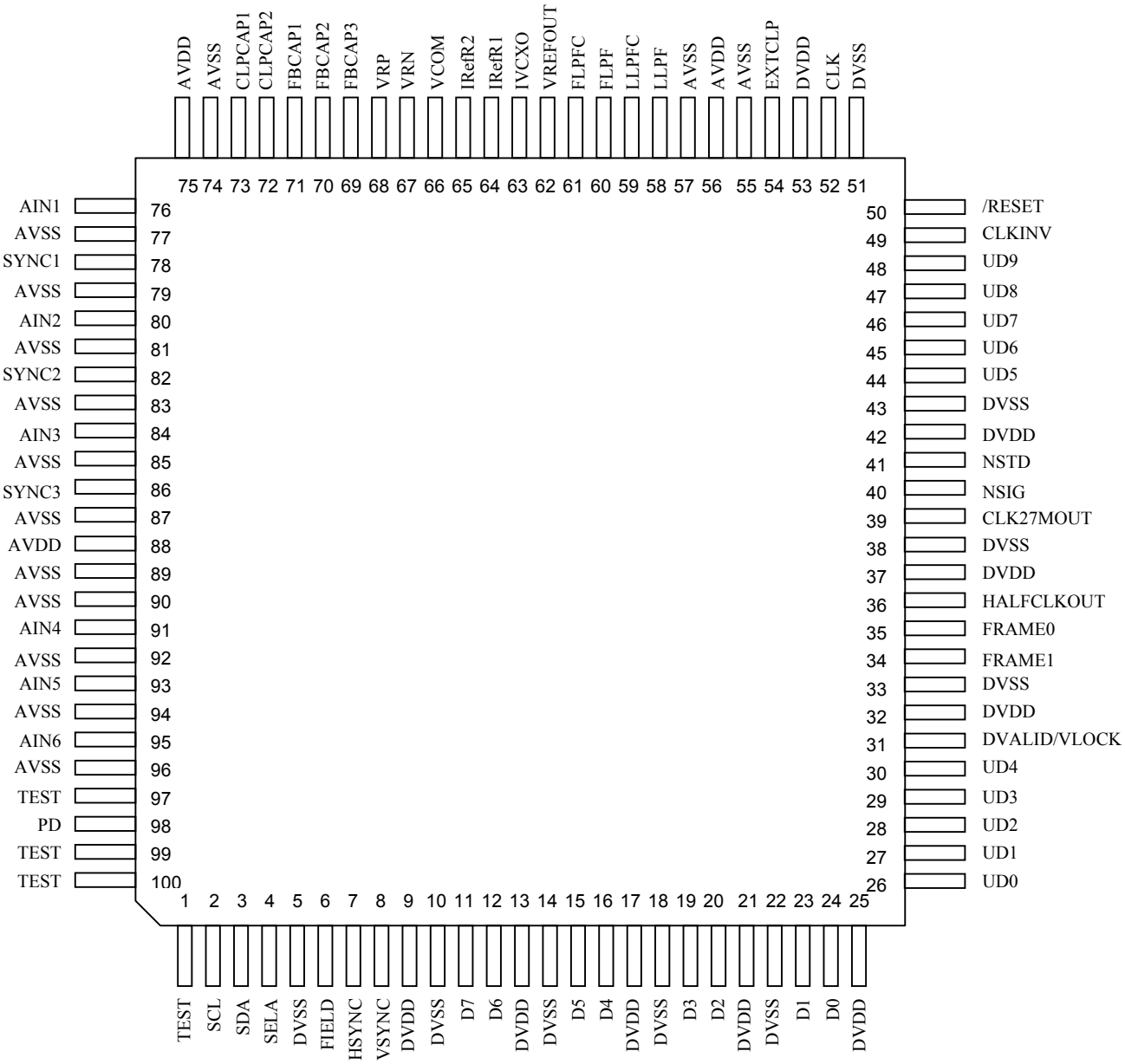


1-2. Signal Path (YC signal input)



1-3. Signal Path (Component signal input)

2. Pin Assignment



3. Pin Functional Description

Pin Number	Identification	I/O	Description
2	SCL	I	I2C bus Clock
3	SDA	I/O	I2C bus Data (Open Collector)
4	SELA	I	I2C bus address selector
6	FIELD	O	FIELD Identify Low□EVEN High□ODD
7	HSYNC	O	HSYNC Timing output pin
8	VSYNC	O	VSYNC Timing output pin. (It is possible to output V_Blank Signal (VD) by setting a register)
11	D7 (MSB)	O	Decoded data output pin (MSB)
12	D6	O	Decoded data output pin
15	D5	O	
16	D4	O	
19	D3	O	
20	D2	O	
23	D1	O	
24	D0 (LSB)	O	Decoded data output pin (LSB)
31	DVALID/VLOCK	O	Active Video Timing signal (720 Pixel) It can also output VLOCK status by setting a register.
34	FRAME1/CSYNC	O	When a standard signal is input, a color frame signal is output. When a non-standard signal input, this pin outputs a timing signal that is toggled every 525/625 lines. FRAME1 pin can output the CYSNC signal by setting a register.
35	FRAME0	O	
36	HALFCLKOUT	O	When Rec.656 data is output, this signal identifies the signal as Y or C. (This rate is about 13.5MHz)
39	CLK27MOUT	O	Output Timing of output data (About 27MHz)
40	NSIG	O	When No-signal is input this pin goes High.
41	NSTD	O	When Non-standard signal is input, this pin goes High.
49	CLKINV	I	This pin decides the polarization of CLK27MOUT.
50	/RESET	I	Reset Signal input pin. (Low Active) After Power up or power down mode, Reset signal should be Low at least 10msec.
52	CLK	I	Input 27MHz Clock.
54	EXTCLP	I/O	External Clamp timing input pin.
58	LLPF	O	Connect Loop Filter for Line Lock clock.
59	LLPFC	O	Connect Capacitors for Line Lock clock.
60	FLPF	O	Connect Loop Filter for Frame Lock clock.
61	FLPFC	O	Connect Capacitors for Frame Lock clock.
62	VREFOUT	O	Internal Voltage Reference output pin. Terminate with 0.1uF or larger capacitor between AVSS.
63	IVCXO	O	Control voltage output pin for the external VCXO. Connect via a resistor to AVSS.
64	IRefR1	O	Terminate with 13kΩ resistor (0.1% accuracy) to AVSS. This Register sets the reference current for the PLL Block.
65	IRefR2	O	Terminate with 4.7kΩ Register (0.1% accuracy) between AVSS. This Register sets the internal reference current.
66	VCOM	O	Internal common voltage for ADC output pin. Terminate with 0.1uF or larger capacitor between AVSS.
67	VRN	O	Internal negative voltage for ADC output pin. Terminate with 0.1uF or larger capacitor between AVSS.
68	VRP	O	Internal positive voltage for ADC output pin. Terminate with 0.1uF or larger capacitor between AVSS.
69	FBCAP3	O	Terminate using a 0.033uF capacitor between AVSS. (for Clamp Level)

70	FBCAP2	O	Terminate 0.033uF capacitor between AVSS. (for Clamp Level)
71	FBCAP1	O	Terminate 0.033uF capacitor between AVSS. (for Clamp Level)
72	CLPCAP2	O	Terminate 0.1uF capacitor between AVSS. (for Clamp)
73	CLPCAP1	O	Terminate 0.1uF capacitor between AVSS. (for Clamp)
76	AIN1	I	Analog video signal input pin. The signal should be input through a 0.1uF capacitor with -6dB Gain.
80	AIN2	I	
84	AIN3	I	
91	AIN4	I	
93	AIN5	I	
95	AIN6	I	
78	SYNC1	I	Analog video signal input pin for the internal clamp pulse generator. This signal should be input through a 0.1uF capacitor with 0dB Gain.
82	SYNC2	I	
86	SYNC3	I	
98	PD	I	Power Down Control Pin. When this pin becomes High, the AK8850 enters a power down state. When returning from power down mode, AK8850 requires reset sequence.
56,75,88	AVDD	P	Analog power supply (3.3V) pin.
55,57,74, 77,79,81, 83,85,87, 89,90,92, 94,96,96	AVSS	G	Analog Ground pin.
9,13,17, 21,25,32, 37,42,53	DVDD	P	Digital power supply (3.3V) pin.
5,10,14, 18, 2,33, 38,43,51	DVSS	G	Digital Ground pin.
26,27,28, 29,30,44, 45,46,47, 48	UD[9:0]	I/O	These pins are for test purpose. These pins should be NC.
1,44,45, 46,47,48, 97,99, 100	TEST	I	These pins are for test purpose. Connect to the DVSS.

4. Electrical Specifications

4-1. Absolute Maximum Ratings

Item	Min.	Max	Unit
Supply Voltage□VDD□ DVDD, AVDD	□0.3	4.5	V
Input Pin Voltage (Vin)	□0.3	VDD + 0.3	V
Input Pin Current (Iin)	□10	10	mA
Storage Temperature	□40	125	□

note) each ground pin (DVSS,AVSS) is equal to 0 V (voltage reference).

4-2. Recommended Operating Conditions

Item	Min.	Typ.	Max.	Unit
Supply Voltage	3.0	3.3	3.6	V
AVDD DVDD	3.0	3.3	3.6	V
Operating Temperature	□10		85**	□

note) * each ground pin (DVSS,AVSS) is equal to 0 V (voltage reference).

** Assumes mounting on a 4-layer PCB□>100mm x 100mm x 1.6mm□with wiring density greater than 60%.

4-3DC Characteristics (DVDD=AVDD=3.0 ~ 3.6 V at room temperature)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital Input High Voltage	VIH	0.7VDD			V	
Digital Input Low Voltage	VIL			0.3VDD	V	
Digital Input Leak Current	IIL			±10	uA	
Digital Output High Voltage	VOH	2.4			V	IOH = □400uA
Digital Output High Voltage	VOL			0.4	V	IOL = 1.2mA
I^2C Input High Voltage I^2C (SDA, SCL)	VIHC	0.7VDD			V	
I^2C Input Low Voltage I^2C (SDA, SCL)	VILC			0.3VDD	V	
I^2C (SDA) L □□	VOLC			0.4	V	IOLC = 3mA

4-4. AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital Maximum Load Capacitance		15		40	pF	

4-5. Analog Characteristics and Power Dissipation

Selector and Clamp (AVDD=3.3V, Room Temperature)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Maximum Input Range (AIN1□AIN6)	VIMX	1.20	1.28		V_{PP}	PGA Gain 0dB
Composite, Luminance Signal Clamp Level	VYCP		0.70		V	
C/U/V Signal Clamp Level	VCCP		1.34		V	
Clamp Current	CLPI		±70		uA	
Isolation between ADC			-60		dB	5.5MHz

PGA (AVDD=3.3V, Room Temperature)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Min.Gain	GMN		0		dB	
Max Gain	GMX		12		dB	
Gain Step	GST		0.094		dB	
Relative Gain accuracy	ERP		±1		LSB	

ADC (AVDD=3.3V, Room Temperature)

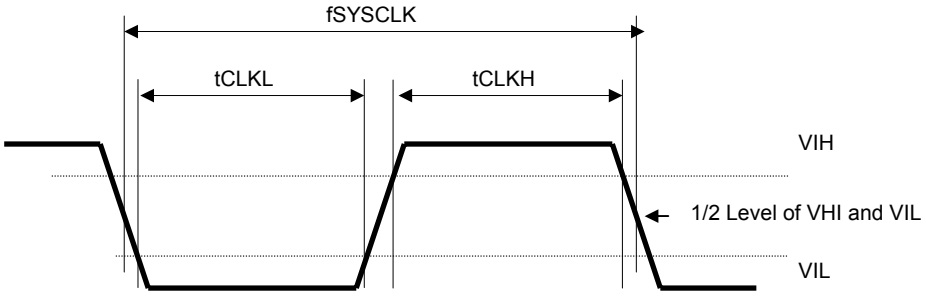
Item	Symbol	Min.	Typ.	Max	Unit	Condition
Resolution	RES			10	bits	
Operating Clock Frequency	FS		27		MHz	
Integral Non Linearity	INL		±2.0	±4.0	LSB	fs=27MHz
Differential Non Linearity	DNL		±0.8	±2.0	LSB	fs=27MHz
S/N	SN		54		dB	fin=1MHz Ain=□1dB fs=27MHz
S/(N+D)	SND		51		dB	fin=1MHz Ain=□1dB fs=27MHz

Power Consumption (DVDD=AVDD=3.3V, Room Temperature)

Item	Symbol	Min.	Typ.	Max	Unit	Condition
Compensation Current (Active)			216	280	mA	
Digital + Analog			71		mA	3ch operating
Analog			145		mA	25pFLoad, Color bar input
Digital						
Power Down Current						Mode 1: Set by Register
Mode 1						
Digital + Analog			58	75	mA	Mode 2: Set by PD pin
Analog			22		mA	
Digital			36		mA	*It requires several second from Mode 2 power down mode to Active mode.
Mode 2			0.01	0.2	mA	
Digital + Analog			0.01		mA	
Analog			0.01		mA	
Digital						

4-6. AC Timing (DVDD=3.0 ~ 3.6 V at 25 deg. C)

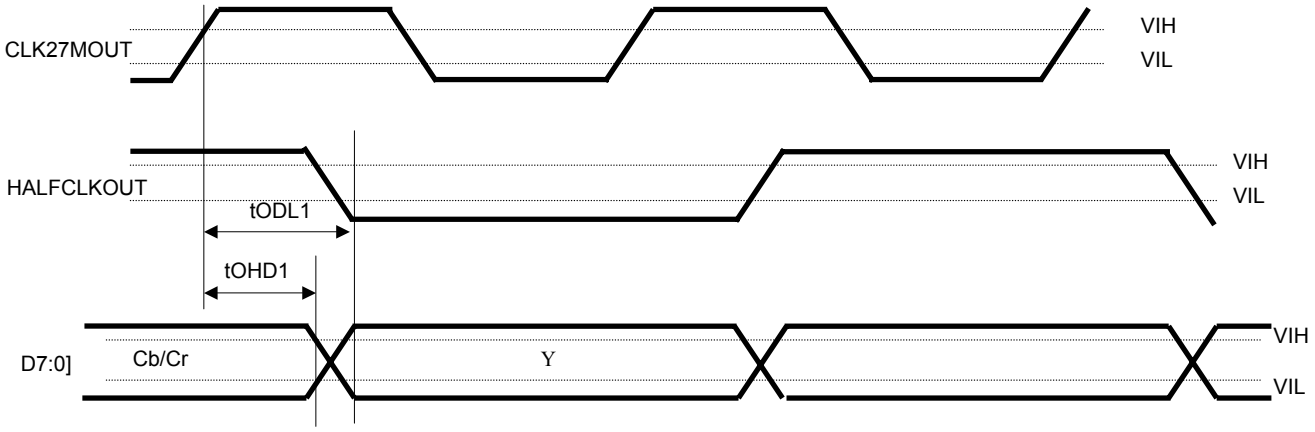
4-6-1 Clock Input



item	Symbol	Min.	Typ.	Max	Unit
CLK	fSYSCLK		27		MHz
CLK pulse width (High)	tCLKH	15			nsec
CLK pulse width (Low)	tCLKL	15			nsec
Stability of Clock				±100	ppm

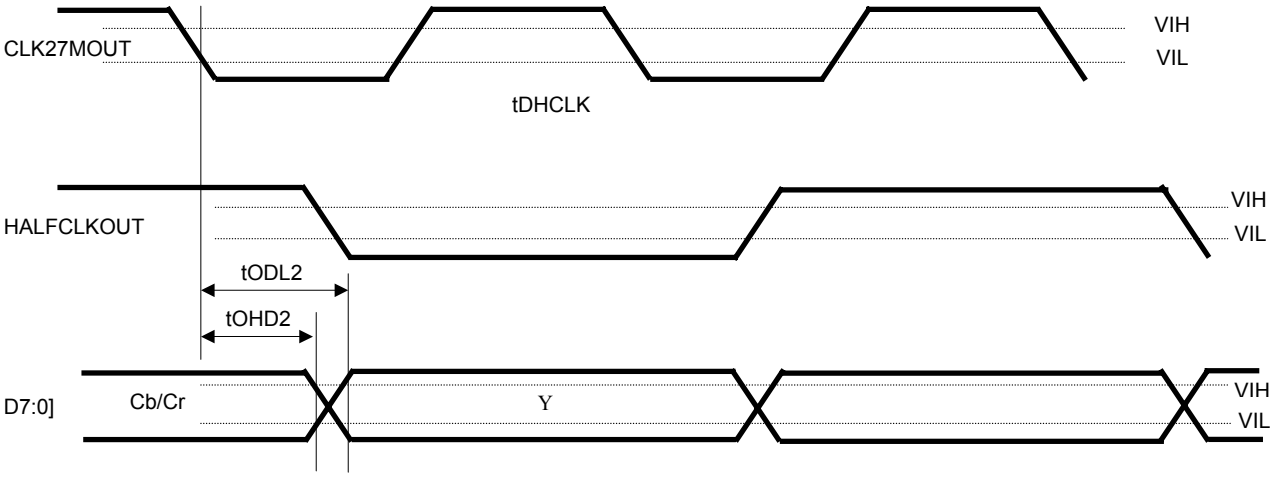
4-6-2 Output Data Timing (D7 ~ D0)

4-6-2-1 CLKINVpin = L



Item	Symbol	Min.	Typ.	Max.	Unit	Note
Output Data Delay Time	tODL1			25.0	nsec	CL 25pF
Output Data Hold Time	tOHD1	3.0			nsec	

4-6-2-2 CLKINVpin = H

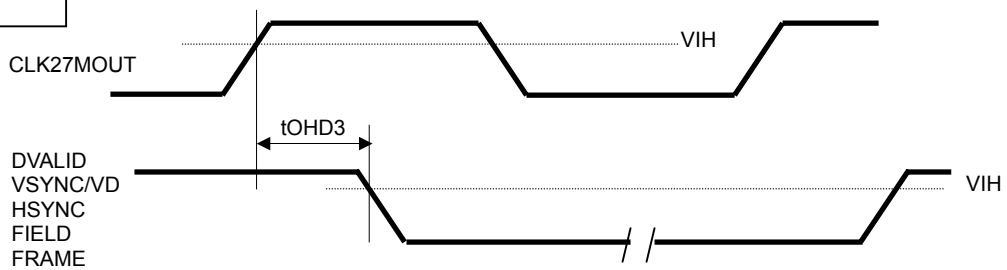


Item	Symbol	Min.	Typ.	Max.	Unit	Note
Output Data Delay Time	tODL2			25.0	nsec	CL 25pF
Output Data Hold Time	tOHD2	3.0			nsec	

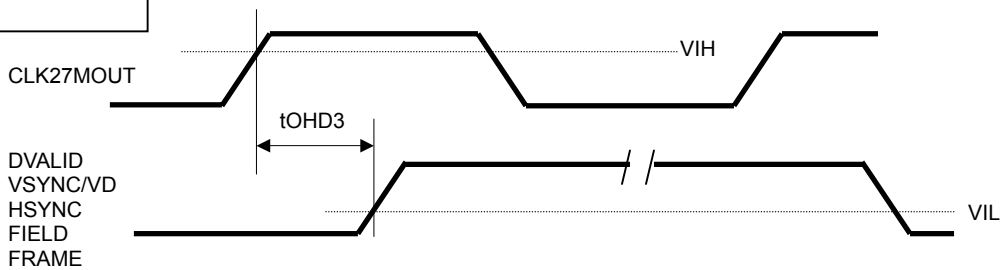
4-6-3 Output Data Timing (DVALID/VSYNC/HSYNC/FIELD/FRAME0/FRAME1)

4-6-3-1 CLKINVpin = L

Output Control Register
DVALID=L
VSYNC=L
HSYNC =L
FIELD=L
FRAME=L



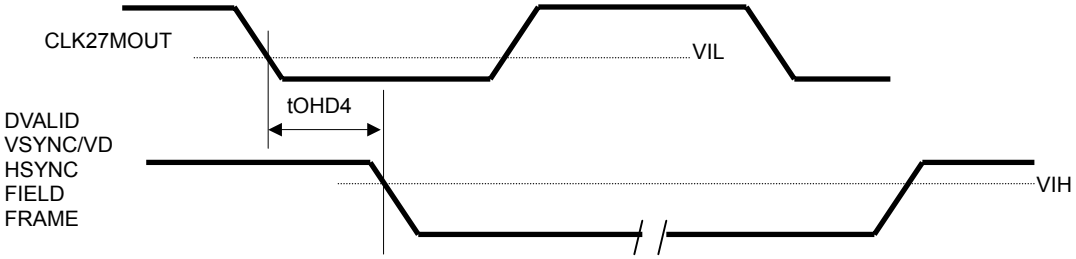
Output Control Register
DVALID=H
VSYNC=H
HSYNC =H
FIELD=H
FRAME=H



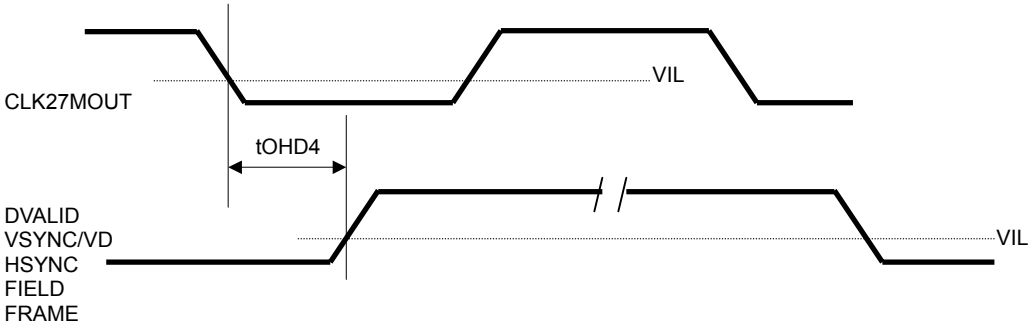
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Output Data Hold Time	tOHD3	3.0			nsec	CL 25pF

4-6-3-2 CLKINVpin = H

Output Control Register
DVALID=L
VSYNC=L
HSYNC =L
FIELD=L
FRAME=L



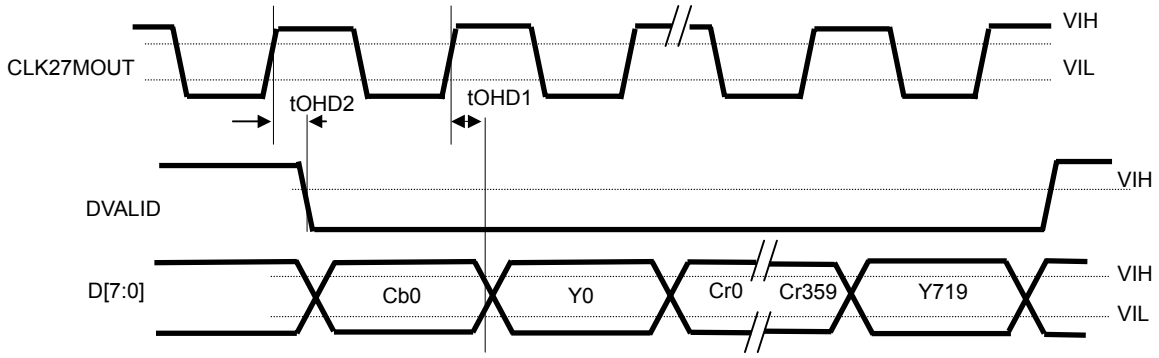
Output Control Register
DVALID=H
VSYNC=H
HSYNC =H
FIELD=H
FRAME=H



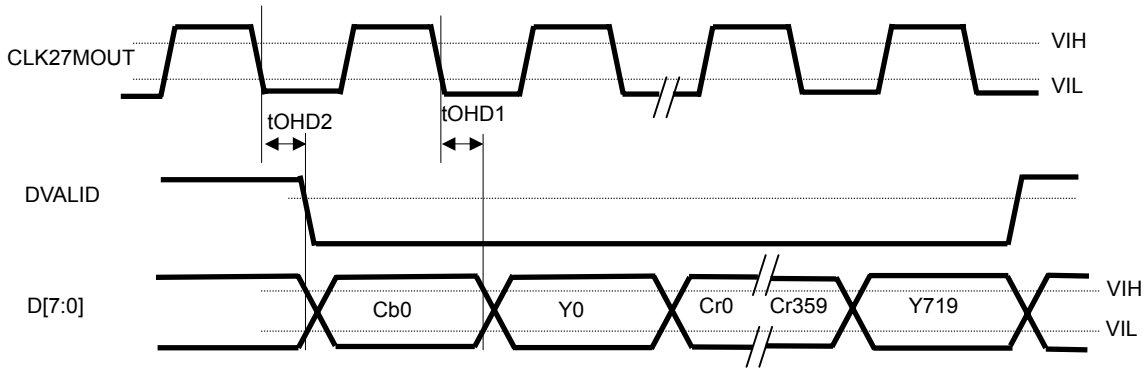
Item	Symbol	Min.	Typ.	Max	Unit	Note
Output Data Hold Time	tOHD4	3.0			nsec	CL 25pF

4-6-4 Output Data Timing (CLK27MOUT, DVALID signal, D7~D0 relation)

4-6-4-1 CLKINVpin L and Output Control Register DVALID-bit=L

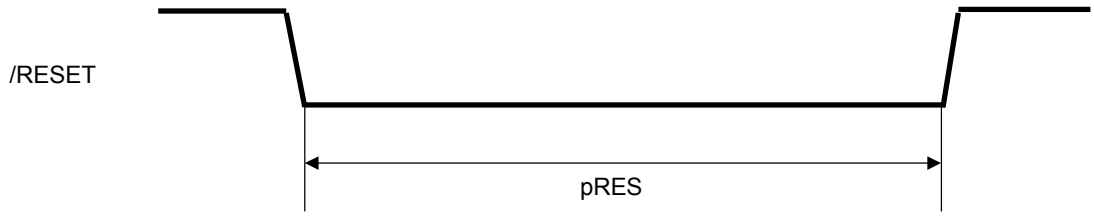


4-6-4-3 CLKINV pin H and Output Control Register DVALID-bit=L



4-6-5 Reset Timing (initialization)

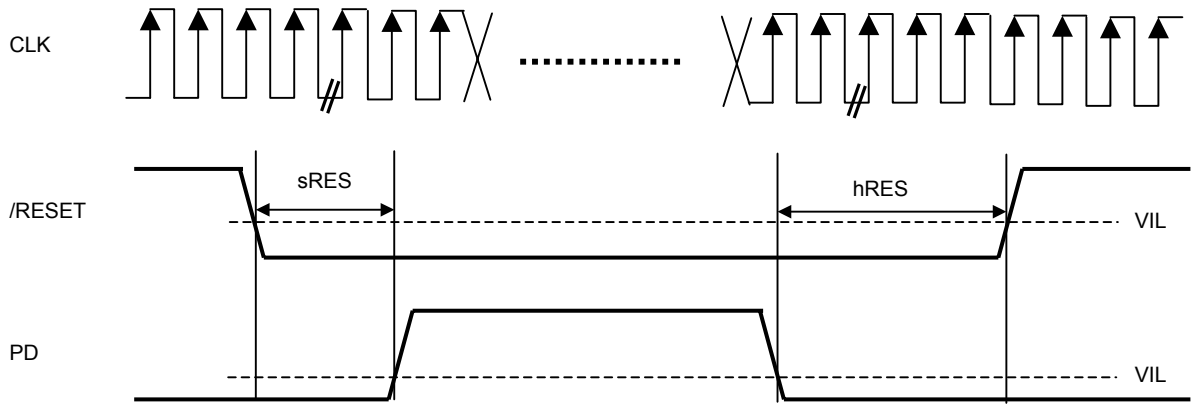
Reset Signal (Reset Signal should be held Low state for 10msec or longer)



Item	Symbol	Min.	Typ.	Max.	Unit	Note
/RESET Pulse width	pRES	10			msec	

Note System Control Pins (SELA, CLKINV, PD etc.) remain in their states for at least 10 clock cycles before/after a reset signal input.

4-6-6 Power-Down / Up Sequence

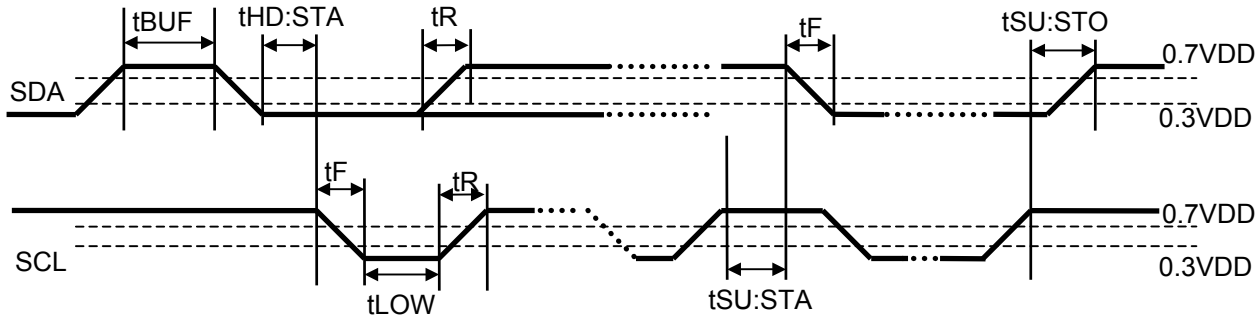


Item	Symbol	Min.	Typ.	Max.	Unit	Note
RESET pulse width (Setting PD mode)	sRES	100			CLK	from CLK Rising edge
RESE pulse width (Returning from PD mode)	hRES	10			msec	

Note) After PD pin becomes High (power down state), /RESETpin status is irrelevant.

4-6-7 I2C bus Input & Output Timing (SCL 400KHz cycle mode)

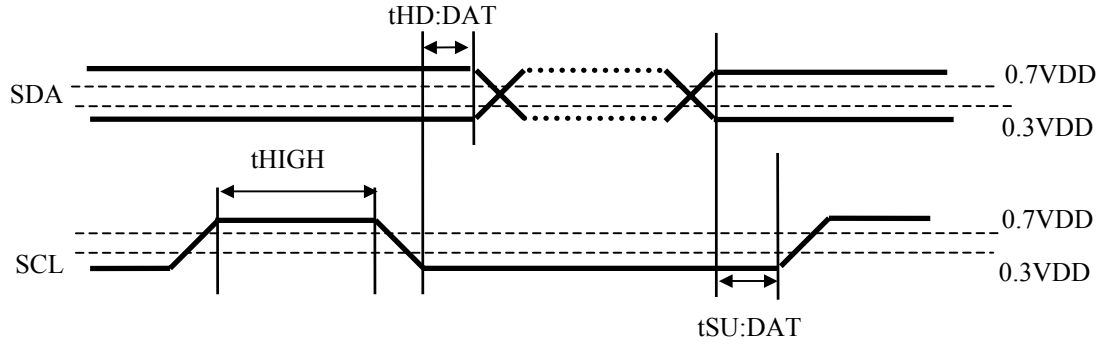
(1) Timing 1



Item	Symbol	Min.	Max.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

All the figures shown above are not defined by the AK8850 but are defined by I^2C Bus standard.
Please see the I^2C Bus standard for further details

(2) Timing 2



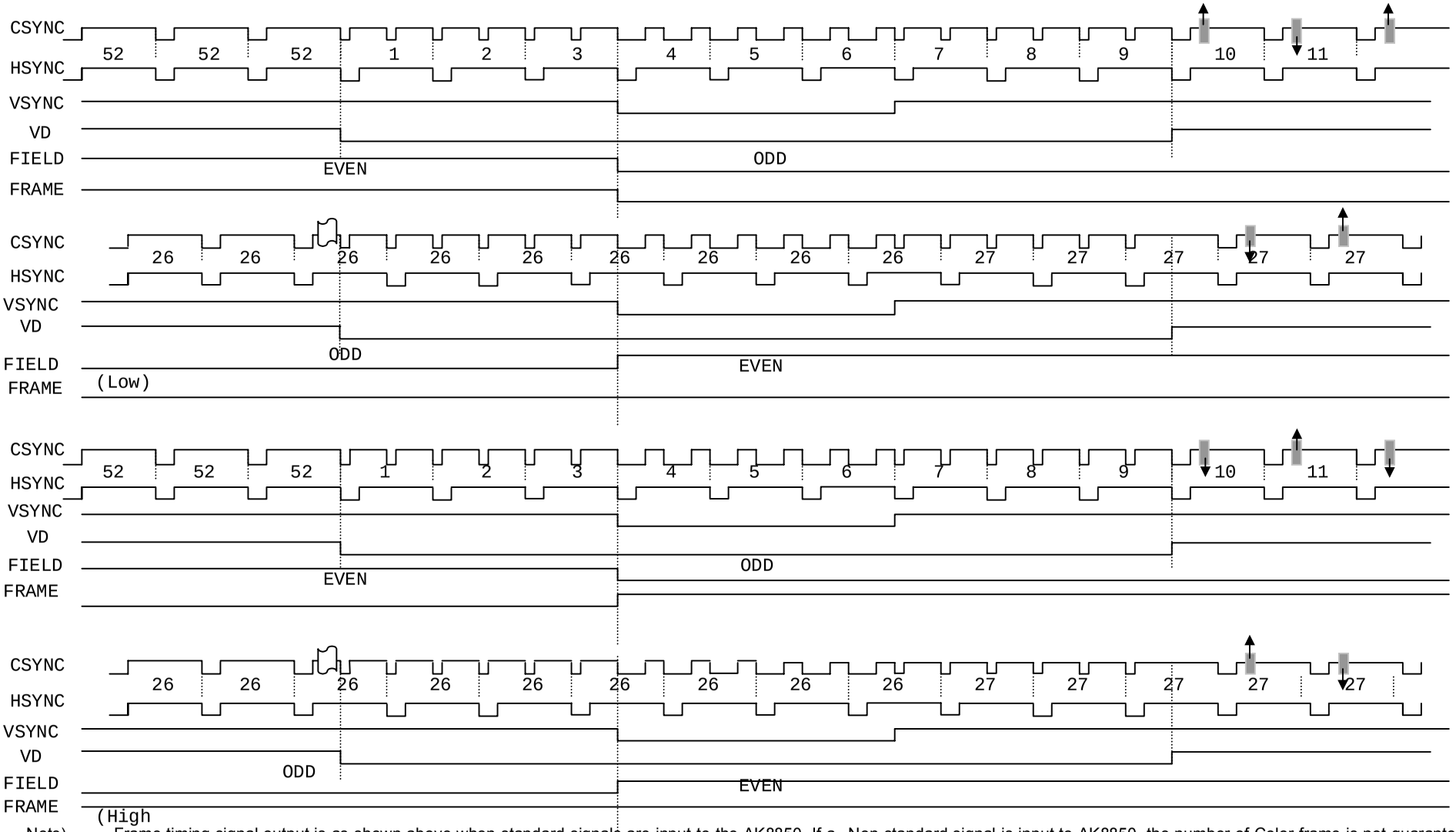
Item	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100(1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9(2□	usec
Clock Pulse High Time	tHIGH	0.6		usec

(1) In case of normal I^2C bus mode tSU:DAT ≥250nsec
(2) Using under minimum tLOW, this value must be satisfied.

5. Output Signal Timing Description

5-1. NTSC Input

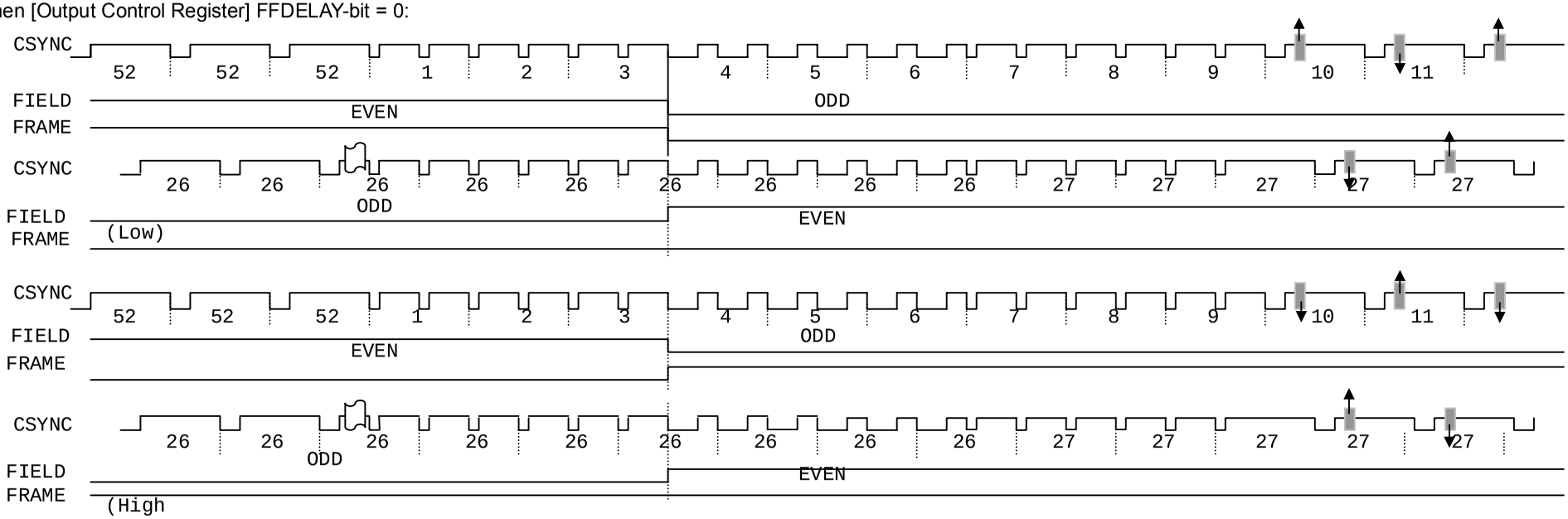
Vertical Sync timing, Field signal and Frame signal timing relations are shown below. The logic states of HSYNC/VSYNC/FIELD/FRAME can be altered via register settings. Depending on the register setting either VSYNC or VD signal is available. FIELD output and FRAME output signals change states on the rising edge of CSYNC just before the 0.5H delay period that is controlled by the Output Control Register. The 0.5H delay timing is shown on page 18.



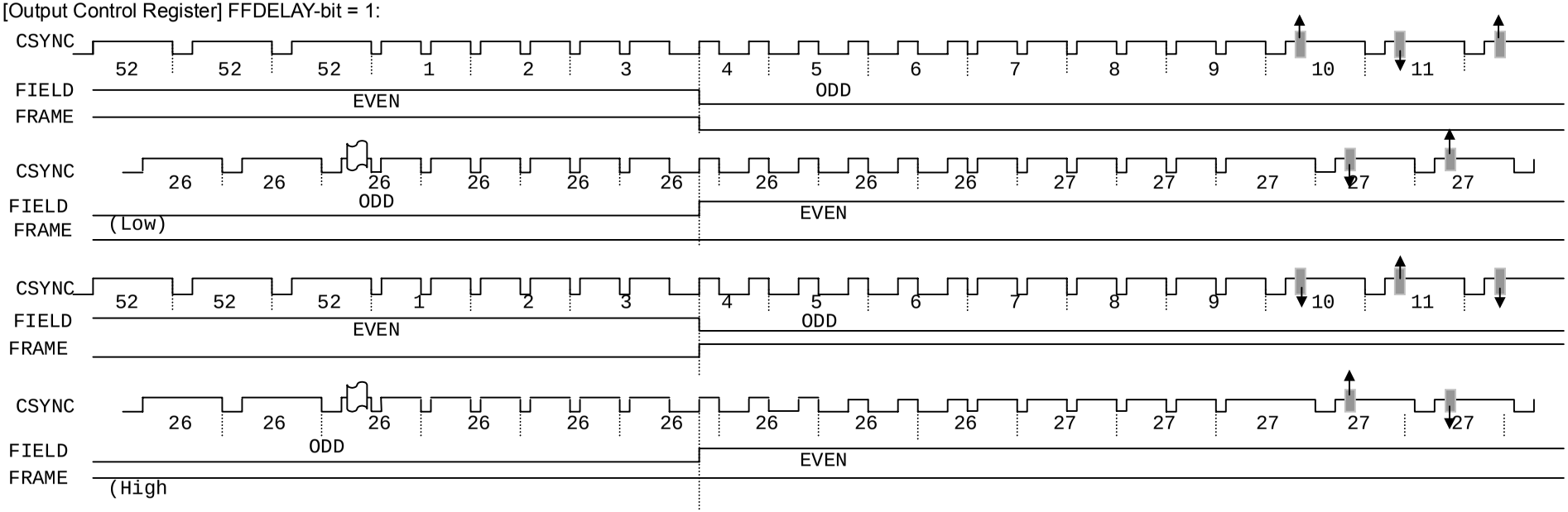
Note) Frame timing signal output is as shown above when standard signals are input to the AK8850. If a Non-standard signal is input to AK8850, the number of Color frame is not guaranteed. When the input signal changes from non-standard to standard, that the Frame timing signal may not change for 512 lines (max) as the AK8850 synchronizes to the input video signal.

5-2. FIELD/FRAME Signal Output Timing Diagram with NTSC signal input (CSYNC & FIELD/FRAME0/FRAME1 relationship)

when [Output Control Register] FFDELAY-bit = 0:

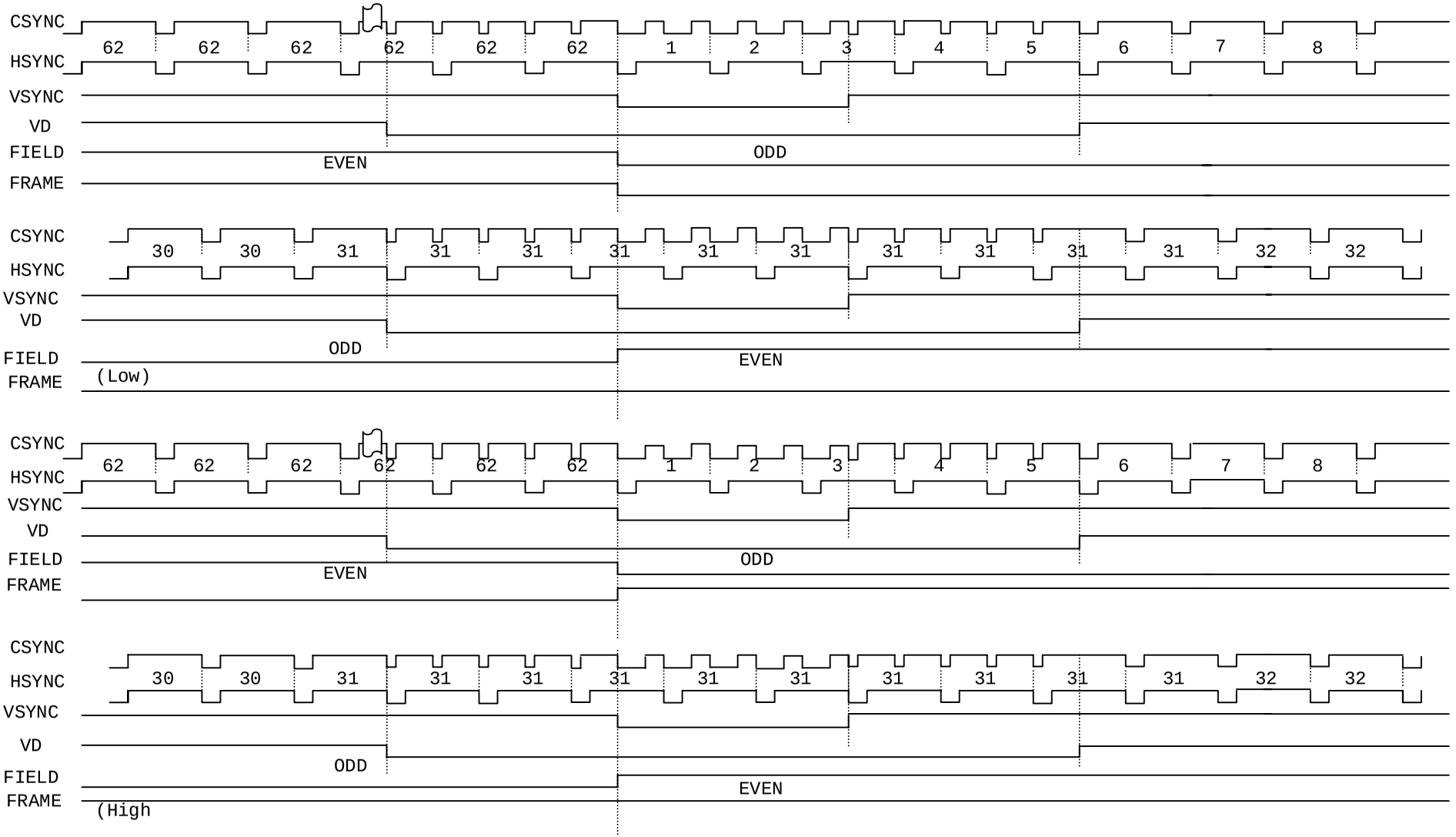


at [Output Control Register] FFDELAY-bit = 1:

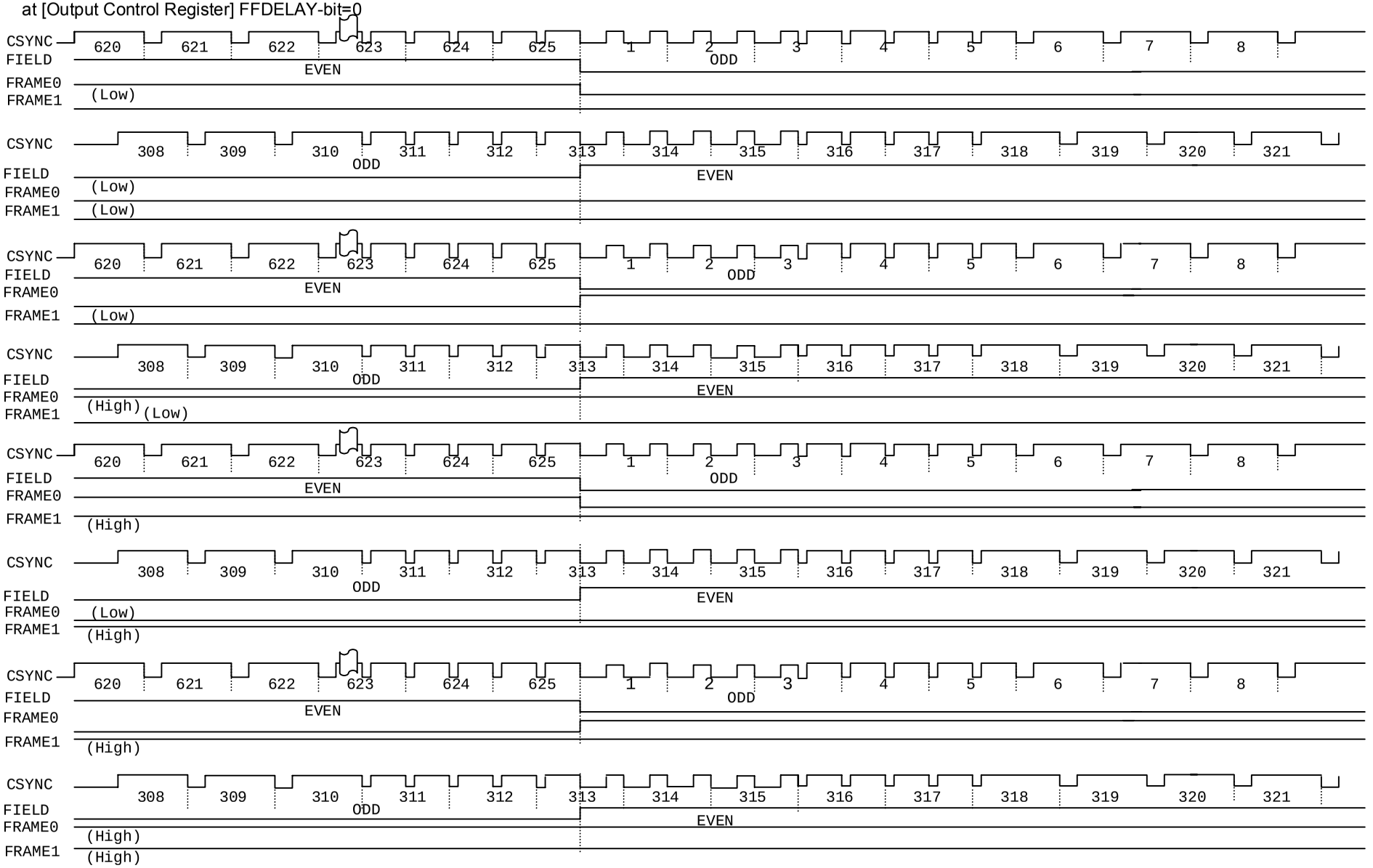


5-3. Output Signal Timing Diagram (CCIR625 Component input)

The VERTICAL Sync signal, FIELD signal and FRAME signal timing relationships are shown. The logical state of HSYNC/VSYNC/FIELD/FRAME can be altered by using register settings. Either VSYNC or VD output signals are available on the VSYNC output pin, depending upon the register setting. The FIELD output and the FRAME output signals change state on the rising edge of the CSYNC, prior to the 0.5H delay period that is controlled by the output control register. Field/FRAME output timings are shown on pages 20 and 21.

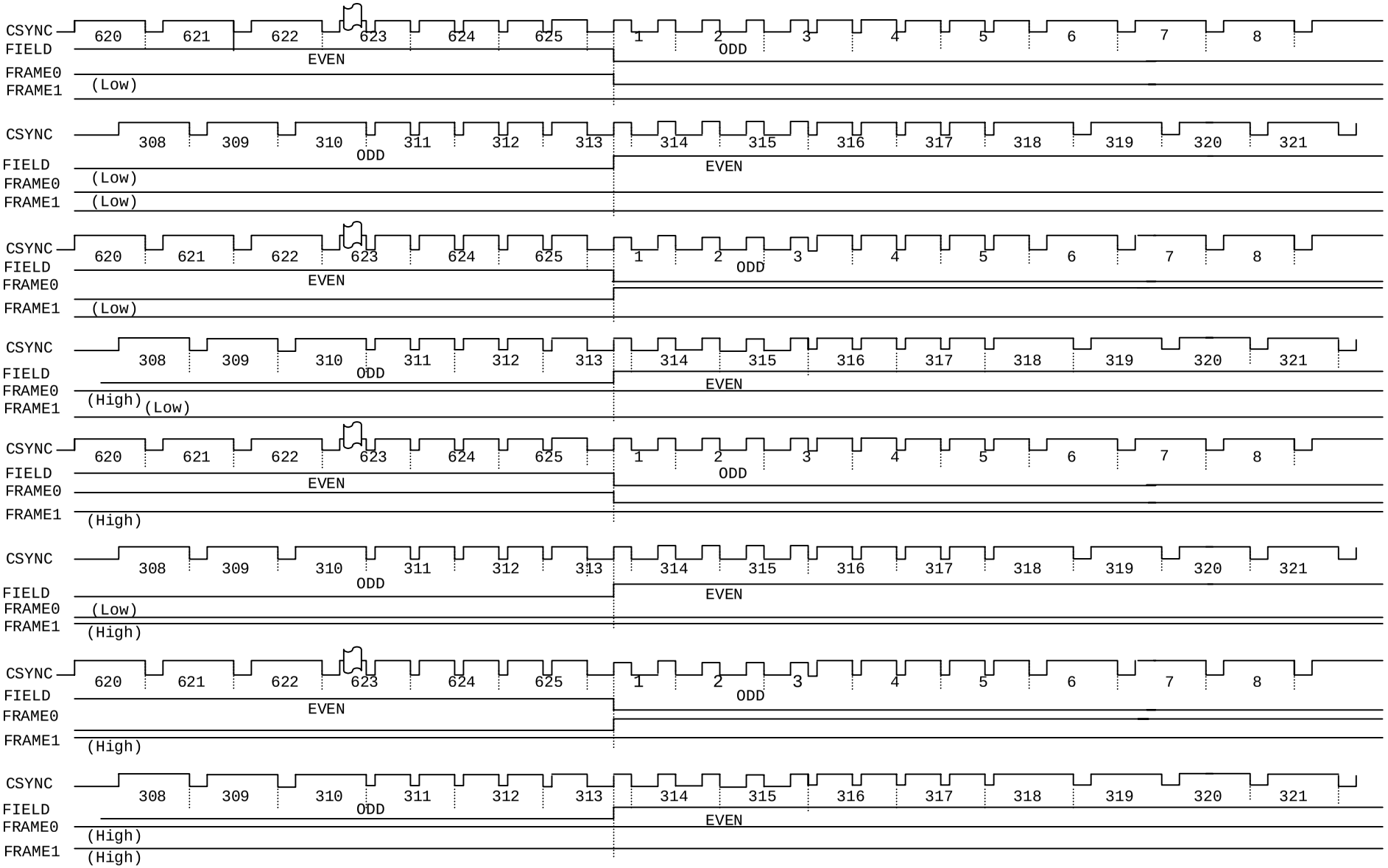


625 Component Signal Output Timing Diagram (CSYNC & FIELD/FRAME0/FRAME1 relationship)
at [Output Control Register] FFDELAY-bit=0



5-5 625 Component Signal Output Timing Diagram (CSYNC & FIELD/FRAME0/FRAME1 relationship)

when [Output Control Register] FFDELAY-bit =1


CSYNC
FIELD
FRAME0
FRAME1
620 621 622 623 624 625 1 2 3 4 5 6 7 8
EVEN
ODD
(Low)
CSYNC
FIELD
FRAME0
FRAME1
308 309 310 311 312 313 314 315 316 317 318 319 320 321
ODD
EVEN
(Low)
(Low)
CSYNC
FIELD
FRAME0
FRAME1
620 621 622 623 624 625 1 2 3 4 5 6 7 8
EVEN
ODD
(Low)
CSYNC
FIELD
FRAME0
FRAME1
308 309 310 311 312 313 314 315 316 317 318 319 320 321
ODD
EVEN
(High)
(Low)
CSYNC
FIELD
FRAME0
FRAME1
620 621 622 623 624 625 1 2 3 4 5 6 7 8
EVEN
ODD
(High)
CSYNC
FIELD
FRAME0
FRAME1
308 309 310 311 312 313 314 315 316 317 318 319 320 321
ODD
EVEN
(Low)
(High)
CSYNC
FIELD
FRAME0
FRAME1
620 621 622 623 624 625 1 2 3 4 5 6 7 8
EVEN
ODD
(High)
CSYNC
FIELD
FRAME0
FRAME1
308 309 310 311 312 313 314 315 316 317 318 319 320 321
ODD
EVEN
(High)
(High)

6. Functional Summary
6-1. Clock

1. Line Locked Clock mode:
An operating mode where the device operates using a clock synchronized with the Horizontal Sync signal for each line.

2. Frame Locked Clock mode:
The device operates using a clock synchronized with the Vertical Sync signal at each Frame.

3. Fixed Clock mode:
An external clock is used.

These clock modes are set with the Control 2 register. Since both the Line Locked and Frame Locked modes use an input-signal synchronized clock, ITU-R BT.656* compatible output is available, although input signal quality may prevent full ITU-R BT.656 compatibility.

6-2. Analog Interface
The AK8850 decodes NTSC-M compatible Composite video signals, S-video and Component signals. For CCIR625 systems, only the Component signal is used. Registers control setup selection.

6-3. Input Signals
The device accepts NTSC-M Composite,S-Video,, Composite (Betacam,MII) and 625 Component signals (EBU N10). Required input signal quality is as follows.

6-3-1 Composite ,S video input signal quality

Item	Input Range	Unit	Condition
Video signal input level	± 6	dB	Video signal should be input with -6dB level (divided be a resistor), and through 0.1uF capacitor.
Color Burst input level □□□	± 10	dB	

6-3-2. Supporting signal characteristics for Composite and S-video signals

Item	Process
Lack of HSYNC	Running with self timing
Lack of VSYNC	Running with self-timing. When VSYNC is absent for two consecutive cycles, the AK8850 identifies this as a “no-signal” state and sets the NSIG pin High.
B/W Video Signal input	Set B/W mode using the register.

6-3-3. Component input signal
A Standard signal is applied in Component decode mode. Supported Component signal conditions are listed below.

Unit [mV]

Input video source	Sync level	Luminance (Setup Level)	Luminance Level (max)	Luminance (Range)	U/V (Range)	Note
BETACAM (w/o Setup)	286	0	714	714	±504	Luminance 100% U/V 100% Level
BETACAM (with 7.5% Setup)	286	53.6	714	660.4	±350	Luminance 100% U/V 75% Level
MII (w/o Setup)	300	0	700	700	±350	Luminance 100% U/V 100% Level
MII (with Setup)	300	52.5	700	647.5	±243	Luminance 100% U/V 75% Level
625 system (EBU N10)	300	0	700	700	±350	Luminance 100% U/V 100% Level

6-4. Analog Input Signal Processing

Input Selector : -60 dB (inter-channel isolation)

PGA : 0 ~ 12 dB

AD converter : operates at 27 MHz
Line-lock or Frame-lock PLL clocks are used in normal operation.

6-5. Y/C Separation Function
Adaptive Y/C separation:
Adaptive Y/C separation enables adjustment of the Chroma Signal Bandwidth. Adaptive Y/C Separation can also be fixed to either 3-line 2 dimensional Y/C separation or single dimension Y/C separation.

6-6. Output Signal Bandwidth
At Composite signal input,
Luminance Signal Bandwidth : DC ~ 5.75 MHz + 0.5 /- 1.5 dB
Chroma Signal Bandwidth : +/- 500 KHz ~ +/- 1 MHz (-3 dB) (3 ranges selectable)
At Component signal input,
Luminance Signal Bandwidth : DC ~ 5.75 MHz +0.5 / -1.5 dB
Chroma Signal Bandwidth : DC ~ 5.75 MHz +0.5 / -1.5 dB

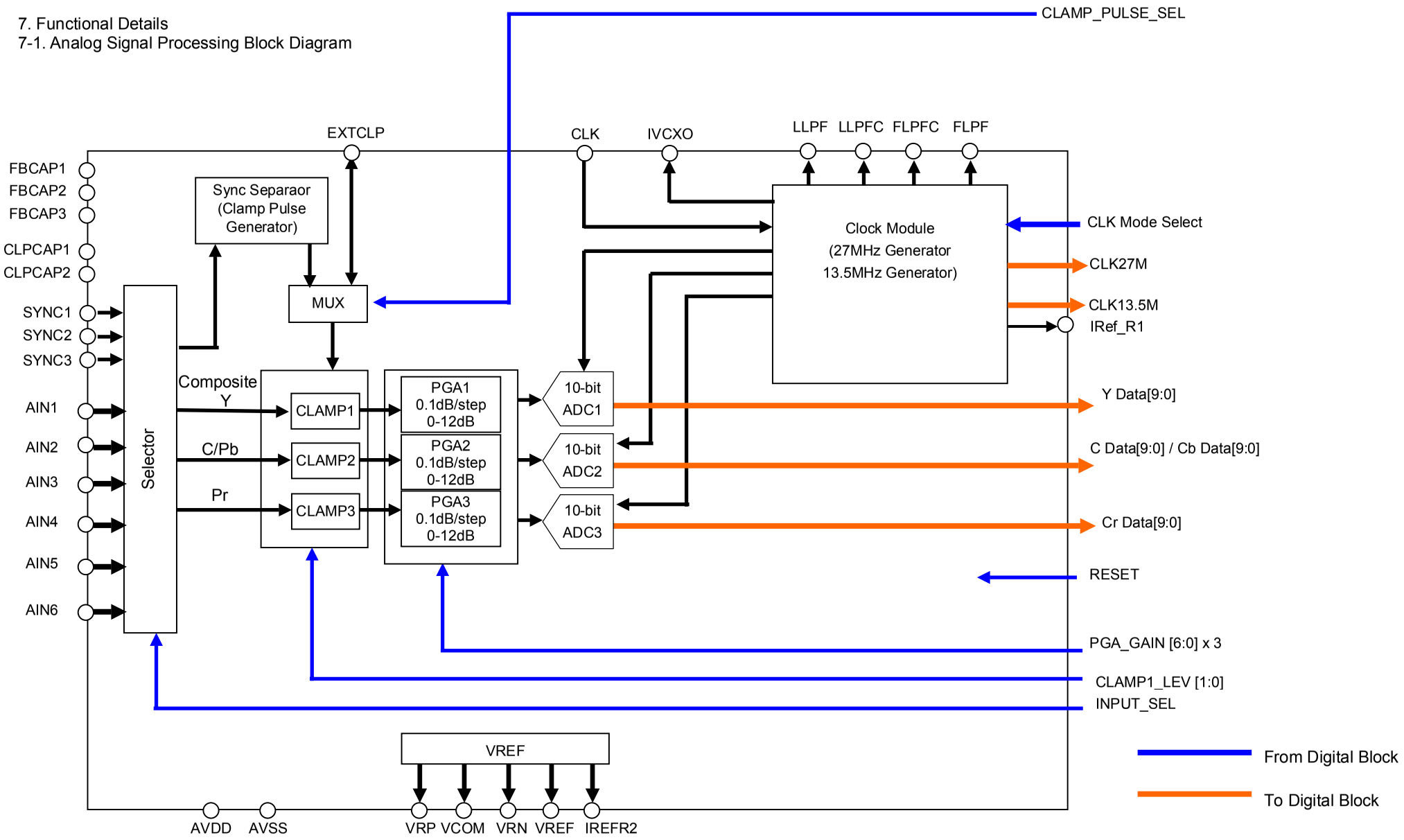
6-7. Video Quality Control Function

Contrast, Brightness, HUE and Color Saturation levels are adjustable.
No HUE adjustment is possible when a Component video signal is input.

6-8. Output Interface
- ITU-R BT.601 compatible signal output levels
- Decoded data is output in ITU-R BT.656 format (depends on the input signal quality).
- Ability to detect signals during Active Video period using HSYNC/VSYNC (FIELD)/ DVALID signals
- 8-Bit output at 27 MHz rate

6-9. Other Functions
- Black level signal is output when no signal is applied (Y = 16Cb,Cr = 128)
- ”Lack of signal” input detection
- I2C Bus Interface (400 KHz)
- Power Save Mode
- Closed Caption, VBID, WSS and Video Aspect ratio decoding Functions.

7. Functional Details
7-1. Analog Signal Processing Block Diagram



7-2. Analog Signal Process Functional Specifications

7-2-1. Input Signal Selector Module
The AK8850 has six (6) input pins. The input signal selector module selects one of the video sources. The Video sources available are single-pin Composite, 2-pin Y / C and 3-pin Component signals. A Video source to be decoded is selected by the [INPUT SIGNAL SELECT REGISTER].
The type of Video signal to be decoded is set by the [INPUT VIDEO STANDARD REGISTER].

COMPOSITE SIGNAL INPUT:
This input is digitized by the CLAMP1, PGA1 and ADC1 in the Analog Signal Processing Block Diagram. When decoding composite video, the ADC2 and ADC3 blocks can be placed in power save mode by programming the [POWER SAVE REGISTER].

Y/C SIGNAL (S-VIDEO) INPUT:
The Y-signal is digitized by the CLAMP1, PGA1 and ADC1 as in the Composite signal input case. The C Signal is digitized by the CLAMP2, PGA2 and ADC2. The ADC3 block can be placed in Power Save mode by programming the [POWER SAVE REGISTER].

COMPONENT SIGNAL INPUT:
In this case, the Y signal is digitized by the CLAMP1, PGA1 and ADC1 as in the Composite signal input case. The Pb signal is digitized by the CLAMP2, PGA2 and ADC2, while the Pr signal is digitized by the CLAMP3, PGA3 and ADC3.

Description of the input signal-type set register and input signal select control register:
The input signal type is set by the [INPUT VIDEO STANDARD REGISTER] and input signal path is selected by the [INPUT SIGNAL SELECT REGISTER].

[Input Video Standard Register]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	NENT	B/W	SETUP	VS3	VS2	VS1	VS0
Default Value							
0	0	0	0	0	0	0	0

[Input Signal Select Register]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SYNCIN1	SYNCIN0	INSEL3	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	1	0	0	0	1

[VS3 : VS0]-bit and NENT-bit setting are also described.

[Input Video Standard Register] [VS3:VS0]-bit setting

[VS3:VS0]-bit	Input Signal source	Note
0000	NTSC	
1111	Component 625 (EBU N10)	

SETUP-bit :

SETUP-bit	Setup or No-Setup	Note
0	No Setup in	
1	With Setup signal in	

B/W-bit : for Black and White video signal

B/W-bit	B/W signal or not	Note
0	Color video signal	
1	Black and White video Signal	YC separation function turns off

NENT-bit : Setting for Component signal input

NENT-bit	Signal source of Component	Note
0	MII	300mV Sync level
1	Betacam	286mV Sync level

(Supplement)
There are 3 categories of Video signals which are summarized in Table 7-2-1-1 below.

Classifying		Signal source
No. of Lines in a Frame	525-lines system	NTSC Composite
		NTSC YC
		MII Component
		Betacam Component
	625-lines system	625 (EBU-N10) Component
Sync Level	286mV Sync level (40IRE □□□□)	NTSC Composite
		NTSC YC
		Betacam
	300mV Sync level	MII Component
		625 (EBU-N10) Component

Table 7-2-1-1

The input signal path (input signal setting) is selected by [INSEL3 : INSEL0]-bits (BIT-3:BIT0) in the [INPUT SIGNAL SELECT REGISTER].
The upper 2-bits (INSEL3 : INSEL2) identify Composite /YC and Component signals.

[INSEL3:INSEL0] (bit3:bit0)□□□	Signal Select
[0,0,0,0]	No Signal is selected.
[0,0,0,1]	Composite signal is input from AIN1 (Default)
[0,0,1,0]	Composite signal is input from AIN2
[0,0,1,1]	Composite signal is input from AIN3
[0,1,1,0]	Y-Signal from AIN2 C-Signal from AIN4
[0,1,1,1]	Y-Signal from AIN2 C-Signal from AIN4
[1,0,1,1]	Y-Signal from AIN3 U-Signal from AIN5 V-Signal from AIN6

As shown in the above table ,the AK8850 accepts following 4 input signals:

- Composite signal x 3 ch
- Composite signal x 2 ch + Y / C input x 1 ch
- Composite signal x 1 ch + Y / C input x 2 ch
- Composite signal x 1 ch + Y / C input x 1 ch + Component signal x 1 ch

Please refer to item (1-6) of Section 7-2-2 CLAMP for SYNC 1 / 2 / 3 combinations.

Register settings for the various input signal types are summarized in the following Table 7-2-1-2.
For Black & White signal input, set [B / W]-bit to “1”.

Input Signal / Register bit setting	NTSC Composite□525Component								625-System
	Composite		Y/C		Component				Component
					Betacam		MII		
	Setup	No Setup	Setup	No Setup	Setup	No Setup	Setup	No Setup	No Setup
[VS3:VS0]-bit	0000	0000	0000	0000	0000	0000	0000	0000	1111
[Setup]-bit	1	0	1	0	1	0	1	0	0
[NENT]-bit	don’t care	don’t care	don’t care	don’t care	1	1	0	0	don’t care
INSEL[3:2]-bit	00	00	01	01	10	10	10	10	10

Table 7-2-1-2

7-2-2. Clamp

The CLAMP function stabilizes the AC-coupled Video input signal level. The AK8850 utilizes both an Analog Clamp circuit and a Digital Clamp circuit.
When the Composite and Y signals (S-video,Component Y signal) are input, the SYNC-TIP level or PEDESTAL level of Composite signal and LUMINANCE signal (Y) are clamped. The digitized input signal data is further signal-processed and clamped to the PEDESTAL level(digital pedestal clamp).
Clamp functions take place during the clamp pulse, as described below, in (1) SYNC SEPARATION FUNCTION.
The Clamp interval is equal to the HSYNC interval (approximately 15 KHz).
Both the C and Pb/Pr signals are clamped at the SYNC-TIP timing of the Luminance signal.

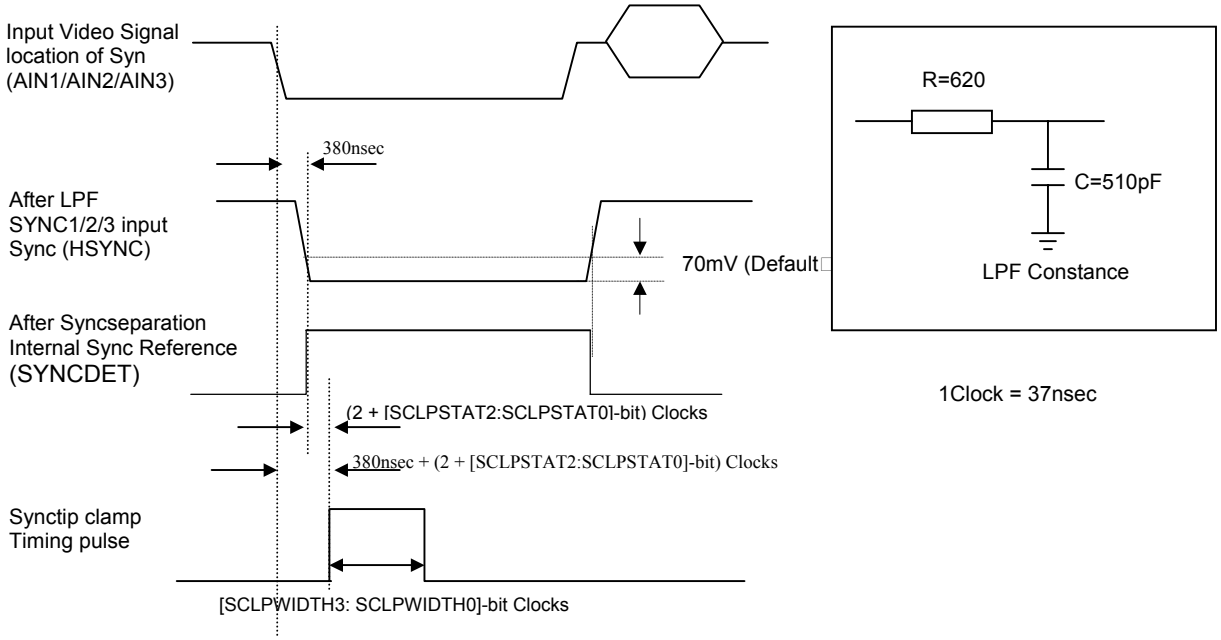
(1) SYNC SEPARATION FUNCTION(Clamp timing pulse generation)

In order to separate the SYNC signal of the target signal, the Clamp Timing Pulse is used to clamp the input signal to a pre-determined level which is fed back via the Ain pin. To generate a Clamp timing pulse ,select one of the SYNC1 / SYNC2 / SYNC3 input signals by setting [SYNCIN1 : SYNCIN0] of the (INPUT SIGNAL SELECT REGISTER).
The selected signal must be a signal which corresponds to AIN1~ AIN6 signals.
The separated SYNC signal is used for the clamp timing.
Sync-separation is done by slicing approximately 70 mV positive point (default value) from the SYNC-TIP level.
As described above, the Clamp timing pulse is generated based on the separated signal (SYNC DET).The slice point is adjustable by register settings.

(1-1) SYNC-TIP Clamp Timing Pulse
The Start point and pulse width of the SYNC-TIP timing pulse is set by the [CLAMP TIMING 1 CONTROL REGISTER].

The Start point of the SYNC-TIP timing pulse is set by [SCLPSTAT 2 : SCLPSTAT 0]-bit of the [CLAMP TIMING 1 CONTROL REGISTER] as shown below.
The CLAMP period (pulse width) is set by [SCLPWIDTH 3 : SCLPWIDTH 0]-bit of the [CLAMP TIMING 1 CONTROL REGISTER].

Clamp pulse point and pulse width setting is further described in item(1-6)SYNC-SEPARATION RELATED REGISTER DESCRIPTION.



(1-2) PEDESTAL CLAMP TIMING PULSE

The AK8850's Clamp point is initially set to the SYNC-TIP level. It is possible to clamp it at the Pedestal point by changing a register value.

The Start point of the Pedestal clamp timing pulse is set by [PCLPSTAT 2 : PCLPSTAT 0]-bit of the [CLAMP TIMING 2 CONTROL REGISTER] as shown below.

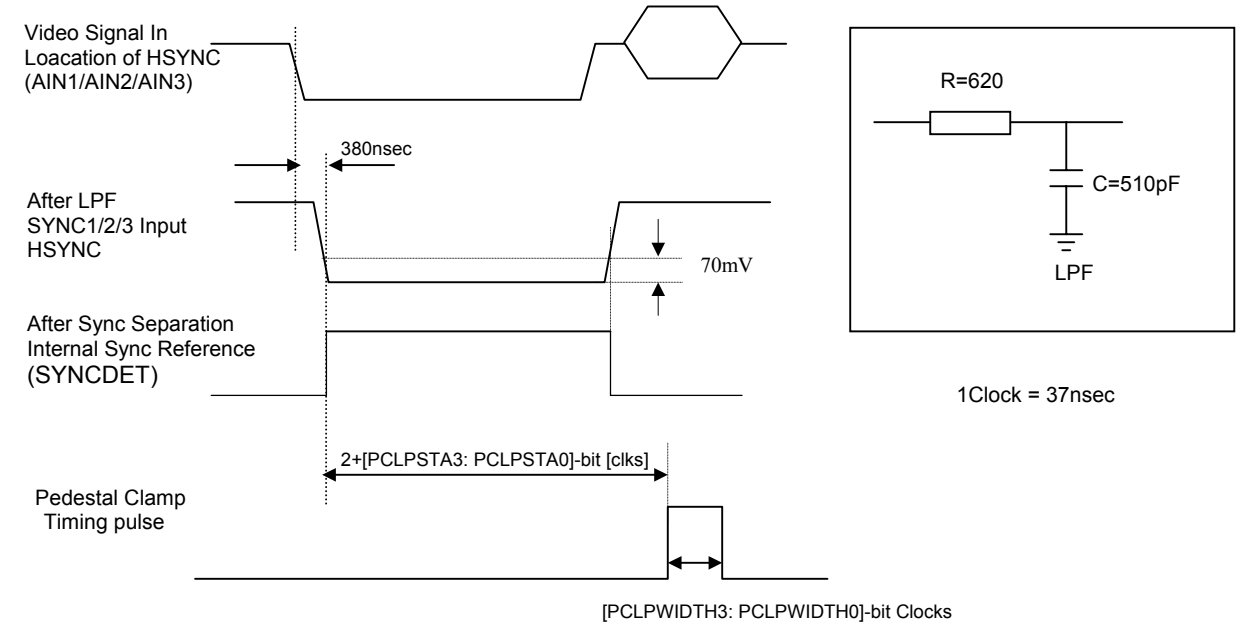
The Clamp period (pulse width) is set by [PCLPWIDTH3 : PCLPWIDTH 0]-bit of the [CLAMP TIMING 2 CONTROL REGISTER].

SYNC-SEPARATION RELATED REGISTER DESCRIPTION.

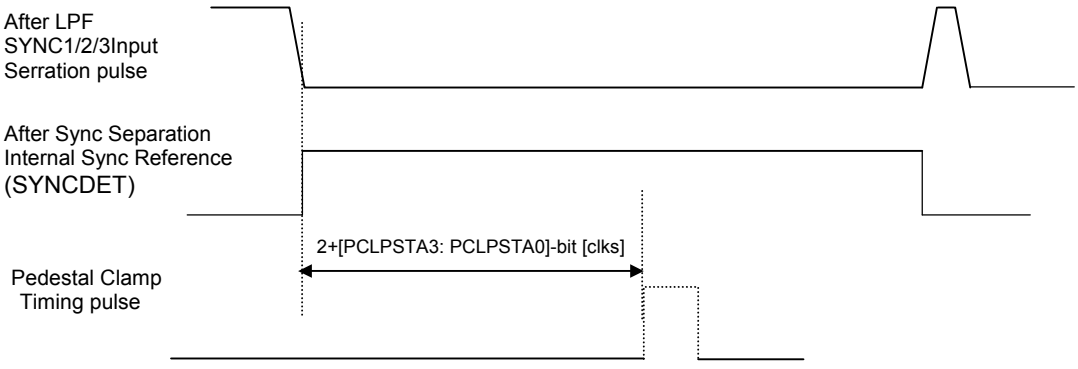
During the SERRATION pulse period, if no SYNCDET falling edge is detected before the start position set by [PCLPSTA2 : PCLSTA0]-bit, the Pedestal clamp timing pulse is not generated. This avoids mis-clamping of Serration pulse input.

* Operation with typical video input signal
* Operation with Serration pulse input signal

at HSYNC Input



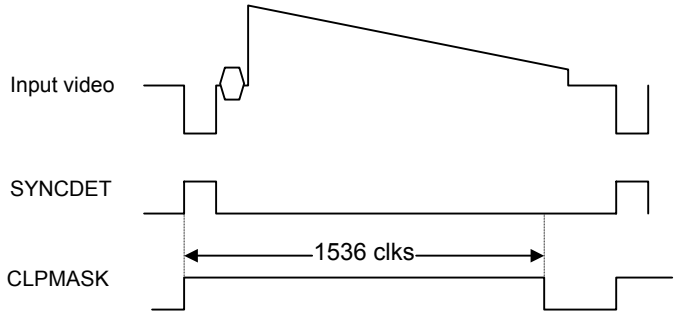
at Serration pulse Input



(1-3) CLAMP PULSE MASK FUNCTION

To avoid mis-clamping, the SYNCDET signal is masked outside the SYNC signal period. The masking period is from the rising edge of the SYNCDET signal to 1536 clock periods (1 clock = 37 ns). During this period, no SYNCDET signal is generated (refer to the timing diagram below).

This pulse mask is reset via register programming (refer to item 1-6-5).



(1-4) EXTERNAL CLAMP TIMING INPUT VIA EXTCLP PIN

It is possible to input an external clamp timing pulse via the EXTCLP pin by setting the INCLPTMG-bit and [FBCLPTMG1 : FBCLPTMG0]-bits of the [CLAMP CONTROL REGISTER]. For further register settings, please refer to item (1-6) SYNC SEPARATION REGISTER RELATED DESCRIPTION.

(1-5) CLAMP TIMING PULSE MONITOR FUNCTION

It is possible to monitor the internal clamp timing through the EXTCLP pin only when no external clamp timing is used. Output signals monitored on EXTCLP pin are SYNC-TIP clamp timing pulse, Pedestal clamp timing pulse and SYNCDET signal. The target signal is selected by [EXTCLP1 : EXTCLP0]-bit of the [CLAMP TIMING 1 CONTROL REGISTER].

(1-6) SYNC-SEPARATION RELATED REGISTER DESCRIPTION

Sync-separation and Clamp pulse related registers are [INPUT SIGNAL SELECT REGISTER], [CLAMP CONTROL REGISTER], [CLAMP TIMING 1 CONTROL REGISTER] and [CLAMP TIMING 2 CONTROL REGISTER].

Select Sync-separation signal is done using the [INPUT SIGNAL SELECT REGISTER].

[Input Signal Select Register]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SYNCIN1	SYNCIN0	INSEL3	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	1	0	0	0	1

[SYNCIN 1 : SYNCIN 0]-bit selects one of the SYNC 1 / 2 / 3 input signals to generate the clamp pulse.

[SYNCIN1:SYNCIN0] (bit5:bit4)	Target video signal for Sync separation
00	No Input
01	Video signal input from SYNC1 pin
10	Video signal input from SYNC2 pin
11	Video signal input from SYNC3 pin

(1-6-1) CLAMP TIMING PULSE SOURCE SET

Input clamp setting is done via the [CLAMP CONTROL REGISTER].

[Clamp Control Register]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
UNMASK	Reserved	ACLAMP	INCLPTMG	FBCLPTMG1	FBCLPTMG0	CLPLVL1	CLPLVL0
Default Value							
0	0	0	0	0	0	0	0

[INCLPTMG]-bit sets the clamp timing pulse of the input clamp.

INCLPTMG-bit (bit-4)	Clamp timing pulse Generation
0	Clamp timing pulse generated by Internal Clamp pulse generator
1	Clamp timing pulse from EXTCLP pin

[FBCLPTMG1 : FBCLPTMG0]-bit sets the clamp position and the clamp source.

[FBCLPTMG1:FBCLPTMG0]-bit (bit-3:bit-2)	Clamp timing pulse
00	Video signal is clamped at synctip level with internal Clamp timing pulse (Default)
01	Video signal is clamped at synctip level with External Clamp timing pulse
10	Video signal is clamped at pedestal level with internal Clamp timing pulse
11	Reserved

Combinations of INCLPTMG-bit, the [FBCLPTMG1 : FBCLPTMG0]-bit and input / output setting of the EXTCLP pin in various modes are shown in the following table. Some combinations are"Prohibited" as shown in the table, and therefore should not be selected (otherwise internal timing has priority).
Internal clamp timing monitoring is described below..

		[FBCLPTMG1:FBCLPTMG0]-bit			
		Synctip Clamp FBCLPTMG1=0		Pedestal Clamp FBCLPTMG1 =1	
		Internal Timing FBCLPTMG0=0	External Timing FBCLPTMG0=1	Internal Timing FBCLPTMG0=0	External Timing FBCLPTMG0=1
INCLPTMG-bit	0 (Internal Timing)	EXTCLP = OUTPUT Synctip Clamp	Prohibit	EXTCLP = OUTPUT Pedestal	EXTCLP = INPUT Pedestal clamp
	1 (External Timing)	Prohibit	EXTCLP =INPUT Synctip Clamp	EXTCLP = INPUT Pedestal Clamp	Prohibit

(1-6-2) INTERNAL CLAMP TIMING MONITORING FUNCTION VIA EXTCLP PIN
It is possible to monitor the clamp timing pulse on EXTCLP pin. This is enabled by the [EXTMON1 : EXTMON0]-bit of the [CLAMP TIMING1 CONTROL REGISTER].
The timing pulse monitor function is disabled when the external clamp pulse input is selected.

* [CLAMP TIMING 1 CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXTMON1	EXTMON0	SCLPWIDTH2	SCLPWIDTH1	SCLPWIDTH0	SCLPSTAT2	SCLPSTAT1	SCLPSTAT0
Default Value							
0	0	0	□	□	0	0	□

Monitoring of clamp timing is possible by setting [INCLPTMG : FBCLPTMG 1 : FBCLPTMG 0]-bit.

[INCLPTMG: FBCLPTMG1:FBCLPTMG0]-bit	Monitor with EXTCLP pin	Note
[000]	possible	Synctip Clamp
[010]	possible	Pedestal Clamp

Monitor pulse is selected as follows.

[EXTMON1:EXTMON0]-bit	Monitor source	Note
00	High Impedance (Unavailable monitoring)	Default
01	Internal Synctipu clamp timing pulse	
10	Internal pedestal clamp timing pulse	
11	SYNCDET pulse	

(1-6-3) SYNC-TIP CLAMP TIMING PULSE SET

When using the internal SYNC-TIP clamp timing pulse for clamp functions, set the start position and pulse width of the SYNC-TIP clamp timing pulse using the [CLAMP TIMING1 CONTROL REGISTER].This setting is valid only when the [INCLPTMG : FBCLPTMG1 : FBCLPTMG0]-bits are set to use the internal clamp pulse for SYNC-TIP clamping (it is invalid if external clamp pulse is used).

To monitor the clamp pulse timing generated by the internal clamp circuit, ensure that [EXTMON1 : EXTMON0]-bit of the [CLAMP TIMING1 CONTROL REGISTER] is properly set.

The slice level is adjustable by setting [SLCLV 1 : SLCLV 0]-bit of the [CLAMP TIMING 2 CONTROL REGISTER].

* [CLAMP TIMING1 CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXTMON1	EXTMON0	SCLPWIDTH2	SCLPWIDTH1	SCLPWIDTH0	SCLPSTAT2	SCLPSTAT1	SCLPSTAT0
Default Value							
0	0	0	□	0	0	0	□

Start position of the Analog SYNC-TIP clamp timing pulse is set by [SCLPSTA2 : SCLPSTAT0]-bit ,and the clamp pulse width is adjusted using the [SCLPWIDTH3 : SCLPWIDTH0]-bit.

* When [SCLPSTA2 : SCLPSTAT0]-bit and [SCLPWIDTH3 : SCLPWIDTH0]-bit are valid, settings are as follows.

[INCLPTMG: FBCLPTMG1:FBCLPTMG0]-bit	monitor with EXTCLP	Note
[000]	Available	Internal Synctip clamp pulse
[010]	Available	internal Pedestal clamp timing Pulse
[011]	Unavailable	External Pedestal clamp timing pulse

SYNC-TIP clamp pulse related settings are shown below.

* SYNC-TIP clamp pulse start position set by [SCLPSTAT2 : SCLPSTAT0]-bit

[SCLPSTAT2:SCLPSTAT0]-bit	Start position from the falling edge of Synchronization pulse	Actual Clamp pulse timing position
000	Passed after 0-Clocks (0nsec)	Passed after 2-Clocks (74nsec)
001	Passed after 2-Clocks (74nsec)	Passed after 4-Clocks (148nsec)
010	Passed after 4-Clocks (148nsec)	Passed after 6-Clocks (222nsec)
011	Passed after 6-Clocks (222nsec)	Passed after 8-Clocks (296nsec)
100	Passed after 8-Clocks (296nsec)	Passed after 10-Clocks (370nsec)
101	Passed after 10-Clocks (370nsec)	Passed after 12-Clocks (444nsec)
110	Passed after 12-Clocks (444nsec)	Passed after 14-Clocks (481nsec)
111	Passed after 14-Clocks (518nsec)	Passed after 16-Clocks (592nsec)

[SCLPSTAT2 : SCLPSTAT0]-bit is used to fine-tune the start position whose default value is [001], or 2 clocks (74ns). The clamp start position is adjusted with the [SCLPSTAT2 : SCLPSTAT0]-bit as follows. The actual clamping position occurs 2 clock cycles after sync pulse is generated..

* SYNC-TIP clamp pulse width set by [SCLPWIDTH2 : SCLPWIDTH0]-bit

[SCLPWIDTH2: SCLPWIDTH0]-bit	Pulse width
000	2-Clocks (74nsec)
001	4-Clocks (148nsec)
010	8-Clocks (296nsec) (Default)
011	16-Clocks (592usec)
100	24-Clocks (888nsec)
101	32-Clocls (1.18usec)
110	40-Clocks (1.48usec)
111	48-Clocks (1.78usec)

SYNC-TIP clamp pulse width is set using the [SCLPWIDTH2 : SCLPWIDTH0]-bit = [010], with (8 clocks = 296 ns) as the default value. Clamp pulse width can be adjusted using the [PCLPWIDTH3 : PCLDWIDTH0]-bit as shown below.

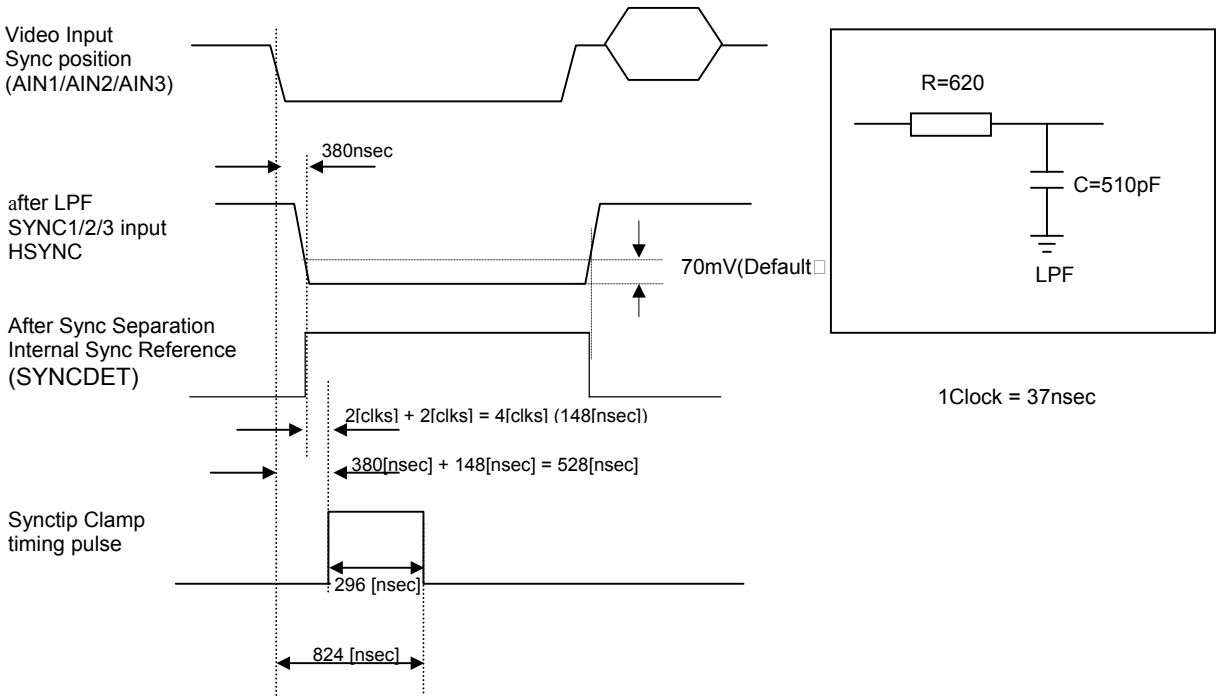
* [CLAMP TIMING2 CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SLCLV1	SLCLV0	PCLPWIDTH2	PCLPWIDTH1	PCLPWIDTH0	PSCLPSTAT2	PCLPSTAT1	PCLPSTAT0
Default Value							
0	0	0	1	1	1	0	0

Please use SLCLV1 : SLCLV0 to adjust the SYNC-TIP slice position.

[SLCLV1: SLCLV0]-bit	Slice Level
00	Sliced at the position from about 70mV over synctip.
01	Sliced at the position from about 140mV over synctip.
10	Invalid setting
11	Sliced at the position from about 105mV over synctip.

The default SYNC-TIP clamp timing pulse generates a clamp pulse as shown in the following timing diagram.



Default Synctip Clamp Timing

(1-6-4) SETTING OF PEDESTAL CLAMP TIMING PULSE

Both the start position and pulse width of the Pedestal clamp timing pulse are programmable.It is done using the [CLAMP TIMING 2 CONTROL REGISTER].

This is valid only when [INCLPTMG : FBCLPTMG1 : FBCLPTMG0]-bit is set, causing the internal clamp pulse to be used for Pedestal clamping (it is invalid if an external clamp pulse is used).

To monitor the clamp timing pulse generated by an internal clamp timing circuit, proper setting of the [EXTMON1 : EXTMON0]-bits of the [CLAMP TIMING1 CONTROL REGISTER] is required.

* [CLAMP TIMING2 CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SLCLV1	SLCLV0	PCLPWIDTH2	PCLPWIDTH1	PCLPWIDTH0	PSCLPSTAT2	PCLPSTAT1	PCLPSTAT0
Default Value							
0	0	0	1	1	1	0	0

The Start position of the Pedestal clamp timing pulse is set by [PCLPSTA2 : PCLPSTAT0]-bit,and the clamp pulse width is adjusted by [PCLPWIDTH3 : PCLPWIDTH0]-bit.

* When [PCLPSTA2 : PCLPSTAT0]-bit and [PCLPWIDTH3 : PCLPWIDTH0]-bit are valid,the setting is as follows.

[INCLPTMG: FBCLPTMG1:FBCLPTMG0]-bit	Monitoring with EXTCLP	
[010]	Available	Internal pedestal clamp timing pulse
[110]	Unavailable	External Pedestal clamp timing pulse

Set the start position and the pulse width of the Pedestal clamp timing pulse.

* Pedestal clamp timing pulse start position set by [PCLPSTAT2 : PCLPSTAT0]-bit

[PCLPSTAT2:PCLPSTAT0]-bit (bit-2:bit-0)	Start position from the falling edge of Synchronization pulse	Color subcarrier Cycles from the falling edge of HSYNC
000	Passed after 118-Clocks (4.37usec)	17Cycles
001	Passed after 126-Clocks (4.65usec)	18Cycles
010	Passed after 132-Clocks (4.88usec)	19Cycles (Color burst start position of the standard NTSC video signal)
011	Passed after 140-Clocks (5.18usec)	20Cycles
100	Passed after 148-Clocks (5.49usec)	21Cycles (Default)
101	Passed after 156-Clocks (5.77usec)	22Cycles
110	Passed after 164 Clocks (6.07usec)	23Cycles
111	Passed after 172 Clocks (6.36usec)	24Cycles

[PCLPSTAT2 : PCLPSTAT0]-bit is used to fine-tune the start position which is set to be 2 clocks later [100] as default value.

Clamp pulse start position changes as follows by [PCLPSTAT2 : PCLPSTAT0]-bit.

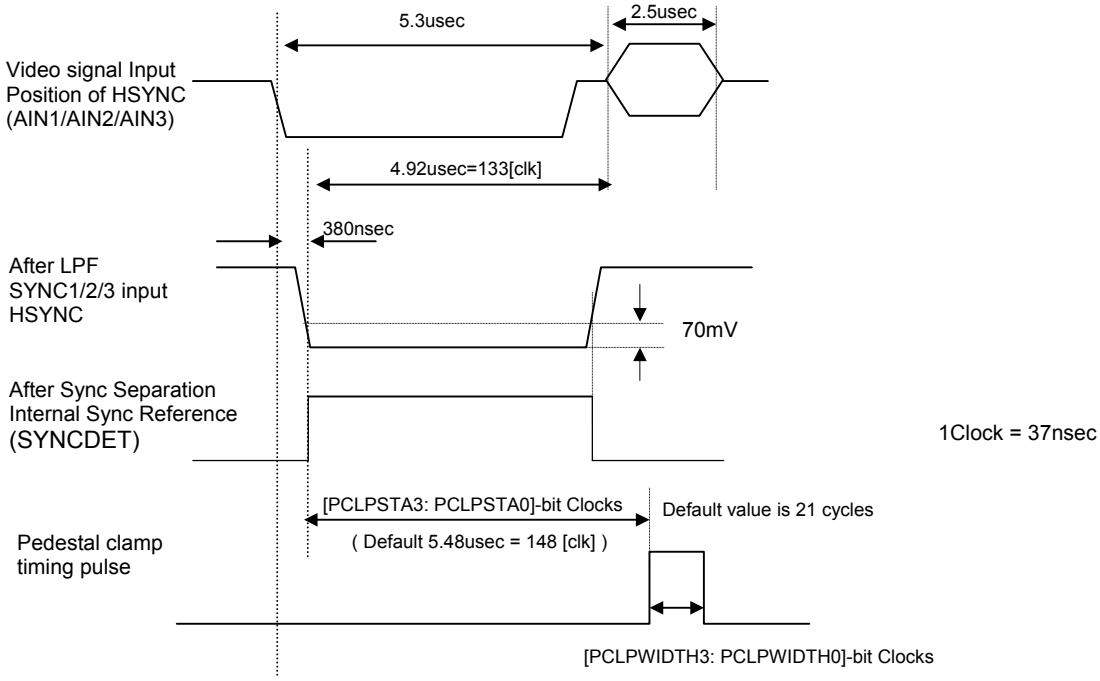
* Pedestal Clamp pulse width set by [PCLPWIDTH2 : PCLPWIDTH0]-bit

[PCLPWIDTH2: PCLPWIDTH0]-bit (bit-6:bit-4)	Pulse width
000	16-Clocks (592nsec)
001	24-Clocks (888nsec)
010	28-Clocks (1.04usec)
011	32-Clocks (1.18usec)
100	40-Clocks (1.48usec)
101	44-Clocks (1.63usec)
110	48-Clocks (1.78usec)
111	52-Clocks (1.92usec)

Pedestal clamp pulse width is set to its default value of [011] via the [PCLPWIDTH2 : PCLPWIDTH0]-bits =(32 clocks = 1.18 micro sec).

The clamp pulse width is adjusted using the [PCLPWIDTH3 : PCLPWIDTH0]-bit as follows.

The Pedestal clamp timing pulse at the default state generates a clamp pulse as shown in the following timing diagram.



Default Pedestal clamp timing

(1-6-5) CLAMP TIMING PULSE MASK FUNCTION

The Clamp timing pulse generation is masked at the default state to avoid mis-clamping outside the SYNC signal timing. This masking function can be disabled.

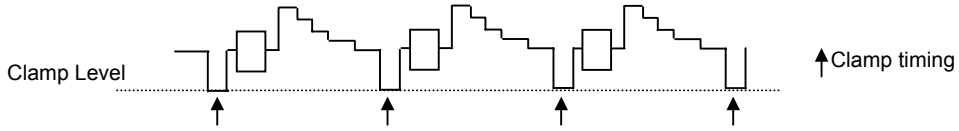
* [CLAMP CONTROL REGISTER] set is done by UNMASK-bit

UNMASK-bit	Function	
0	Masked	default
1	Un-Masked	

For typical use,please set UNMASK bit =0.

(2) INPUT SIGNAL CLAMP FUNCTION

This function clamps the input signal to a proper level. The circuit clamps the SYNC-TIP level of input signal to approximately 0.7 V. The input signal is clamped at the position as shown below.
The clamp timing pulse is controlled by either the internal Sync-separation circuit or by an externally-fed clamp timing pulse via EXTCLP pin (please refer to SYNC-TIP clamp timing pulse item).



(2-1) INPUT CLAMP CONTROL REGISTER:

* INPUT SIGNAL CLAMP ON /OFF BIT : ACLAMP-bit (bit-3)

ACLAMP	Function
0	Clamp ON (default)
1	Clamp OFF

The Input signal clamp function can be turned –off, for example, when DC signals are input..
Set ACLAMP=0 (ON) for normal operation.

(3) ANALOG CLAMP FUNCTION

This function clamps the input signal using analog signal processing for a higher degree of precision, enabling SYNC-TIP to be clamped to approximately 0.7 V by the input signal clamping.
Either of the SYNC-TIP clamp or the Pedestal clamp is selectable by the [CLAMP CONTROL REGISTER]. Clamp timing is controlled by a clamp pulse that is generated by an internal Sync-separation circuit. It is also possible to control it with an external signal connected to the EXTCLP pin. Either the SYNC-TIP clamp or the Pedestal clamp must be selected and its clamp level set by [CLPLVL 1 : CLPLVL 0]-bit.
If an internal clamp pulse is used, the selected clamp pulse can be output on the EXTCLP pin. When the C signal and Pb / Pr component signals are input, the clamp levels of CLAMP2 / CLAMP3 are set to fixed values.

(3-1) CLAMP CONTROL REGISTER DESCRIPTION

Clamp function is set by [CLAMP CONTROL REGISTER].

* [CLAMP CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPMASK	Reserved	ACLAMP	INCLPTMG	FBCLPTMG1	FBCLPTMG0	CLPLVL1	CLPLVL0
Default Value							
0	0	0	0	0	0	0	0

[CLPLVL1: CLPLVL0]-bit (bit1:bi0)	Clamp level	Note
[00]	Synctip	Clamped at synctip level. When internal clamp pulse is used, set to this mode
[01]	Pedestal	Clamped at Pedestal Level For 286mV Sync levels and Analog Pedestal Clamp settings, use this mode. 286mV Sync : NTSC Composite , Y/C signal , Betacam Component
[10]	Pedestal	Clamped at Pedestal Level For 300mV Sync level and Analog Pedestal Clamp settings, use this mode. 300mV Sync : 625 Component, MIIComponent
[11]	Clamp OFF	Analog clamp function is off

The control clamp timing is done by setting the clamp pulse timing [CLPTMG 1 : CLPTMG 0]-bit.

* Clamp timing is set by [FBCLPTMG 1 : FBCLPTMG 0]-bit (bit-3 : bit-2).

[FBCLPTMG1:FBCLPTMG0]-bit	Clamp Pulse
00	Internal Synctip Clamp pulse
01	Internal Pedestal Clamp pulse
10	External clamp timing pulse input from EXTCLP pin.
11	Reserved

* Clamp timing and clamp level are summarized in the following table.

Bit Set	Internal Clamp timing pulse				External Clamp timing pulse			
	286mV Sync signal		300mV Sync signal		286mV Sync signal		300mV Sync signal	
	Synctip Clamp	Pedestal Clamp	Synctip Clamp	Pedestal Clamp	Synctip Clamp	Pedestal Clamp	Synctip Clamp	Pedestal Clamp
[FBCLPTMG1:FBCLPTMG0]-bit	00	01	00	01	10	10	10	10
[CLPLVL1:CLPLVL0]-bit	00	01	00	10	00	01	00	10

(4) DIGITAL PEDESTAL CLAMP FUNCTION

This function clamps at the Pedestal position the Analog-clamped input signal by using digital signal processing. For details, please refer to digital portion details.

7-2-3 PGA (PROGRAMMABLE GAIN AMP)

A Programmable Gain Amp (PGA) to adjust input signals to their proper levels.

The gain range of the PGA is from 0 dB to 12 dB with the gain step of 0.1 dB / step (127 steps).When the AGC function is enabled,PGA1 / PGA 2 / PGA 3 are properly gain set by digital control. AGC function is disabled by default and the gain of each PGA is independently set via registers.

PGA Control Register description:

To manually control the PGA, the AGC function is turned off by the [CONTROL 1 REGISTER]. The AGC function is disabled by default.

* [CONTROL 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FRCSYNC	Reserved	INTPOL[1]	INTPOL[0]	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
1	0	0	0	0	0	0	0

to the AGC must be disabled in order to set PGA manually. The setting is done as follows : i.e., set [AGCT 1 : AGCT 0] = [0,0].

[AGCT1:AGCT0](bit-1:bit-0)	AGC Function
[0,0]	Disable (Default)
[0,1]	T=1Field
[1,0]	T=7Field
[1,1]	T=29Field

For further details of AGC function, please refer to the AGC description section.

* [PGA 1 /2 /3 GAIN CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA1/2/3[6]	PGA1/2/3[5]	PGA1/2/3[4]	PGA1/2/3[3]	PGA1/2/3[2]	PGA1/2/3[1]	PGA1/2/3[0]
Default Value							
0	1	0	0	0	0	0	0

Registers for setting the PGA gain values are [PGA 1 / 2 / 3 GAIN CONTROL REGISTER]. Each PGA has a corresponding register. [PGA 1 GAIN CONTROL REGISTER] example is shown here.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA1[6]	PGA1[5]	PGA1[4]	PGA1[3]	PGA1[2]	PGA1[1]	PGA1[0]
Default Value							
0	1	0	0	0	0	0	0

Each value set by PGA 1 / 2 / 3 [6 : 0]-bit uses 0.1 dB / step increments. The default gain is set to approximately 6 dB (PGA 1 /2 / 3 [6 : 0]= 0x40).

7-2-4 CLOCK MODES
The AK8850 operates under the following 3 clock modes.

(1) LINE-LOCKED CLOCK MODE
A high quality input signal from a Signal generator or DVD can be used and the corresponding Horizontal Sync Signal (HSYNC) can be extracted. A clock generated in this way is called Line-Locked Clock. Even if the Line-Locked Clock mode is selected, it is possible for the chip to be forced into Fixed–Clock mode, depending upon the input signal quality (poor or no-input signal conditions).

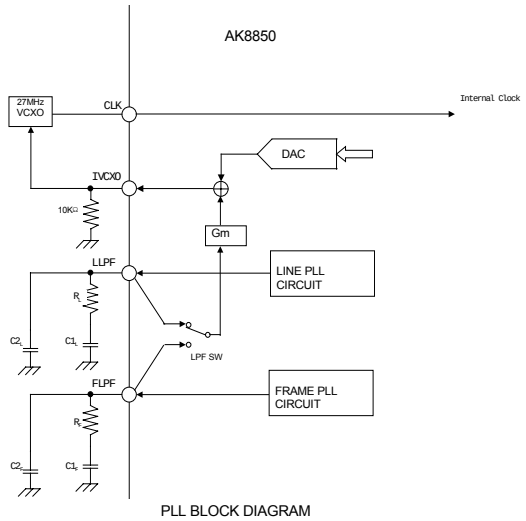
(2) FRAME-LOCKED CLOCK MODE
The Vertical Sync Signal in the input signal is used to generate a clock when skew exists in the input signal, as in the case of a VCR. A clock generated in this way is called Frame-Locked Clock. Even if the Frame-Locked Clock mode is selected, there is a case to be forced to the Fixed-Clock mode which is depending on the input signal quality (poor or no- input signal conditions).

(3) FIXED-CLOCK MODE
A clock not affected by PLL control.

(4) CLOCK AUTO TRANSITION MODE (default mode)
Depending on the characteristics of the input signal, the clock mode is automatically selected. When the auto select mode is enabled, the AK8850 automatically shifts its clock mode from / to Line-Clocked mode to / from Frame-Locked mode then to Fixed-Clock mode until it selects the optimum mode.

Since an input- signal-synchronized clock can be generated in both the Line-Locked Clock and Frame-Locked Clock modes, ITU-R BT.656 compatible output is available if the input signal quality is good enough.
In Fixed Clock mode operation, the AK8850's PLL is disabled. This clock mode is usually selected when the input signal quality is poor and the Auto Clock mode is set by Clock Mode Register. In this mode, the input clock must be synchronized with the input signal so that output data remains compatible with ITU-R BT.656 specifications.

An external VCXO clock circuit connection is shown below.
The AK8850 internally switches the Line and the Frame-Locked Loop Filter outputs, and adds the V-I converted current and the internal current DAC output together, then it outputs this value on the IVCXO pin. By connecting an external resistor to this pin, a control voltage to the external VCXO is provided. A voltage to control the oscillating center frequency of the VCXO is adjustable by setting the above-mentioned current DAC input code, using the PLL-DAC Code Set Register (address : 0x47). In this case, adjusting the external VCXO oscillating center frequency is accomplished by selecting the Fixed Clock mode [CONTROL 2 REGISTER].



PLL BLOCK DIAGRAM

Clock Control Register Description :
Clock mode is controlled by the [CONTROL

* [CONTROL 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	ACC1	ACC0	DPCC1	DPCC0	DPCT1	DPCT0
Default Value							
1	1	0	0	0	0	0	1

* [CLKMODE1 : CLKMODE0]-bit set

[CLKMODE1: CLKMODE0]	□□□□□□□	
00	Fixed clock	External Clock mode
01	Line-Locked Clock	Line Lock Clock mode According to the input video signal quality, AK8850 works in Fixed clock mode.
10	Frame-Locked Clock	Frame Lock Clock mode According to the input video signal quality, AK8850 works in Fixed clock mode.
11	Auto Clock Mode	According to the Input video signal quality, Clock mode is switched to the most suitable clock mode.(default)

The VCXO's oscillating center frequency control voltage is adjusted by setting the DAC output current value [PLL DAC SET REGISTER]. In Fixed Clock mode operation, the VCXO oscillating frequency is fixed by the value set here.

* [PLL DAC SET REGISTER]

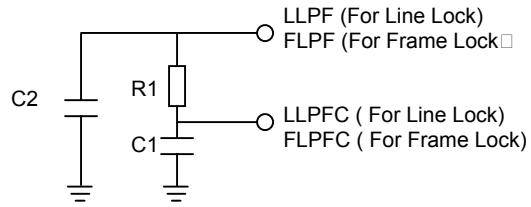
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PLLDACI7	PLLDACI6	PLLDACI5	PLLDACI4	PLLDACI3	PLLDACI2	PLLDACI1	Reserved
1	0	0	0	0	0	0	0

The DAC's upper 7 bits are valid. Adjustable DAC current value ranges are as follows.

PLLDAC[7:1]	□□□[uA]□Typ.)
0000000	0
1111111	127

(7-2-5) LOOP FILTER

The AK8850 requires external loop filters. Proper loop filters should be connected for the Line-Locked and the Frame-Locked PLLs respectively. The optimum value of the loop filter constant varies with the VCXO gain [ppm / V] characteristics.



An example of the loop filter constant for a 100 ppm/V VCXO is shown (IVCXO output load resistor at 10 Kohm).This loop filter constant (reference value) is set by the [PLL CONTROL REGISTER] (Sub address 0x46) [LPGAUTO]-bit

	[LPGAUTO] - bit = 0 (Default)			[LPGAUTO]-bit = 1		
	R	C1	C2	R	C1	C2
Line Lock	9.1kΩ	6.8uF	0.68uF	18kΩ	3.4uF	0.34uF
Frame Lock	5.6MΩ	0.18uF	0.018uF	3.3MΩ	0.3uF	0.03uF

(7-2-6) ADC

The AK8850 integrates three 27 MHz 10-bit ADCs (ADC1 / ADC2 / ADC3).Each ADC can be disabled by the [POWER SAVE MODE REGISTER].

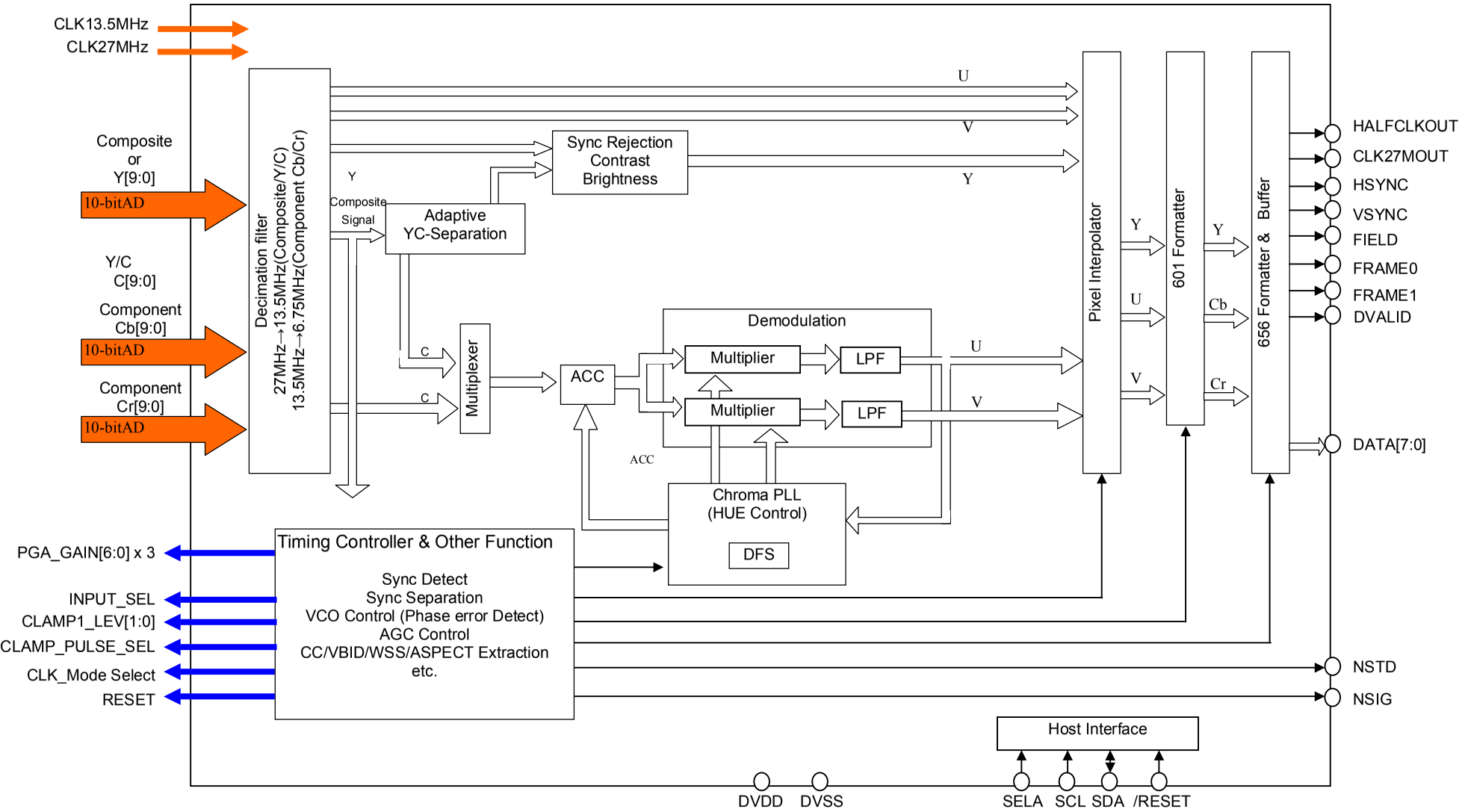
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	ADC2	ADC1	ADC0	PS
Default Value							
0	0	0	0	0	0	0	0

* ADC1 /2 / 3 – bit set

ADC1/2/3-bit	Function	Note
0	ADC1/2/3 Active mode	
1	ADC1/2/3 Sleep mode	Each ADC can be set sleep mode individually

7-3 DIGITAL SIGNAL PROCESSING BLOCK DIAGRAM

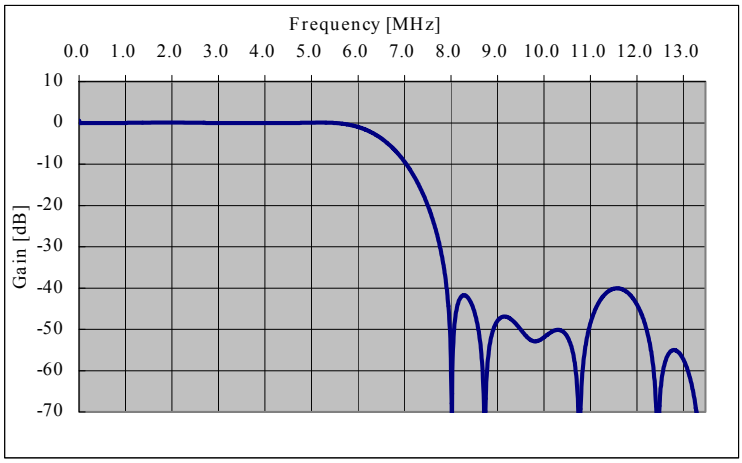
7-3-1 Digital Block Details



7-4 DIGITAL SIGNAL PROCESSING FUNCTIONAL SPECIFICATION

7-4-1 Decimation Filter

Composite, YC, and Component input signals are sampled at 27 MHz and then are down- sampled to 13.5 MHz by the Decimation Filter. The Frequency Response of the Decimation Filter is shown as follows.



7-4-2 SYNC-Separation, SYNC-Detection, Phase-Error Detection

This detects SYNC-signal position of the discrete signal. The detected SYNC signal controls the PLL.

7-4-3 DIGITAL PEDESTAL CLAMP

This sets the digitized data Pedestal position 240 / 252 levels (286 mV-type SYNC / 300 mV-type SYNC). This function decreases the effect of SYNC level depth variations in the video. The control-time-constant and non-sensing bandwidth can be set by the [CONTROL 2 REGISTER].
For 286 mV-type SYNC and 300 mV-type SYNC details, please refer to [Table 7-2-1-1] in section [7-2-1 INPUT SIGNAL SELECTOR MODE].

Digital Pedestal Clamp Control Register description :

* [CONTROL 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	ACC1	ACC0	DPCC1	DPCC0	DPCT1	DPCT0
Default Value							
1	1	0	0	0	0	0	1

The control-time-constant is set by the [DPCT1 : DPCT0]-bit ,and the non-sensing bandwidth is set by the [DPCC1 : DPCC0]-bit.

[DPCT1:DPCT0]	Pedestal Clamp	Time Constance
00	OFF	
01	Fast (Default)	About 1.5-Lines
10	Middle	About 3.5-Lines
11	Slow	About 7.5-Lines

* Non-Sensing Bandwidth of the Pedestal Clamp is set as follows.

[DPCC1:DPCC0]	286mV SYNC Pedestal Level 240	300mV Sync Pedestal Level 252
00 □Default□	Pedestal level is not 240, digital pedestal clamp function works.	Pedestal level is not 252, digital pedestal clamp function works.
01	Non-Sensing Bandwidth : +/- 1LSB □Pedestal Level is not in the range of 238 - 241, digital pedestal clamp function works□	Non-Sensing Bandwidth : +/- 1LSB □Pedestal Level is not in the range of 250 - 253, digital pedestal clamp function works□
10	Non-Sensing Bandwidth : +/- 2LSB □Pedestal Level is not in the range of 236 - 243, digital pedestal clamp function works□	Non-Sensing Bandwidth : +/- 2LSB □Pedestal Level is not in the range of 248 - 255, digital pedestal clamp function works□
11	Non-Sensing Bandwidth : +/- 3LSB □Pedestal Level is not in the range of 232 - 247, digital pedestal clamp function works□	Non-Sensing Bandwidth : +/- 3LSB □Pedestal Level is not in the range of 244 - 259, digital pedestal clamp function works□

7-4-4 AGC (Automatic Gain Control)

This function sets the PGA gain so that input level is properly set. The PGA gain is calculated so that the SYNC level is equal to 40 IRE / 300 mV (286 mV-type Sync / 300 mV-type Sync) and its value is set to PGA (classification of 286 mV-type Sync and 300 mV-type Sync is listed in Table 7-2-1-1).

Gain-calculation and Gain-set are performed during the VBI interval of each Field.

The AGC time constant is programmable in 3 steps using the [CONTROL 1 REGISTER]. The PGA gain is derived from the SYNC level information only.

AGC is performed only on the Composite signal and the Y portion of the YC input and Component input signals. Auto gain is not performanced on the C-signal or Pb / Pr signals.

It is assumed that correction of the C-signal is done using the ACC of the digital portion. Correction of the Component Pb /Pr signals should be manually done using the Color Saturation Control function.

When the AGC function is disabled by the [CONTROL 1 REGISTER], the gain of each channel can be manually set via the [PGA1 / PGA 2 / PGA 3 GAIN CONTROL REGISTER].

AGC Control Register Description:

AGC is controlled by the [CONTROL 1 REGISTER].

* [CONTROL 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FRCSYNC	Reserved	INTPOL[1]	INTPOL[0]	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
1	0	0	0	0	0	0	0

AGC set is defined as follows.

Enable / Disable and the Time-Constant (T) of the AGC are set .

[AGCT1:AGCT0](bit-1:bit-0)	AGC Function
[0,0]	Disable (Default)
[0,1]	T=1Field
[1,0]	T=7Field
[1,1]	T=29Field

The AK8850 sets the PGA value so that the SYNC-TIP level is equal to 40 IRE / 300 mV (286 mV-type Sync / 300 mV-type Sync) while the AGC is enabled.

The 286 mV-type Sync here means NTSC Composite, NTSC YC input and Betacam Component signals, while the 300 mV-type Sync means 625 Component and MII Component signals.

40 IRE / 300 mV (286 mV-type Sync / 300 mV-type Sync) are equivalent to 240 / 252 (10-bit) in digital code. As the SYNC-TIP is set to 16 (10-bit), Sync sizes are equivalent to 224 / 236 (10-bit) respectively.

	Sampled Digital Code	Sync level
286mV SYNC	240	224
300mV SYNC	252	236

While the AGC is enabled, manual gain adjustment is not possible by the PGA1 / PGA2 / PGA3 GAIN CONTROL Registers (AGC has higher priority than manual gain adjustments).

It is also possible to program the non-sensing bandwidth of the AGC by [AGCC1 : AGCC0]-bit of the [CONTROL 1 REGISTER].

[AGCC1:AGCC0](bit-3:bit-2)	286mV Sync	300mV Sync	Non-Sensing Bandwidth
[0,0]	Sync level is not 224, AGC function works.	Sync level is not 236, AGC function works.	No Non-Sensing Bandwidth
[0,1]	Sync level is not in the range of 222 - 225, AGC function works.	Sync level is not in the range of 234 - 237, AGC function works.	1-bit Non-Sensing Bandwidth
[1,0]	Sync level is not in the range of 220 - 227, AGC function works.	Sync level is not in the range of 232 - 239, AGC function works.	2-bit Non-Sensing Bandwidth
[1,1]	Sync level is not in the range of 218 - 229, AGC function works.	Sync level is not in the range of 230 - 241, AGC function works.	3-bit Non-Sensing Bandwidth

Same gain as for the Y signal input case is multiplied to the C-signal in Y / C input and the Pb / Pr signals in Component signal input.
The gain constant value set for the AGC does not affect to any of the [PGA1 / PGA2 / PGA3 GAIN CONTROL REGISTER], regardless of input sources.

7-4-5 Y / C SEPARATION

The Y / C Separation function separates the Composite Video input signal into Luminance (Y) and Chroma signals (C). Three register-selectable Y / C Separation methods are available: Primary Y/C Separation (Band Pass Filter), Two Dimensional Y/C Separation (3-Line Comb Filter) and an Adaptive Y/C Separation Filter.
For Y/C Separation, the input data is converted CCIR601 compatible formats and it is output as a Y signal when the Black & White mode is selected, during the VBI interval set by [VBIL4 : VBIL0]-bit of the [VERTICAL BLANKING LENGTH REGISTER]. The output Cb/Cr signal is at 0x80, or Black level.The resulting output on the AK8850 is selected by VBIDEC-bit of the [VERTICAL BLANKING LENGTH REGISTER]. Black level output (Y= 0x16,Cb/Cr=0x80) at VBIDEC-bit = 0 and Black & White output at VBIDEC-bit=1.
The Y/ C Separation function is enabled only when a Composite signal is input.

Y/C Separation Control Register Description :
The Y/C Separation is controlled by the [Y/C SEPARATION CONTROL REGISTER].

* [Y/C SEPARATION CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	CBPFS1	CBPFS0	YCSEP1	YCSEP0
Default							
0	0	0	0	0	1	1	0

The Y/C Separation mode is set as follows.

[YCSEP1:YCSEP0] (bit-1:bit-0)	YC-Separation mode
00	3-Line 2-D YC-Separation
01	1-Line BPF YC-Separation
10	Adaptive 3-Line 2-D YC-Separation (Default)
11	Reserved

3 types of the Color Band–Limiting Filters are selectable which are used for Y/C Separation. Use the[Y/C SEPARATION CONTROL1 REGISTER] to select.
The Band Limiting Filters are applicable for all Y/C Separation modes (in Black & White mode, filter selection becomes invalid since the Y/C Separation function is disabled).

[CBPFS1:CBPFS0] (bit-3:bit-2)	Chroma Bandwidth	Filter characteristic□-3dB□
00	OFF	OFF
01	Wide (Default)	+/- 1MHz
10	Middle	+/- 750kHz
11	Narrow	+/- 500kHz

7-4-6 ACC (Auto Color Control)

This function adjusts the Color Burst level of the C-signal input to its appropriate level, which is 40 IRE (with NTSC Composite ,Y/C input). The adjustable range is from –12 dB to + 12 dB. The ACC processing can be turned on or off by the [CONTROL 2 REGISTER]. Its function is valid for Composite and Y/C inputs (invalid for Component input).

ACC Control Register Description :

ACC is controlled by [CONTROL 2 REGISTER].

* [CONTROL 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	ACC1	ACC0	DPCC1	DPCC0	DPCT1	DPCT0
Default Value							
1	1	0	0	0	0	0	1

Enable/Disable and the Constant (T) of the ACC are set as follows.

[ACC1:ACC0](bit-5:bit-4)	ACC Function
[0,0]	Disable (Default)
[0,1]	T=2-Field
[1,0]	T=8-Field
[1,1]	T=30-Field

The ACC and the Color Saturation adjustments function independently.

7-4-7 COLOR KILLER

The signal quality of the Chroma signal is evaluated from the Color Burst level of input signal. If this level is lower than a target level, the Chroma signal decoding process is not performed. When the Standard 40 IRE Color Burst input signal level becomes lower than the pre-set value (presettable range is from –17 dB to – (infinite),-20 dB at default), the Color Killer function is activated.The Cb/Cr output signal is fixed to 0x80.

When the Color Killer is activated, the C-data output is 0x80, (Black & White mode). Since the Color Killer function checks the Color Burst signal, it is disabled when the Component signal is selected.

Operating range of the Color Killer can be set from –17 dB to – (infinite). It can be turned on or off by the [COLOR KILLER CONTROL REGISTER].

When the Color Killer process is executed, the Chroma signal output becomes Black level (0x80) which is a similar level in the Black & White mode. However, since the C-signal is subtracted from the Composite signal by the Y/C Separation block, the output result differs from the Black & White mode.

Color Killer Control Register Description :

Color killer function is controlled by the [COLOR KILLER CONTROL REGISTER].

* [COLOR KILLER CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CL_KILL	Reserved	CKLVL5	CKLVL4	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
1	0	1	0	1	1	0	1

* Turning on and off of the Color Killer function is set by CL-KILL-bit (bit-0)

CL_KILL-bit (bit-7)	Color Killer
0	OFF (Disable)
1	ON (Enable) Default

* Turning on and off of the Color Killer function is set by CL-KILL-bit (bit-0)

The Color Killer level setting is given in the following equation:

ON / OFF decision level of the Color Killer is made by checking the U level after de-modulating the Color Burst signal. A proper input signal gives the U-signal a level of 112. A decision is made within the device by multiplying by 4 the U-signal after de-modulating the input signal. The register set value [CKLVL5 :CKLVL0] is given as:

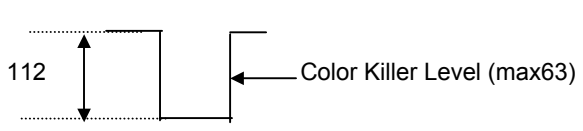
[CKLVL5 : CKLVL0]=10 exp(clk/20) *448

where CKL [dB] is the level to enable Color Killer.

In reverse, the Color Killer enable level is calculated from the register set value as :

Input U level = 20 *log ([CKLVL5 : CKLVL0] / 448)

i.e., when a lower-than-the input U level signal is input, the Color Killer is activated.



Set to 63(max), when the calculated value which is 4 times the demodulated U-signal is less than 63, Color killer is active.

7-4-8 BLACK & WHITE MODE

Black & White mode outputs all input signals as luminance (Y) only. In this mode, the C-signal output becomes 0 level (output code 0x80) and Y/C Separation function is turned off (Black & White mode).
If Y/C and Component signals are input, the Chroma signal to be output is fixed to 0x80. The Black & White mode is user programmable and it is turned on and off by the [INPUT VIDEO STANDARD REGISTER].

Black & White Mode Control Register Description:
Black & White mode is controlled by the [INPUT VIDEO STANDARD REGISTER]

* [INPUT VIDEO STANDARD REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	NENT	B/W	SETUP	VS3	VS2	VS1	VS0
Default Value							
0	0	0	0	0	0	0	0

* ON / OFF of Black & White mode function is controlled by B/W-bit (bit-5)

B/W-bit (bit-5)	B/W mode set
0	OFF (Color Video signal : default)
1	ON (B/W video signal

* Output Status in Black & White mode (at B/W-bit = 1).

	Output data
Y Singal out	Level converted value to Rec.601 level.
Cb/Cr Signal out	Fixed value at 0x80

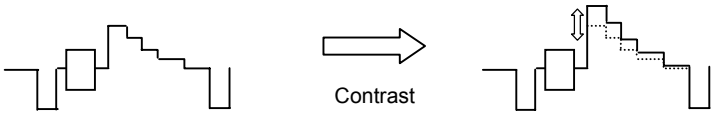
Above output status is applicable for NTSC (Composite Y/C) and 525 & 625 Component signals.

7-4-9 PICTURE ADJUSTING FUNCTION

The AK8850 has Picture Quality Adjusting functions which include Contrast, Brightness, Color Saturation and HUE adjustments.

(1) CONTRAST

The Contrast adjustment is made by multiplying the Luminance signal (Y) by the gain factor which is set by the [CONTRAST CONTROL REGISTER].
The Contrast adjustment is made within the range of 0 ~ 2 (1/ 255 step).
These arithmetic operations areperformed on 10-bit data. When the result exceeds the specified range,it is clipped to 1023 (upper limit) or to 0 (lower limit).



Contrast Control Register :

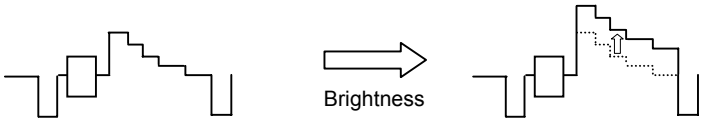
* [CONTRAST CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Sets a multiplying factor over the Luminance signal. Adjustable range is from 0 ~ 2 in 0.008 fraction per step. Default value is 0x80.

(2) BRIGHTNESS

Brightness adjustment is accomplished by adding an offset factor to the Luminance signal which is set by the [BRIGHTNESS CONTROL REGISTER]. The adjustable range is +/- 200 (255 steps). Arithmetic operations are performed on the 10-bit data. When the result exceeds the specified range,it is clipped to 1023 (upper limit) or to 0 (lower limit).



Brightness Control Register :

* [BRIGHTNESS CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

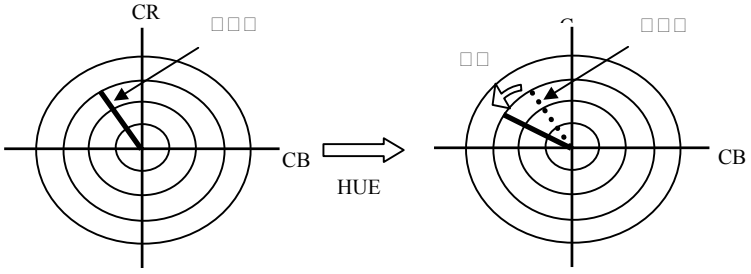
Increases the value of the Luminance signal. Arithmetic operations are done on the 10-bit data and adjustable range is from – 128 to + 127 with 1 fraction per step. The adjustable value per step of the ITU-R BT.601 compatible output is shown in the table below. The register is expressed in 2's complement form and its default value is 0x00.

* Adjustable Value Per Each Step

Input Video Signal	Add Value (rounding)	Note
286mV Sync without Setup	1 [BR7:BR0]*100/255	NTSC Composite/YC /Betacam
286mV Sync (with Setup)	1 [BR7:BR0]*108/255	NTSC Composite/YC /Betacam
300mV Sync (without Setup)	1 [BR7:BR0]*102/255	MII / EBU-N10
300mV Sync (with Setup)	1 [BR7:BR0]*111/255	MII

(3) HUE CONTROL

HUE adjustment is made by rotating the Chroma signal by a predetermined angle which is set by the [HUE CONTROL REGISTER]. HUE adjustment ranges from – 90 degrees to + 90 degrees (1/255 step). HUE control is valid only when either a Composite orY/C signals are input.



Hue Control Register :

* [HUE CONTROL REGISTER]

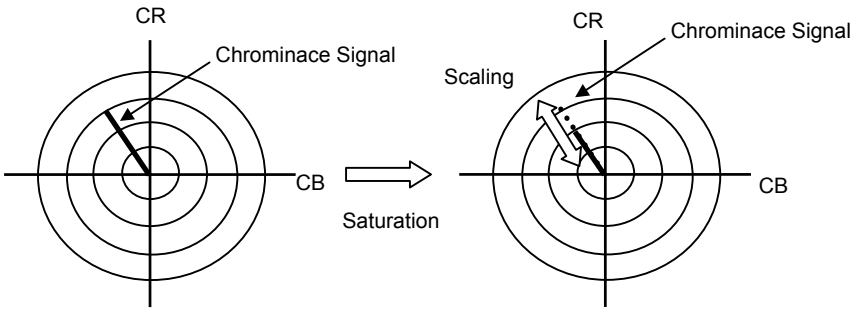
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

Sets the rotation angle of HUE. Adjustable range is +/- 90 degrees with 0.7 degree HUE rotation per step. Default value is the un-adjusted 0x00. The value is in 2's complement format. The HUE control is valid only when the Composite or Y/C signals are input (it is disabled for Component input).

NTSC(525 System)				625 System
Composite	Y/C	Component		Component
		Betacam	MII	
This Register is functioned		This Register is disable		This register is Disable

(4) COLOR SATURATION

Color Saturation adjustment is made by multiplying the Chroma signal with a gain factor which is set by the [SATURATION CONTROL REGISTER]. The Color Saturation is adjustable range is from – (infinite) to + 6 dB (1/ 255 step). Arithmetic operations are performed on the 10-bit data. When the result exceeds the specified range, it is clipped to 1023 (upper limit) or to 0 (lower limit).



Saturation Control Register :

* [SATURATION CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

Sets the Chroma signal multiplying factor. The adjustable range is from – (infinite) to + 6 dB (0 ~ 2) with 0.008 fraction per step. Default value is 0x80.

7-4-10 VERTICAL BLANKING INTERVAL

This section describes setting the Vertical Blanking Interval (VBI) and to set tasks to be performed during this interval.
The Vertical Blanking Interval is set by [VBIL4 : VBIL0]-bit of the [VERTICAL BLANKING LENGTH REGISTER].(hereafter,VBI period means an interval defined by [VBIL4 : VBIL0]-bit).
Default value is 0x14 (20 lines). For normal operation, it is recommended to set the VBI interval to be more than 9 / 7 (525 line system / 625 line system).
The V-bit transition point of the Video Timing Reference Code can be altered by the TRSVSEL-bit of the [VERTICAL BLANKING LENGTH REGISTER]. TRSVSEL-bit selects either of the ITU-R BT.656 or SMPTE 125M Standards compatibility. The relationship between TRSVSEL-bit and the Video Timing Reference Code V-bit is shown in the table below.

TRSVSEL-bit	Standard
0	ITU-R BT.656
1	SMPTE125M

During the VBI period, the black level (Y = 0x10,Cb/Cr= 0x80) is output by default.
By setting the VBIDEC-bit of the [VERTICAL BLANKING LENGTH REGISTER] to [1], the Y/C Separation function on those lines which are specified during VBI interval is turned off and input signal is directly output as a Y signal. The SETUP-bit of the [INPUT VIDEO STANDARD REGISTER] becomes invalid during VBI period (no setup process is executed).
Turning the setup process on /off on the latter half of a scan line line (0.5 H) can be controlled by the HALFSU-bit which is applied only to the first line of the second Field of Active Video.

VBID Control Register Description :
* [VERTICAL BLANKING LENGTH REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC	TRSVSEL	HALFSU	VBIL4	VBIL3	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	1	0	1	0	0

The VBI period is set by [VBIL4 : VBIL0]-bit. NTSC default values and typical setups of 625 Component signals are shown in the table below.

[VBIL4:VBIL0]-bit	525 System				625 System
	Composite	Y/C	Component		Component
			Betacam	MII	
	0x14□Default□ (20-Decimal)				0x18 (24-Decimal)
VBI-Line	Line1 ~ Line20 Line263.5 ~ Line283.5 (from 430th pixedl of Line-263 to 429th pixel of Line-283)				Line623.5 ~ Line625 Line1 ~ Line22.5 Line311 ~ Line335

The VBI start line period for 625 Component Video is Line 624.
The VBI period of Field –2 is given as :
For 525 system, from 264 (fixed value) to (set-value) + 245.
For 625 system,from 311 (fixed value) to (set value) + 311.

TRSVSEL-bit is the control bit that specifies the V-bit in the REC. 656 EAV/SAV code.
This bit is set by [VBIL4 : VBIL0] and is not affected by VBI period as shown below.

* < V-bit value in Rec.656 TRS and the line relationship >

V-bit	NTSC(525 System) Composite/YC/Component(MII,Betacam)		625 System Component (EBU N10)	
	TRSVSEL=0	TRSVSEL=1	TRSVSEL=0	TRSVSEL=1
V-bit = 0	Line10 ~ Line263 Line273 ~ Line525	Line20 ~ Line263 Line283 ~ Line525	Line23 ~ Line310 Line336 ~ Line623	
V-bit = 1	Line1 ~ Line9 Line264 ~ Line272	Line1 ~ Line19 Line264 ~ Line282	Line1 ~ Line22 Line311 ~ Line335 Line624 ~ Line625	

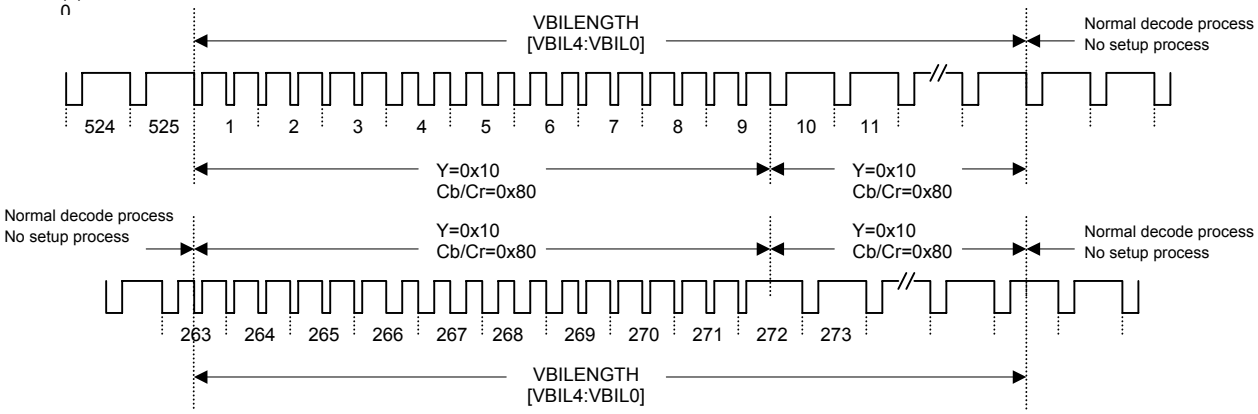
note) TRSVSEL-bit setting is as shown above. It is not affected by [VBIL4 : VBIL0]-bit.
TRSVSEL-bit setting is shown above for all modes of 525/625 systems.

VBIDEC-bit is the control bit that specifies the device operation during the period is assigned by VBI [4 : 0]-bit. The output code is determined by the VBI period , VBIDEC-bit, HALFSU-bit and SETUP-bit of the [INPUT VIDEO STANDARD REGISTER]. When HALFSU-bit = 1, the SETUP processing is executed on the latter half 0.5 H time of the first Line in the second Field.
Output status is shown in the following table.

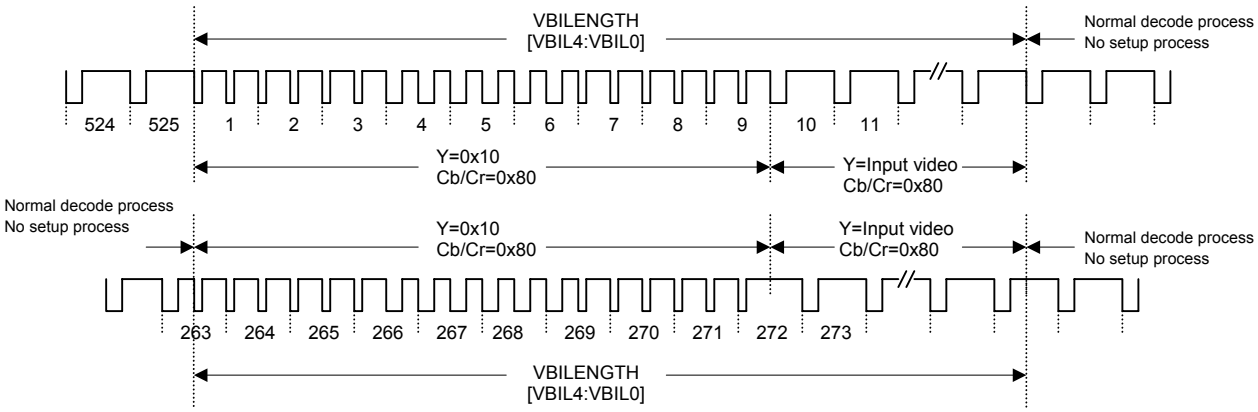
NTSC (525 System)

			VBIDEC-bit = 0		VBIDEC-bit = 1	
			HALFSU-bit = 0	HALFSU-bit=1	HALFSU-bit=0	HALFSU-bit=1
SETUP-bit = 0	1st Field	Line-1 - Line-9	Y = 0x10 C = 0x80	←	←	←
		Line-10 - [VBIL4:VBIL0]	Y = 0x10 C = 0x80	←	Y =Input Signal C = 0x80 No Setup Process	←
		[VBIL4:VBIL0] + 1 - Line-263.5 (till 429th pixel of Line-263)	Normal decode procidure No Setup Process	←	←	←
		Line-263.5 (from 430th pixel of Line-263) - Last pixel of Line263	Y = 0x10 C = 0x80	←	←	←
	2nd Field	Line-264 - Line-272.5 (till 429th pixel of Line272)	Y = 0x10 C = 0x80	←	←	←
		Line-272.5 (from 430th pixel of Line-272) - 263.5 + [VBIL4:VBIL0] (till 429th pixel of Line(263+[VBIL4:VBIL0]))	Y = 0x10 C = 0x80	←	Y =Input signal C = 0x80 No Setup Process	←
		263.5 + [VBIL4:VBIL0] (from 430th pixel of Line(263+[VBIL4:VBIL0])) - Line-263.5 + Last pixel of [VBIL4:VBIL0] (858th pixel of Line(263+[VBIL4:VBIL0]))	Normal decode procidure No Setup Process	←	←	←
		Line-264 + [VBIL4:VBIL0] - Line-525	Normal decode procidure No Setup Process	←	←	←
SETUP-bit = 1	1st Field	Line-1 - Line-9	Y = 0x10 C = 0x80	←	←	←
		Line-10 - [VBIL4:VBIL0]	Y = 0x10 C = 0x80	←	Y =Input Signal C = 0x80 No Setup Process	←
		[VBIL4:VBIL0] + 1 - Line-263.5 □Line-263 □ 429 □□□□□□□□	Normal decode procidure Setup Process	←	←	←
		Line-263.5 (from 430th pixel of Line-263) - the last pixel of Line263	Y = 0x10 C = 0x80	←	←	←
	2nd Field	Line-264 - Line-272.5 (till 429th pixel of Line272)	Y = 0x10 C = 0x80	←	←	←
		Line-272.5 (from 430th pixel of Line-272) - 263.5 + [VBIL4:VBIL0] (till 429th pixel of Line(263+[VBIL4:VBIL0]))	Y = 0x10 C = 0x80	←	Y =Input Signal C = 0x80 No Setup Process	←
		263.5 + [VBIL4:VBIL0] (from 430th pixel of Line(263+[VBIL4:VBIL0])) - the last pixel of Line-263.5 + [VBIL4:VBIL0] (till 858th pixel of Line(263+[VBIL4:VBIL0]))	Normal decode process No Setup Procedure	Normal decode process Setup Process	Normal decode process No Setup process	Normal decode process. Setup Process
		Line-264 + [VBIL4:VBIL0] - Line-525	Normal decode process. Setup Process	←	←	←

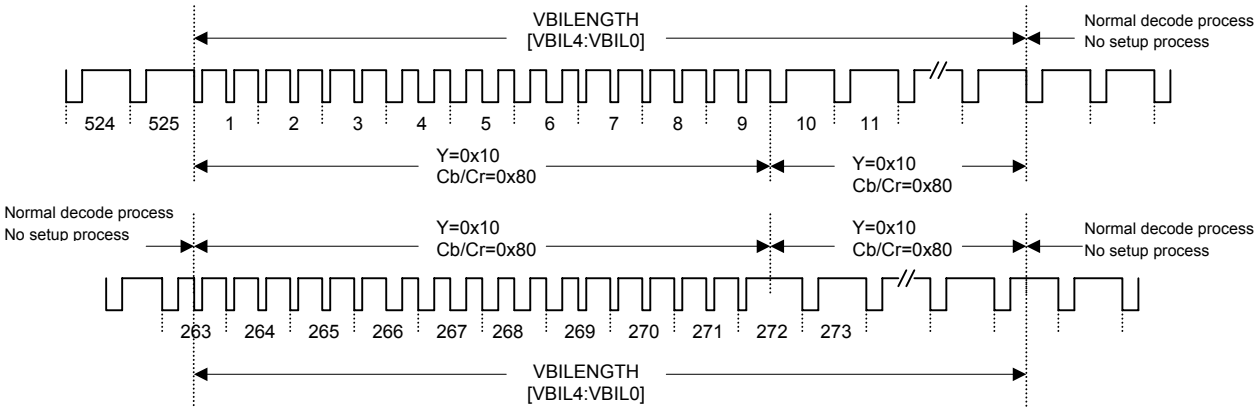
(1) VBIDEC-bit = 0 / HALFSU-bit = 0 / SETUP-bit = 0



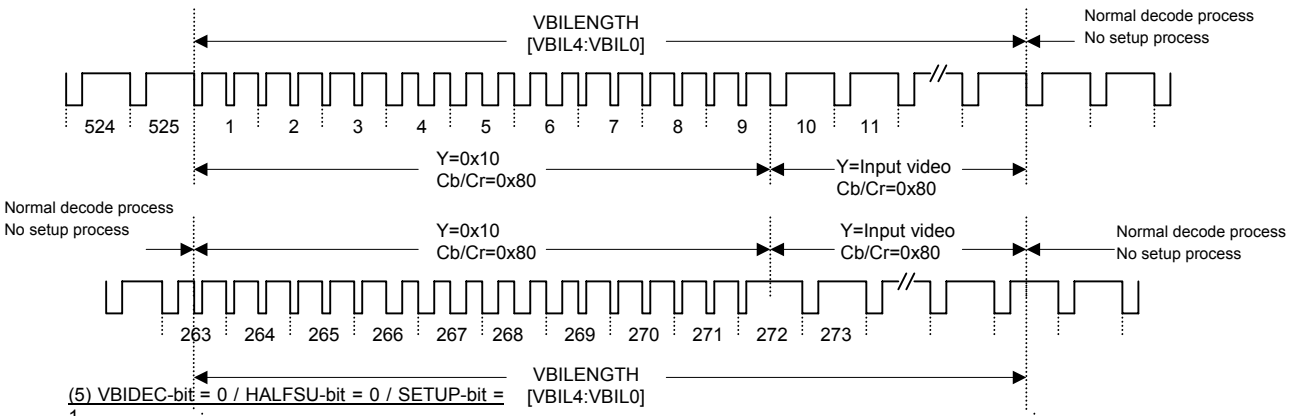
(2) VBIDEC-bit = 1 / HALFSU-bit = 0 / SETUP-bit = 0



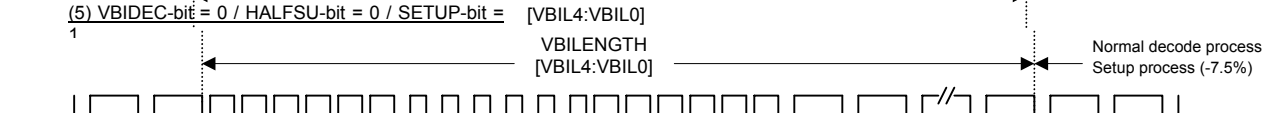
(3) VBIDEC-bit = 0 / HALFSU-bit = 1 / SETUP-bit = 0 (VBIDEC-bit = 0 / HALFSU-bit = 0 / SETUP-bit = 0)



(4) VBIDEC-bit = 1 / HALFSU-bit = 1 / SETUP-bit = 0 (VBIDEC-bit = 1 / HALFSU-bit = 0 / SETUP-bit = 0 □□□)



(5) VBIDEC-bit = 0 / HALFSU-bit = 0 / SETUP-bit = 1



Y=Input video
Cb/Cr=0x80

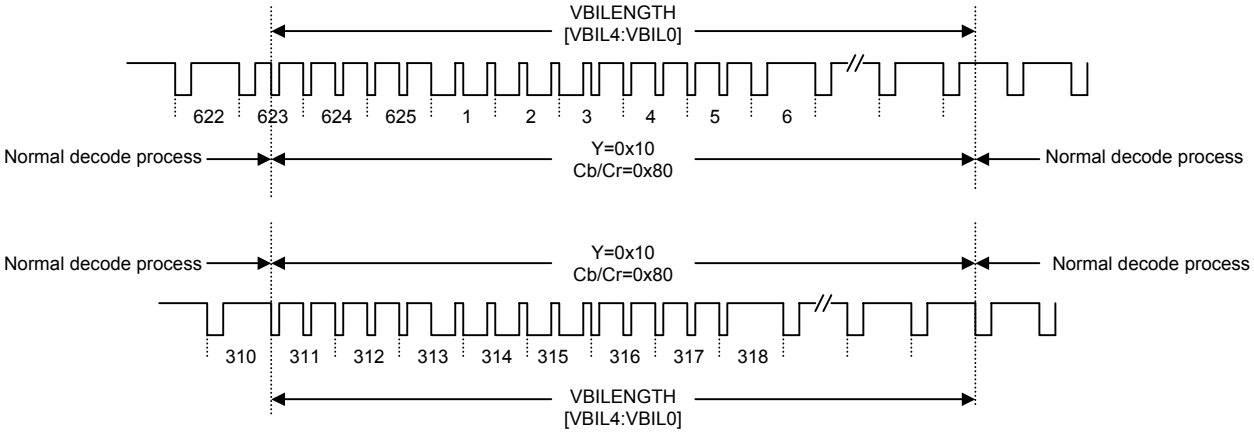
Y=Input video
Cb/Cr=0x80

* 625 system

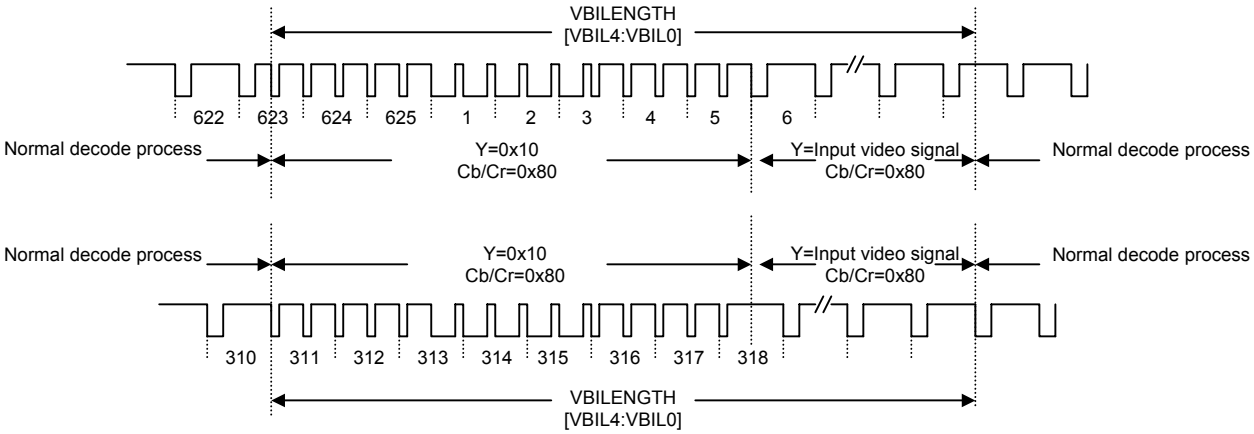
	VBIDEC-bit = 0	VBIDEC-bit = 1

□1□□□□□	Line-623.5 (from 429th pixel of Line-623) - Line-5	Y = 0x10 C = 0x80	←
	Line-6 - [VBIL4:VBIL0]-1.5 (till 429th pixel of Line-([VBIL4:VBIL0] - 2))	Y = 0x10 C = 0x80	Y = Input video signal C = 0x80
	[VBIL4:VBIL0] - 1.5 (from 430th pixel of Line-([VBIL4□ VBIL0] - 2) - Line-310	Normal decode process	←
□2□□□□□	Line-311 - Line-318.5 (till 429th pixel of Line-318)	Y = 0x10 C = 0x80	←
	Line-318.5 (from 430th pixel of Line-318) - 311 + [VBIL4:VBIL0] - 1	Y = 0x10 C = 0x80	Y = Input video signal C = 0x80
	311 + [VBI4:VBIL0] - Line-623.5 (till 429th pixel of Line-623)	Normal decode process	←

(1) output code at VBIDEC-bit = 0



(2) output code at VBIDEC-bit = 1



7-4-11 CLOSED CAPTION/CLOSED CAPTION EXTENDED DATA/VBID (CGMS)/WSS
It is possible to request decoding of Closed Caption, Closed Caption Extended Data, VBID and WSS signals by programming the [REQUEST VBI INFORMATION REGISTER].
The [STATUS 2 REGISTER] tells a host that data is detected and idecoding has been completed for a given decode request.
Decoded data are written into the [CLOSED CAPTION 1.2 REGISTER], [VBID 1.2 REGISTER], [WSS 1 REGISTER] and [WSS 2 & ASPECT DATA REGISTER] respectively.
The Closed Caption Data, Closed Caption Extended Data, VBID and WSS Data are encoded on each specified line respectively as listed below.

Closed Caption : NTSC specified line 21st Line

Closed Caption Extended Data : NTSC specified line 284th Line

VBID (CGMS Data) : 525 system specified line 20th Line / 238th Line

625 system specified line 20th Line / 338th Line

WSS (625 system only) : 625 system specified line 23rd Line

VBI Information Request Register :

* [REQUEST VBI INFO REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ	ASPECTRQ
Default Value							
0	0	0	0	0	0	0	0

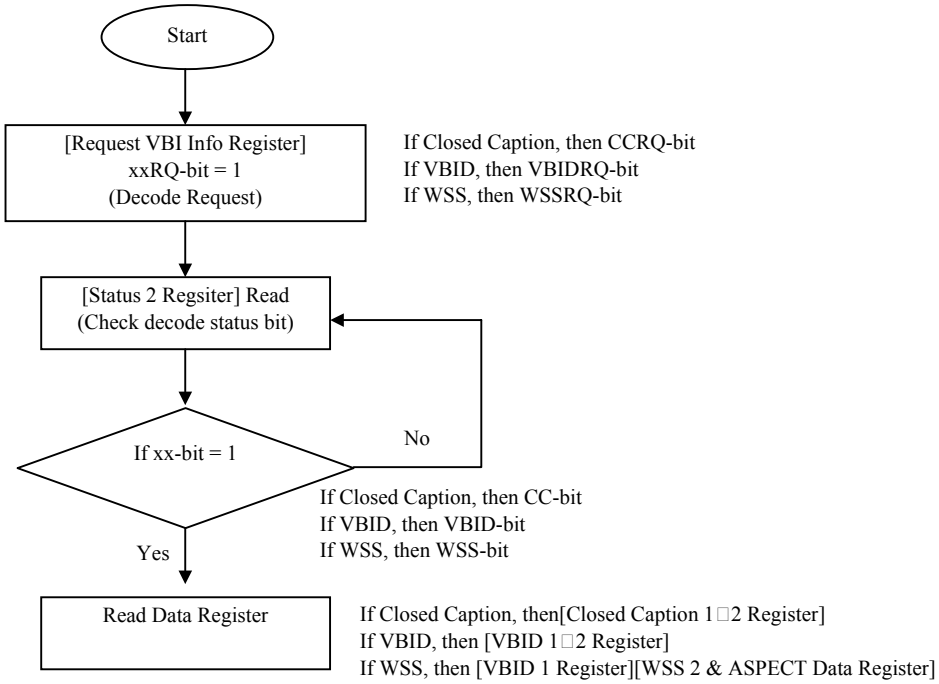
* [STATUS 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
APS1	APS0	Reserved	WSS	VBID	EXT	CC	ASPECT

* Read –out Line Number of the VBI information for each mode is as follows.

	NTSC(525 System)				625 System
	Composite	Y/C	Component		Component
			Betacam	MII	
Closed Caption	Line 21				Line 22
Extended Data	Line 284				Line 335
VBID	Line 20/Line 283				Line 20/Line 333
WSS	□□				Line 23

A procedure to read out each data is described here.



READ OPERATION OF CLOSED CAPTION DATA :
To read closed-caption data, write “1” to the CCRQ-bit. The AK8850 will enter a wait state for the Closed Caption data decoding. Upon receipt of the data, it is decoded and when decoding is completed, ”1” is sent back to CC-bit of the [STATUS 2 REGISTER].
The CC-bit is usually at “1” right after a reset (it becomes “0” by writing “1” at CCRQ-bit).
The decoded data is written into the [CLOSED CAPTION 1.2 REGISTER] as shown. Data in the [CLOSED CAPTION 1.2 REGISTER] is remains in this register until it is over-written.

* [CLOSED CAPTION 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

* [CLOSED CAPTION 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

READ OPERATION OF CLOSED CAPTION EXTENDED DATA :
Write “1” at EXTRQ-bit, which places the AK8850 into a wait state while Extended Data decoding occurs. The received data is decoded and after the decoding is completed,”1” is sent back to EXT-bit of the [STATUS 2 REGISTER]. EXT-bit is usually at “1” right after the reset (it becomes “0” by writing “1” at EXTRQ-bit).
Then the decoded data is written into the [EXTENDED DATA 1.2 REGISTER] as shown. Data in the [EXTENDED DATA 1.2 REGISTER] remains in this register it is over-written.

* [EXTENDED DATA 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

* [EXTENDED DATA 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

READ OPERATION OF VBID DATA

To read the VBID data, write “1” to the VBIDRQ-bit. The AK8850 is put into a wait state while VBID data decodes. Received WSS data is decodecd and after the decoding is complete, ”1” is sent back to VBID-bit of the [STATUS 2 REGISTER]. The VBID-bit is usually at “1” after a reset (it becomes “0” by writing “1” at VBIDRQ-bit).
The decoded 13-bit data is then written into the [VBID 1.2 REGISTER] as shown.
Data in the [VBID 1.2 REGISTER] is remains until it is over-written.

* [VBID 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

* [VBID 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

READ OPERATION OF WSS DATA

To read WSS data, write “1” to the WSSRQ-bit, The AK8850 is placed into a wait state while the WSS data decodes. Received WSS data is decoded and after the decoding is complete, ”1” is sent back to WSS-bit of the [STATUS 2 REGISTER].WSS-bit is usually at “1” right after the reset (it becomes “0” by writing “1” at WSSRQ-bit).
Then the decoded data is written into the [WSS 1 REGISTER] and [WSS 2 & ASPECT DATA REGISTER] as shown.
Data in the [WSS 1 REGISTER] and [WSS 2 & ASPECT DATA REGISTER] is remains until it is over-written.

* [WSS 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

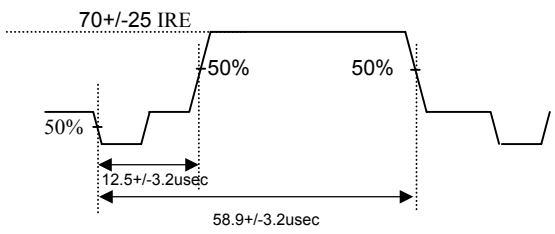
* [WSS 2 & ASPECT DATA REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ASPECT	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

7-4-12 VIDEO ASPECT SIGNAL

This command detects the Video Aspect signal (refer to the following diagram) that is superimposed on Line 16 and Line 279 of the Composite signal. The Aspect signal detection is performed by making a decode request which is set by the [REQUEST VBI INFO REGISTER].
After the decoding is completed, a decode complete notification is generated. The decode data is written into the Aspect-bit of the [WSS 2 & ASPECT DATA REGISTER].Aspect-bit data remains until it is over-written.

Video Aspect Signal Outline
Input signal : Composite signal only (at NTSC / YC input only)
Line : 16th Line and 279th Line
Level : 70 +/- 25 IRE
Rising Edge Point : 12.5 +/- 3.2 microsec from HSYNC rising edge (at 50 % point)
Falling Edge Point : 58.9 +/- 3.2 microsec from HSYNC falling edge (at 50 % point)
Aspect Bit : Wide at “1”
Normal at “0”



Video Aspect Related Registers :

* [REQUEST VBI INFO REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	
Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ	ASPECTRQ
Default Value							
0	0	0	0	0	0	0	0

* [STATUS 2 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
APS1	APS0	Reserved	WSS	VBID	EXT	CC	ASPECT

A decoding request of the Video Aspect signal, superimposed on the input signal is done by writing “1” to the ASPECTRQ-bit of the [REQUEST VBI INFO REGISTER]. The AK8850 is put into a wait state for data decoding. A decode complete signal is sent back to the [STATUS 2 REGISTER]. The decoded data is written into the [WSS 2 & ASPECT DATA REGISTER].

* [WSS 2 & ASPECT DATA REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ASPECT	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

Aspect-bit =0 : Normal signal
Aspect-bit =1 : Wide signal

A Video Aspect decode request signal should be made only when NTSC Composite or Y/C signals are input. If a decoding request is made with the 525 Component input, decoding is actually done as in the Composite signal input case. In this case no Video Aspect signal exists in the signal and resulting data is meaningless.
If a decoding request is made with the 625 Component input, it is ignored and the request bit is kept at “1”).

7-4-14 DIGITAL PIXEL INTERPOLATOR

A digital Pixel Interpolator is equipped in order to align Pixels in the Vertical direction. ON / OFF / AUTO modes of the interpolator is selectable by the [CONTROL 1 REGISTER] setting. If the Auto mode is selected, the ON / OFF state of the interpolator is automatically set by the clock mode used as follows.

Line-locked mode : OFF
Frame-locked mode : ON
External clock mode : ON

Pixel Interpolator Related Registers :

* [CONTROL 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FRCSYNC	Reserved	INTPOL1	INTPOL0	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
1	0	0	0	0	0	0	0

* INTOL1 : INTOL0-bit set

INTPOL1:INTPOL0	Pixel Interpolator
00	Auto
01	ON
10	OFF
11	Reserved

In Auto mode, ON / OFF states of the interpolator are selected by the clock mode used. The interpolator mode selection is not affected by the types of input signals (same for 525 line and 625 line systems).

7-4-15 NON-SIGNAL INPUT DETECTION

The AK8850 detects non-signal input conditions and, when detected, outputs a Black level signal (Y=0x10,Cb/Cr=0x80). The non-signal input condition is detected by checking for the existence of the VSYNC signal. In order to have higher margin against non-Standard signal inputs, the non-signal detection is made only when the VSYNC is not detected two or more consecutive times. The result is output via the NSIG output pin.

Output State: NSIG=1 (non-signal input)
NSIG=0 (valid input signal)

7-4-16 STANDARD SIGNAL DETECTION

The AK8850 has a Standard Signal Detection function. When a non-Standard input signal is detected, the NSTD output pin changes to " high ". The NSTD output becomes " low " (Standard signal input) when either (a) or (b) conditions below are met.

(a) with Component input (525 / 625), the Frame configuration during the past 2 Frames is made with ODD / EVEN or EVEN / ODD sequence.

(b) with Composite input (including Y/C input), the SCH phase is within +/- 67.5 degrees and the Frame configuration is made with ODD / EVEN or EVEN / ODD sequence.

7-4-17 OUTPUT FORMAT (601 FORMATTER)

The AK8850 outputs the decoded data in ITU-R BT.601 compatible format (Y/Cb/Cr 4:2:2). The min. and max. values of the output code are selectable by 601LIMIT-bit of the [OUTPUT FORMAT REGISTER].

At 601LIMIT-bit = 0 Y : 1 ~ 254
Cb/Cr : 1 ~ 254

At 601LIMIT-bit = 1 Y : 16 ~ 235
Cb / Cr : 16~ 240

Output Format Related Register :

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACTSTA[2]	ACTSTA[1]	ACTSTA[0]	YCDELAY[2]	YCDELAY[1]	YCDELAY[0]	601LIMIT	ERRHND
Default Value							
0	0	0	0	0	0	0	0

7-4-18 SETUP

Enabling and Disabling SETUP is selected by the [INPUT VIDEO STANDARD REGISTER]. When the SETUP-bit is "1", internal signal processing is performed, assuming that the SETUP signal is input. This signal is processed outside of the VBI period. The VBI period is set by the [VERTICAL BLANKING LENGTH REGISTER].

Signal Set Register with SETUP Features :

When the input signal contains a SETUP command, set [SETUP]-bit of the [INPUT VIDEO STANDARD REGISTER] to "1".

* Input Video Standard Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	NENT	B/W	SETUP	VS3	VS2	VS1	VS0
Default Value							
0	0	0	0	0	0	0	0

* SETUP-bit Set

SETUP-bit	Setup	Note
0	without Setup	
1	with Setup	Setup process should be done exclusive the term of VBI interval.

Setting is not affected by input signal types (Composite, YC and Component signals).

When the SETUP-bit is set at "1", the following conversion is performed on input signal.

On 286 mV SYNC system signals (NTSC Composite, YC signal, Betacam signal) with SETUP,

Luminance signal (Y) : Y = (Y- 42) / 0.925 ;

Chroma signal (U / V) : Pb = Pb / 0.925 ;

Pr = Pr / 0.925 ;

On 300 mV SYNC systems (MII signal) with SETUP ,

Luminance signal (Y) : Y = (Y-41) / 0.925 ;

Chroma signal (U / V) : Pb = Pb / 0.925 ;

Pr = Pr / 0.925 ;

7-4-19 TIMING OUTPUT

The AK8850 outputs the signals listed below. Output logical states can be altered by the [OUTPUT CONTROL REGISTER]. The state shown is the default value (refer to the Output Timing Diagram).
Either the VSYNC or VD signals can be output on the VSYNC output pin per the register setting. Output timing of the Field signal and the Frame signal can be delayed by 0.5 H time using the FFDELAY-bit of the [OUTPUT CONTROL REGISTER]. CSYNC signals can be output via the FRAME1 pin by setting the FRCSYNC-bit of the [CONTROL 1 REGISTER] bit-7.

FFDELAY-bit	Function
0	FIELD/FRAME timing signal changes at the falling edge of HSYNC of proper line.
1	FIELD/FRAME timing signal chages at the raising edge of serration pulse of proper line.

FRCSYNC-bit	Function
0	Frame timing signal is output from FRAME1pin
1	CSYNC timing signal is output from FRAME1pin

At 525-Line-System input (output state at default value)

HSYNC : " low " level signal of 4.7 microsec. Duration in 15.734 KHz interval
VSYNC : " low " output signal during Line 4 ~ Line 6 / Line 266.5 ~ Line 269.5
(Line 266.5 means from the latter 0.5 H time of Line 266,and Line 269.5 means up to the former 0.5 H time of Line 269).
VD : " low " output signal during Line1 ~ Line 9 / Line263.5 ~ Line 272.5
(Line 263.5 means from the latter 0.5 H time of Line 263, and Line 272.5 means up to the former 0.5 H time of Line 272).
FIELD : Output signal to become " low " at Odd Fields, and " high " at Even Fields.
FRAME : Color Frame

For non-Standard signal inputs, Field signal toggles at the rate of (Line numbers per each Frame / 2).
Frame signal changes at the rate of Line numbers per each Frame (Frame signal changes state at Line 4).

CSYNC : Composite Sync signal.CSYNC output does not change state.

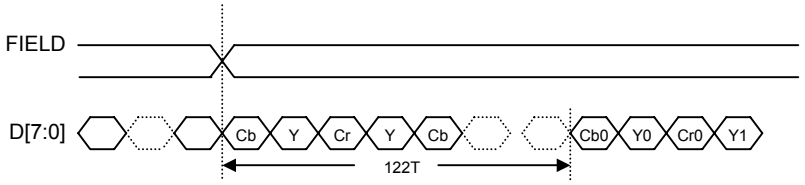
At 625-Line-System input (output state at default value)

HSYNC : " low " level signal of 4.7 microsec. duration in 15.734 KHz interval
VSYNC : " low " output signal during Line 1 ~ Line 3.5 / Line 313.5 ~ Line 315
(Line 3.5 means up to the former 0.5 H time of Line 3,and Line 313.5 means from the latter 0.5 time of Line 313).
VD : " low " output signal during Line 623.5 ~ Line 5 / Line 311 ~ Line 318.5.
(Line 632.5 means from the the latter 0.5 H time of Line 623, and Line 318.5 means up to the former 0.5 H time of Line 318).
FIELD : Output signal to become " low " on Odd Fields, and " high " on Even Fields.
FRAME : Color Frame

For non-Standard signal inputs, Field signal toggles at the rate of (Line numbers per each FRAME / 2).
Frame signal changes state at the rate of Line numbers per each Frame (Frame signal changes state at Line 1).

CSYNC : Composite Sync signal. CSYNC output does not change state

Data at both rising edge and falling edge of the FIELD signal is Cb data. The FIELD signal and data relationship of Standard signal inputs is as follows.



* [OUTPUT CONTROL REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDVSYNC	FFDELAY	HALFCLK	FRAME	DVALVLK	FEILD	VSYNC	HSYNC
Default Value							
0	0	0	1	0	1	0	0

Logical state can be altered by these registers. Default value is " 0 " as shown in the timing diagram.

* [CONTROL 1 REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FRCSYNC	DECIMAT	INTPOL1	INTPOL0	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
1	0	0	0	0	0	0	0

FRCSYNC-bit controls output on FRAME 1 pin.

7-4-20 VLOCK FUNCTION

The AK8850 synchronizes its internal operation with the input signal's FRAME configuration. For example, if the input signal Frame configuration consists of 525 lines, the internal operation uses the 525 Line configuration. This is called the VLOCK configuration.

When the input signal configured with 525 Line per Frame is switched to 524 Lines, the operation tracks to the switched input signal system.

In this case VLOCK function is put into un-locked state during the tracking time. The un-locked state is verified by the [STATUS 1 REGISTER].

VLOCK status is observed on the DVALID pin by setting the DVAL / VLK-bit of the [OUTPUT CONTROL REGISTER] (R / W) [SUB ADDRESS 0x05].

VLOCK Status	Status 1 Register VLOCK-bit	VLOCK output pin
Locked (synchronaize with Input video signal)	1	High
UnLocked□Un-synchronaized with input video signal□	0	Low

The transition timing of the VLOCK output pin changes with VLOCK configuration conditions. .

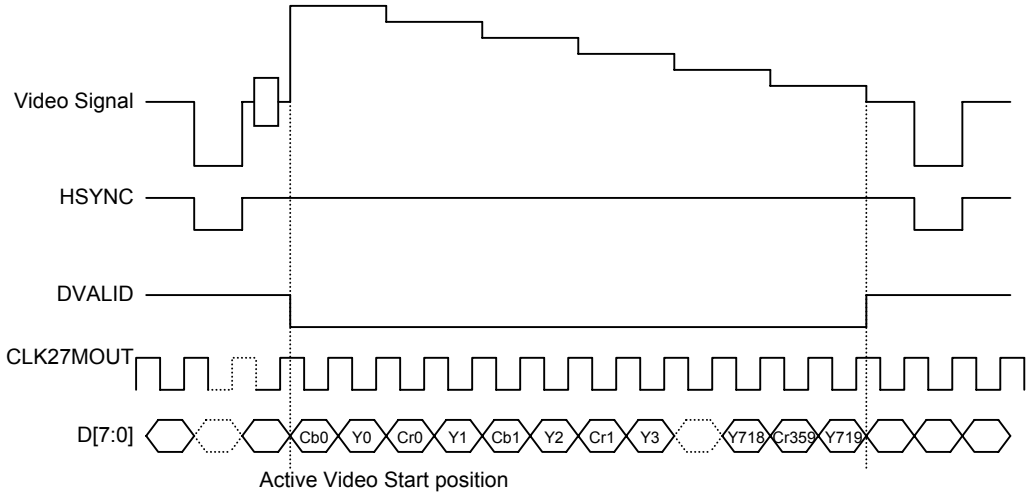
7-4-21 OUTPUT INTERFACE

The AK8850 outputs decoded data in ITU-R BT.656 compatible interface formats, i.e.,
The sample number for each Line is guaranteed to be 858 / 864 (525 system / 625 system) respectively.
Poor input quality or non Line-locked/Frame-locked PLL clocks may prevent ITU-R BT.656 compatible output. , In these cases, the Input signal and Output data are correlated by the following 2 methods, selected by the [OUTPUT FORMAT REGISTER].

(1) Adjust using a Line-Drop / Repeat scheme (number of Lines is not equal to 525 / 625, but number of samples is guaranteed to be 858 / 864).
This process is performed when the final stage output buffer of the device either overflows or underflows.

(2) Make 858 / 864 samples to be variable (number of samples is not equal to 858 / 864, but number of Lines is guaranteed to be 525 / 625).
Decoded data becomes ITU-R BT.656 compatible except for the last line of each Frame (Line 3 in 525 system , Line 625 in 625 system).i.e., typical 858 / 864 samples per each line is guaranteed other than at Line 3 / Line 625 (525 system / 625 system).
The number of samples at Line 3 and Line 625 is un-determined since it is decided by relationdhip between the input signal rate and the PLL-generated clock rate (it hovers around 858 / 864 samples). In this processing mode, there is less of a chance for buffer overflow or underflow since the buffer pointer is moved to the mid point of the buffer at the last line. When either overflow or underflow occurs at the final stage buffer, a Line Drop / Repeat function is processed (which can occur when the input signal rate differs much from the PLL-generated clock rate).

The DVALID pin output is “ low “ during the Active-Video period of the output data.
Relationship between HSYNC, DVALID and output data are shown below.



Fine-tuning the Active-Video start position and a Y / C Delay amount to be output can be accomplished by programming the [OUTPUT FORMAT REGISTER].

Output Interface Set Register :
Output Interface is set by the [OUTPUT FORMAT REGISTER].

* [OUTPUT FORMAT REGISTER]

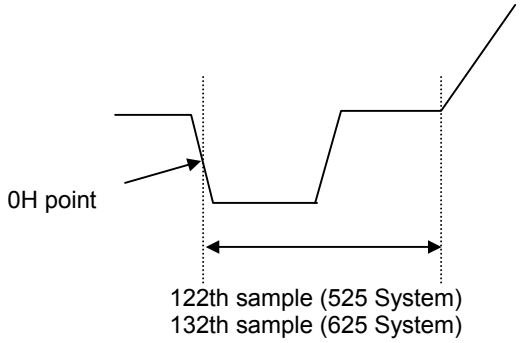
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACTSTA[2]	ACTSTA[1]	ACTSTA[0]	YCDELAY[2]	YCDELAY[1]	YCDELAY[0]	601LIMIT	ERRHND
Default Value							
0	0	0	0	0	0	0	0

[ERRHND]-bit of the [OUTPUT FORMAT REGISTER] controls error handling as follows.

* ERRHND-bit

ERRHND-bit	□□□□	□□
0	Number of sample is constant	525 System : 858 samples 625 System : 864 samples
1	Number of line in a frame is constant	525 System : 525Line 625 System : 625Line

Fine-tuning of the start position is accomplished by programming the ACTSTA [2 :0]-bit.



* ACTSTA [2 : 0]-bit set

ACTSTA2:ACTSTA0	Function	Note
100	525system : Active Video starts at the 119th sample 625system : Active Video starts at the 129th sample	
101	525system : Active Video starts at the 120th sample 625system : Active Video starts at the 130th sample	
110	525system : Active Video starts at the 121th sample 625system : Active Video starts at the 131th sample	
111	525system : Active Video starts at the 122th sample 625system : Active Video starts at the 132th sample	
000	525system : Active Video starts at the 123th sample 625system : Active Video starts at the 133th sample	default
001	525system : Active Video starts at the 124th sample 625system : Active Video starts at the 134th sample	
010	525system : Active Video starts at the 125th sample 625system : Active Video starts at the 135th sample	
011	525system : Active Video starts at the 126th sample 625system : Active Video starts at the 136th sample	

a fine-tuning of the YC output timing is possible by setting YC delay [2 : 0]-bit of the [OUTPUT FORMAT REGISTER].The YC delay fine-tuning bit is set in 2's complement values.

ACTSTA2:ACTSTA0	Function	Note
100	Y data is delayed 4samples (296nsec) agaist C-data	
101	Y data is delayed 3samples (222nsec) agaist C-data	
110	Y data is delayed 2samples (148nsec) agaist C-data	
111	Y data is delayed 1sample (74nsec) agaist C-data	
000	No delay	Default
001	C data is delayed 1sample (74nsec) agaist Y-data	
010	C data is delayed 2samples (148nsec) agaist Y-data	
011	C data is delayed 3samples (222nsec) agaist Y-data	

7-4-22 POWER SAVE MODE

The AK8850 is placed in Power Save mode by setting the PS-bit of the [POWER SAVE MODE REGISTER] to " 1 ". Exiting Power Save mode is done by setting the PS-bit to "0". During Power Save mode, the I2C bus controller, clock output driver and VREF generating circuit are active, the PLL block is initialized and PLL DAC local code becomes 0x80. After exiting Power Save mode, the device re-starts operation from the state which is set via the I2C bus.
All circuits are put into Sleep mode when the Power Down pin (PD) is set to high.
The IVCXO output current is zero micro Amps in this state. To re-start the AK8850, an input reset and initialization are required after setting PD pin from high to low. Operation is stabilized in a few milliseconds.
Please follow the Power Down set sequence for proper setting.

Power Save Mode Related Register :
Power Save related registers are programmed by the [POWER SAVE MODE REGISTER].

* [POWER SAVE MODE REGISTER]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	PLLRST	ADC3	ADC2	ADC1	PS
Default Value							
0	0	0	0	0	0	0	0

* PS-bit set

PS-bit	Function	Note
0	Normal function	
1	Stops the clock supply to the Internal digital Block, exclusive control block.. Stops ADC1/2/3. Resets the PLL control circuit.	

* ADC1 / 2 / 3-bit set

ADC1/2/3-bit	Function	Note
0	ADC1/2/3 Active mode	
1	ADC1/2/3 sleep mode	Each ADC can be set to sleep mode individually.

7-4-23 DEVICE CONTROL INTERFACE

The AK8850 is controlled via the I2C bus interface.

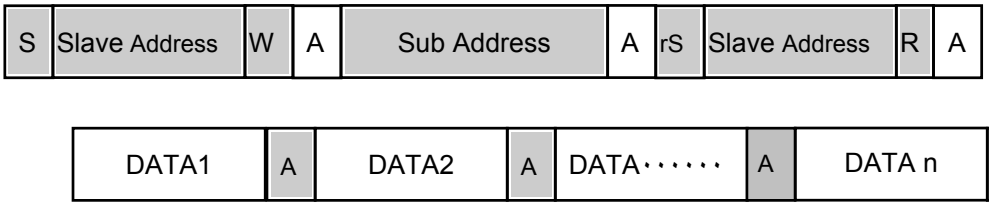
I2C Control Sequence

Slave Address is selected to be either 0x88 or 0x8A by SELA pin set.

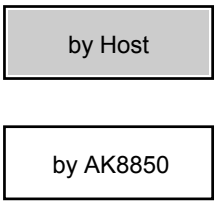
SELA	Pull down(L)	Pull up(H)
Slave Address	0x88	0x8A

Write Sequence:

Sequential Read:



S,(rS) : Start Condition
A : Acknowledge (SDA LOW)
$\overline{A}$: Not Acknowledge (SDA HIGH)
Stp : Stop Condition
R/W 1 : Read 0 : Write



8. REGISTER DEFINITION

The AK8850 has the following registers.

Sub Address	Register	Default	R/W	Function
0x00	Input Video Standard Register	0x00	R/W	Set Input Video Standard
0x01	Input Signal Select Register	0x11	R/W	Select Input Video signal
0x02	Vertical Blanking Length Register	0x14	R/W	Set VBI Interval
0x05	Output Control Register	0x14	R/W	Set the attribution of output data
0x06	Output Format Register	0x00	R/W	Set the output I/F
0x08	Control-1 Register	0x80	R/W	Control Register
0x09	Control-2 Register	0xC1	R/W	Control Register
0x0A	Clamp Control Register	0x00	R/W	Set the clamp function setting
0x0B	Clamp Timing Control Register	0x11	R/W	Set the clamp pulse timing
0x0C	Clamp Timing 2 Control Register	0x1C		Set the clamp pulse timing
0x0D	PGA1 Gain Control Register	0x40	R/W	Set the manual Gain of PGA1
0x0E	PGA2 Gain Control Register	0x40	R/W	Set the manual Gain of PGA2
0x0F	PGA3 Gain Control Register	0x40	R/W	Set the manual Gain of PGA3
0x10	Y/C Separation Control Register	0x06	R/W	Set the YC Separation function
0x11	Color Killer Control Register	0xAD	R/W	Color killer setting
0x12	Brightness Control Register	0x00	R/W	Set Brightness adjustment
0x13	Contrast Control Register	0x80	R/W	Set Contrast adjustment
0x14	Saturation Control Register	0x80	R/W	Set Saturation adjustment
0x15	HUE Control Register	0x00	R/W	Set HUE adjustment
0x1C	Power Save Register	0x00	R/W	Power Save setting
0x1F	Request VBI Info Register	0x00	W	VBIDdata decode requet
0x20	Status 1 Register	0x00	R	Internal status of AK8850
0x21	Status 2 Register	0x00	R	nternal status of AK8850
0x22	Closed Caption1 Register	0x00	R	Closed Caption data
0x23	Closed Caption2 Register	0x00	R	Closed Caption data
0x24	Extended Data 1 Register	0x00	R	Closed Caption Extended data
0x25	Extended Data 2 Register	0x00	R	Closed Caption Extended data
0x26	VBID1 Register	0x00	R	VBID data
0x27	VBID2 Register	0x00	R	VBID data
0x28	WSS1 Register	0x00	R	WSS data
0x29	WSS2 & Aspect Data Register	0x00	R	WSS data and video aspect data.
0x2E	Device/Revision ID Register	0x00	R	Device ID / Revision ID
0x36	Clock Control-1 Register	0x84	R/W	Clock transition control register.
0x37	Clock Control-2 Register	0x7C	R/W	Clock transition control register.
0x38	Clock Control-3 Register	0x3C	R/W	Clock transition control register.
0x39	Clock Control-4 Register	0xDC	R/W	Clock transition control register.
0x3A	Clock Control-5 Register	0x04	R/W	Clock transition control register.
0x46	PLL Control Register	0x00	R/W	PLL Control Register
0x47	PLL DAC Set Register	0x80	R/W	PLL_DAC Setting register

INPUT VIDEO STANDARD REGISTER (R / W)[SUB ADDRESS 0x00]

This register sets the input video signal Standard. Automatic setup recognition is not available.
Reserved Bits must be set to " 0 ".

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	NENT	B/W	SETUP	VS3	VS2	VS1	VS0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register Definition

BIT	Register Name		R/W	
bit 0 ~ bit 3	VS0 ~ VS3	Video Standard bit	R/W	Set the input video standard VS3□VS0 0000 : NTSC/ 525Component 1111 : 625Component AK8850 can deal with only component signal for 625- video ssytems. Other settings are reserved.
bit 4	SETUP	Setup bit	R/W	0 : without Setup [Default] 1 : with Setup
bit 5	B/W	Black & White bit	R/W	B/W video signal setting 0 : Color video signal is input [Default] 1 : B/W video signal is input
bit 6	NENT	Component Video Sel bit	R/W	Set the Component Video Signal 0 : MII Level Component Video signal [Default] 1 : BETACAM Level component video signal
bit 7	Reserved	Reserved bit	R/W	Reserved bit

Setting Component input is done as follows.

1. Component input is selected via the input signal select register.
2. Selection of MII or Betacam is done by the Input Video Standard Register NENT-bit.
3. Set either 525- or 625 line systems.

INPUT SIGNAL SELECT REGISTER (R / W) [SUB ADDRESS 0x01]

Register to select the input signal.

Sub Address 0x01 **Default Value : 0x11**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SYNCIN1	SYNCIN0	INSEL3	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	1	0	0	0	1

Input Select Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	INSEL0 ~ INSEL3	Input Select bit	R/W	Select the Input video signal INSEL3□INSEL0 0000 : No Input 0001 : AIN1 Composite [Default] 0010 : AIN2 Composite 0011 : AIN3 Composite 0110 : AIN2 Y AIN4 C 0111 : AIN3 Y AIN5 C 1011 : AIN3 Y AIN5 U AIN6 V
bit 4 ~ bit 5	SYNCIN0 □ SYNCIN1	SYNCIN Select bit	R/W	Select the video signal for the Clamp timing generator. SYNC1: SYNC0 00 : No Input 01 : SYNC1 timing [Default] 10 : SYNC2 timing 11 : SYNC3 tiimng
bit 6 □ bit 7	Reserved	Reserved bit	R/W	Reserved bit

Supplement□bit3 - bit0 bit3=1: component , bit2=1: Y/C Video input

VERTICAL BLANKING LENGTH REGISTER (R / W) [SUB ADDRESS 0x02]

Register to set VBI interval.

Sub Address 0x02 **Default Value : 0x14**

bit 7	bit 6	bit 5	bit 4		bit 2	bit 1	bit 0
VBIDEC	TRSVSEL	HALFSU	VBIL4	VBIL3	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	1	0	1	0	0

Vertical Blanking Register Definition

BIT	Register Name		R/W	Definition
bit 0 - bit 4	VBIL4 □ VBIL0	Vertical blanking Information Length bit	R/W	Set the VBI interval Default value is 20 (decimal) i.e., Active video starts from Line-21 The value of VBI[4:0] must be set more than 10.
bit 5	HALFSU	Half Setup bit	R/W	Set the setup function for the first active line of the 2nd field. 0 : 0.5H of 2nd field is not made setup process. 1 : 0.5H of 2nd field is made setup process.
bit 6	TRSVSEL	Time Reference Signal V Select bit	R/W	Set the V-bit transition timing for EAV/SAV. NTSC, 525 Component TRSVSEL = 0 : Line 1-9 / Line264-Line272 : V=1 Other V=0 TRSVSEL = 1: Line 1-19 / Line 264-Line282 V=1 Other V=0 625 Sytem : V-bit setting should reflect TRSVSEL-bit setting
bit 7	VBIDEC	VBI Decode bit	R/W	Output data while the VBI Interval. 0 : Y = 0x10 C = 0x80 1 : Y = input data(same as B/W process) C = 0x80

For details, please refer to section 7-4-10 VERTICAL BLANKING INTERVAL.

OUTPUT CONTROL REGISTER (R / W) [SUB ADDRESS 0x05]

Thie register sets the external output signal attributes like HSYNC, VSYNC, FIELD, DVALID and FRAME etc. Timing of output signals can be altered by CLKOUT-bit set.

Sub Address 0x05 **Default Value : 0x14**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDVSYNC	FFDELAY	HALFCLK	FRAME	DVALVLK	FIELD	VSYNC	HSYNC
Default Value							
0	0	0	1	0	1	0	0

Output Control Register Definition

BIT	Register Name		R/W	
bit 0	HSYNC	HSYNC-Logic bit	R/W	0 : Low [default] 1 : High
bit 1	VSYNC	VSYNC-Logic bit	R/W	0 : Low[default] 1 : High
bit 2	FIELD	FIELD-Logic bit	R/W	0 : ODD FIELD : Low 1 : ODD FIELD : High [default]
bit 3	DVAL/VLK	DVALID VLock Switch- bit	R/W	0 : DVALID signal output [default] 1 : VLOCK status output
bit 4	FRAME	FRAME-Logic bit	R/W	0 : Low at CF = 0 1 : High at CF = 0[default]
bit 5	HALFCLK	HALFCLK-bit	R/W	0 : Low at Y-data ouput timing [Default] 1 : Hight at Y-data output
bit 6	FFDELAY	Field Frame Delay bit	R/W	Field timing signal and Frame timing signal can be output 0.5H delayed with this bit. 0 : No Delay [default] 1 : 0.5H Delay
bit 7	VDVSYNC	VD/VSYNC Select bit	R/W	0 : Output VSYNC Pulse [default] 1 : Ouput VD pulse. (Refer to the Figure “Output timing Signal”)

FIELD and FRAME signals are correct values only when the Standard signal is input. (in case of Non-Standard signal input, FIELD and FRAME signals are not necessarily correct ones .For handling of Non-Standard signal input,refer to item 7-4-21).

OUTPUT FORMAT REGISTER (W / R) [SUB ADDRESS 0x06]

Register to set output format.

Sub Address 0x06 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2		bit 0
ACTSTA2	ACTSTA1	ACTSTA0	YCDELAY2	YCDELAY1	YCDELAY0	601LIMIT	ERRHND
Default Value							
0	0	0	0	0	0	0	0

Output Format Register Definition

BIT	Register Name		R/W	Definition
bit 0	ERRHND	Error Handling bit	R/W	Setting the data handling procedure when AK8850 cannot output the data follow to ITU-R. Bt.656. Error handling normally occurs within the last lines of the Frame. 0 : Line Drop/Repeat 1 : Number of Smaples of the line is change.
bit 1	601LIMIT	601 Output Limit bit	R/W	Min/Max value of the output data 0 : 1~254 (Y/Cb/Cr) [Default] 1 : 16~235 (Y) 16~240 (Cb/Cr)
bit 2 ~ bit 4	YCDELAY0 - YCDELAY2	Y/C Delay Control bit	R/W	Y/C delay setting for output data. One delay time is 74nsec(1clock@13.5MHz) Set the value with 2's complement [YCDELAY2-YCDELAY0]= 101 : Y-data is 3clocks delay against C-data 110 : Y-data is 2clocks delay against C-data 111 : Y-data is 1clock delay against C-data 000 : No delay [Default] 001 : C-data is 1clock delay against Y-data 010 : C-data is 2clocks delay against Y-data 011 : C-data is 3clocks delay against Y-data
bit 5 ~ bit 7	ACTSTA0 - ACTSTA2	Active Video Start Control bit	R/W	Set fine adjustment of Start position of decoded video data. Set the value with 2's complement [ACTSTA2:ACTSTA0]= 101 : Decoding the video data 3pixels earlier. 110 : Decoding the video data 2pixels earlier. 111 : Decoding the video data 1pixel earlier. 000 : Normal position [Default] 001 : Decoding the video data 1pixel delayed. 010 : Decoding the video data 2pixels delayed. 011 : Decoding the video data 3pixels delayed.

CONTROL 1 REGISTER / CONTROL 2 REGISTER

These registers control the AK8850 operations.
There are 2 registers, CONTROL 1 and CONTROL 2. Reserved bits must be set to " 0 ".

Control 1 Register (R/W) [Sub Address 0x08]

Sub Address 0x08 Default Value : 0x80

bit 7	bit 6	bit 5	bit 4		bit 2	bit 1	bit 0
FRCSYNC	Reserved	INTPOL1	INTPOL0	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
1	0	0	0	0	0	0	0

Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	AGCT0 ~ AGCT1	AGC Time Constant Control bits	R/W	Set the AGC time constant. When the AGC is Disabled, each PGA can be set manually. [AGCT1□AGCT0] = 00 : Disable [default] 01 : Fast [T = 1Field] 10 : Middle [T = 7Field] 11 : Slow [T = 29Field] (T : Time constance)
bit 2 ~ bit 3	AGCC0 ~ AGCC1	AGC Coring Control bits	R/W	Set the non-sensing bandwidth of AGC [AGCC1□AGCC0] = 00 : No non-sensing bandwidth[Default] 01 : 1bit 10 : 2bits 11 : 3bits
bit 4 ~ bit 5	INTPOL0 □ INTPOL1	Interpolator Control bit	R/W	Setting for Pixel Interpolator [INTPOL1□INTPOL0] = 00 : Auto [Default] 01 : ON 10 : OFF 11 : Reserved Setting to Automode, the Interpolator switch turns on/off according to the clock mode as described bellow, Line Lock PLL : OFF Frame Lock PLL: ON Fixed Clock mode: ON
bit 6	Reserved	Reserved	R/W	Reserved
bit 7	FRCSYNC	Frame CSYNC switch bit	R/W	Define the output data from FRAME1pin. 0 : FRAME timing pulse output 1 : CSYNC timing pulse output [default]

Control 2 Register (R/W) [Sub Address 0x09]

Sub Address 0x09 **Default Value : 0xC1**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	ACC1	ACC0	DPCC1	DPCC0	DPCT1	DPCT0
Default Value							
1	1	0	0	0	0	0	1

Control 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	DCPT0 ~ DPCT1	Digital Pedestal Clamp Timing bit	R/W	Setting of TIme constant of the digital pedestal clamp. DPCT1:DPCT0 00 : digital pedestal clamp OFF 01 : Fast [Default] 10 : Middle 11 : Slow
bit 2 ~ bit 3	DPCC0 ~ DPCC1	Digital Pedestal Clamp Coreing bit		Setting the non-sensing bandwidth of digital pedestal clamp. DPCC1 : DPCC0 00 : No non-sensing bandwidth [Default] 01 : 1bit 10 : 2bits 11 : 3bits
bit 4 ~ bit 5	ACC0 ~ ACC1	Auto Color Control bits	R/W	Setting the ACCf function [ACC1□ACC0] = 00 : Disable ACC [Default] 01 : Fast [T = 2-Field] 10 : Middle [T = 8-Field] 11 : Slow [T = 30-Field] (T : Time constance)
bit 6 ~ bit 7	CLKMODE0 ~ CLKMODE1	Clock Mode bits	R/W	Setting Clock mode CLKMODE1: CLKMODE0 = 00 : Fixed clock mode(27MHz) 01 : Line-Locked Clock mode 10 : Frame-Locked Clock mode 11 : Clock mode Auto Select □ mode [Default]

CLAMP CONTROL REGISTER (R / W) [SUB ADDRESS 0x0A]

This register controls clamp-related matters. Reserved bits must be set to " 0 ".

Sub Address 0x0A **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	Bit 3	bit 2	bit 1	bit 0
UNMASK	Reserved	ACLMP	INCLPTMG	FBCLPTMG1	FBCLPTMG0	CLPLVL1	CLPLVL0
Default Value							
0	0	0	0	0	0	0	0

Clamp Control Register

BIT	Register Name		R/W	Definition
bit 0 □ bit 1	CLPLVL0 ~ CLPLVL1	CLAMP Level 0 ~ CLAMP Level1 bit	R/W	Setting analog video clamp. This setting is valid for Clamp 1. The level of Clamp 2/3 is constant at 512 level. CLPLVL1□CLPLVL0 00: 16 [default] 01: 240 10: 252 11: Analog clamp is off
bit 2 □ bit 3	FBCLPTMG0 ~ FBCLPTMG1	Feed Back Clamp Timing bit	R/W	Setting the clamp timing pulse. 00 : Synctip level clamp with the internal clamp timing [default] 01 : Synctip level clamp with the external clamp timing pulse. 10 : Pedestal level clamp with the internal clamp timing pulse. 11 : Pedestal level clamp with the external clamp timing pulse.
bit 4	INCLPTMG	Input Clamp Timing bit		Setting the clamp timing pulse. 0 : Internal Clamp timing pulse [default] 1 : External Clamp timing pulse
bit 5	ACLAMP	Analog Clamp On/Off bit	R/W	Setting the clamp on/off. When a video signal is input through AC coupling capacitor, this set must be set to "0". 0 : ON [default] 1 : OFF (AIN Clamp OFF)
bit 6	Reserved	Reserved bit	R/W	Reserved
bit 7	UNMASK	Clamp Unmask bit	R/W	Clamp mask on/off bit. Normally this bit set to 0. 0 : Masked [default] 1 : Unmasked

CLAMP TIMING 1 CONTROL REGISTER (R / W) [SUB ADDRESS 0x0B]

This register sets SYNC-TIP Clamp timing. Clamp Timing Pulse generation and its pulse width can be adjusted. Output signal mode selection of the EXTCLP pin is also possible. For a timing diagram, refer to the SYNC Separation description in the Clamp section. Reserved bits must be set to " 0 ".

Sub Address 0x0B **Default Value : 0x11**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXTCLP1	EXTCLP0	SCLPWIDTH2	SCLPWIDTH1	SCLPWIDTH0	SCLPSTAT2	SCLPSTAT1	SCLPSTAT0
Default Value							
0	0	0	1	0	0	0	1

Clamp Timing Control Register

BIT	Register Name		R/W	Definition
bit 0 □ bit 2	SCLPSTAT0 □ SCLPSTAT2	Synctip Clamp Start timing0 □ Synctip Clamp Start timing2 bit	R/W	Setting the start position of synctip clamp pulse default value is SCLPSTA2 : SCLPSTA0 = 001 [SCLPSTAT2□SCLPSTAT0] 000 : 2clks later 001 : 4clks later 010 : 6clks later 011 : 8clks later 100 : 10clks later 101 : 12clks later 110 : 14clks later 111 : 16clks later 1clk is about 37[nsec]
bit 3 □ bit 5	SCLPWIDTH0 □ SCLPWIDTH2	Synctip Clamp Pulse Width0 bit □ Synctip Clamp Pulse Width2 bit	R/W	Setting the synctip clamp pulse width Default value is SCLPWIDTH2 : SCLPWIDTH0 = 010. [SCLPWIDTH3□SCLPWIDTH0] 000 : 2 clks (74nsec) 001 : 4 clks (148nsec) 010 : 8 clks (296nsec) 011 : 16 clks (592nsec) 100 : 24 clks (888nsec) 101 : 32 clks (1.18usec) 110 : 40 clks (1.48usec) 111 :48 clks (1.78usec)
bit 6 □ bit 7	EXTCLP0 □ EXTCLP1	External Clamp 0 bit □ External Clamp 1 bit	R/W	Setting the output the timing data from EXTCLP-pin. [EXTCLP1:EXTCLP0] 00 : Hi-Z (Defaul) 01 : Internal synctip clamp timing pulse. 10 : Internal pedestal clamp timing pulse. 11 : SYNCDET signal

CLAMP TIMING 2 CONTROL REGISTER (R / W) [SUB ADDRESS 0x0C]

This register sets the Pedestal Clamp timing.
The timing of the Clamp Timing Pulse generation and its pulse width can be adjusted.
For timing diagram,refer to the SYNC-Separation description in the Clamp section. Reserved bits must be set to " 0 ".

Sub Address 0x0C **Default Value :0x1C**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SLCLV1	SLCLV0	PCLPWIDTH2	PCLPWIDTH1	PCLPWIDTH0	PCLPSTAT2	PCLPSTAT1	PCLPSTAT0
Default Value							
0	0	0	1	1	1	0	0

CLAMP Timing 2 Control Register

BIT			R/W	Definition
bit 0 □ bit 2	PCLPSTAT0 □ PCLPSTAT2	Pedestal Clamp Start timing0 bit □ Pedestal Clamp Start timing2 bit	R/W	Setting the start position of pedestal clamp pulse. default value is PCLPSTA2 : PCLPSTA0 = 100 [PCLPSTAT2□PCLPSTAT0] 000 : 118 clks (4.37usec) later 001 : 126 clks (4.65usec) later 010 : 132 clks (4.88usec) later 011 : 140 clks (5.18usec) later 100 : 148 clks (5.48usec) later 101 : 156 clks (5.77usec) later 110 : 164 clks (6.07usec) later 111 : 172 clks (6.36usec) later 1clk is about 37[nsec]
bit 3 □ bit 5	PCLPWIDTH0 □ PCLPWIDTH3	Pedestal Clamp Pulse Width0 □ Pedestal Clamp Pulse Width3 bit	R/W	Setting the pedestal clamp timing pulse width. Default value is PCLPWIDTH2 : PCLPWIDTH0 = 011 [PCLPWIDTH3□PCLPWIDTH0] 000 : 16 clks (592 nsec) 001 : 24 clks (888 nsec) 010 : 28 clks (1.04 usec) 011 : 32 clks (1.18 usec) 100 : 40 clks (1.48 usec) 101 : 44 clks (1.63 usec) 110 : 48 clks (1.78 usec) 111 : 52 clks (1.92 usec)
bit 6 □ bit 7	SLCLV0 □ SLCLV1	Slice Level Control bit	R/W	Setting the slice level Default value is 00 [SLCLV1:SLCLV0] = 00 :Sliced 1/4 level above the synctip 01 :Sliced 1/2 level above the synctip 10 :Prohibit to set 11: Sliced 3/8 level above the synctip

PGA1 Gain Control Register (R/W) [Sub Address 0x0D]

Sub Address 0x0D **Default Value : 0x40**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA1[6]	PGA1[5]	PGA1[4]	PGA1[3]	PGA1[2]	PGA1[1]	PGA1[0]
Default Value							
0	1	0	0	0	0	0	0

PGA1 Gain Control Register

BIT	Register Name		R/W	Definition
bit 0 □ bit 6	PGA1[0] □ PGA1[6]	PGA1[0] □ PGA1[6] bit	R/W	Setting PGA1 Gain. This register is available when Control 1 Register is set to [bit-1,0] = [0,0] (AGC Disable) Gain step of PGA is about 0.1dB/LSB.
bit 7	Reserved	Reserved	R/W	Reserved

PGA2 Gain Control Register (R/W) [Sub Address 0x0E]

Sub Address 0x0E **Default Value : 0x40**

bit 7	bit 6	bit 5	bit 4	bit 3		bit 1	bit 0
Reserved	PGA2[6]	PGA2[5]	PGA2[4]	PGA2[3]	PGA2[2]	PGA2[1]	PGA2[0]
Default Value							
0	1	0	0	0	0	0	0

PGA2 Gain Control Register

BIT	Register Name		R/W	Definition
bit 0 □ bit 6	PGA2[0] □ PGA2[6]	PGA2[0] □ PGA2[6] bit	R/W	Setting PGA2 Gain. This register is available when Control 1 Register is set to [bit-1,0] = [0,0] (AGC Disable) Gain step of PGA is about 0.1dB/LSB.
bit 7	Reserved	Reserved	R/W	Reserved

PGA3 Gain Control Register (R/W) [Sub Address 0x0F]

Sub Address 0x0F **Default Value : 0x40**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA3[6]	PGA3[5]	PGA3[4]	PGA3[3]	PGA3[2]	PGA3[1]	PGA3[0]
Default Value							
0	1	0	0	0	0	0	0

PGA3 Gain Control Register

BIT	Register Name		R/W	Definition
bit 0 □ bit 6	PGA3[0] □ PGA3[6]	PGA3[0] □ PGA3[6] bit	R/W	Setting PGA3 Gain. This register is available when Control 1 Register is set to [bit-1,0] = [0,0] (AGC Disable) Gain step of PGA is about 0.1dB/LSB.
bit 7	Reserved	Reserved	R/W	Reserved

YC SEPARATION CONTROL 1 REGISTER (R / W) [SUB ADDRESS :0x10]

This register sets YC Separation- related matters.

Sub Address 0x10 **Default Value : 0x06**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	CBPFS1	CBPFS0	YCSEP1	YCSEP0
Default							
0	0	0	0	0	1	1	0

YC Separation Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	YCSEP0 ~ YCSEP1	YC Separation bit	R/W	Setting YC Separation YCSEP1□YCSEP0 00 : 2D YC-Separation 01 : 1D YC-Separation 10 : Adaptive Y/CSeparation [Default] 11 : Reserved
bit 2 ~ bit 3	CBPFS0 ~ CBPFS1	C Band Pass Filter Select bit	R/W	Setting the Bandwidth of Chrominance signal CBPFS1:CBPFS0 00 : Reserved 01 : Wide [Default] 10 : Middle 11 : Narrow

Color Killer Control Register (R/W) [Sub Address 0x11]

Sub Address 0x11 **Default Value : 0xAD**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CL_KILL	Reserved	CKLVL5	CKLVL4	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
1	0	1	0	1	1	0	1

Color Killer Control Register Definition

BIT	Register Name		R/W	Definition
bit 1 ~ bit 5	CKLVL0 □ CKLVL5	Color Killer Level	R/W	Setting the color killer level. The range of color killer level is from -17db to -∞ with 63 step. 0 : -∞ dB 63 : -17dB Default value is 45 (-20dB) Setting value is defined as following formula Color killer level is CKL[dB]. Setting value = $10^{CKL/20}$ * 448
bit 6	Reserved	Reserved bit	R/W	Reserved
bit 7	CL-KILL	Color Killer bit	R/W	Color killer switch 0 : Color Killer disable. 1 : Color Killer enable[Default]

BRIGHTNESS CONTROL REGISTER (R / W) [SUB ADDRESS 0x12]

This register controls the Brightness adjustment.
Default value (0x00) corresponds to un-adjusted condition.

Sub Address 0x12 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	BR0 ~ BR7	Brightness Control bit	R/W	Brightness level is defined following formula -286mV Sync signal (without setup) 1□[BR7:BR0]*100/255 -286mV Sync signal (with setup) 1□[BR7:BR0]*108/255 -300mV Sync signal (without setup) 1□[BR7:BR0]*102/255 -300mV Sync signal (with setup) 1□[BR7:BR0]*111/255

CONTRAST CONTROL REGISTER (R / W) [SUB ADDRESS : 0x13]

This register controls the Contrast adjustment.
Default value (0x80) corresponds to un-adjusted condition.

Sub Address 0x13 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CONT0 ~ CONT7	Contrast Control bit	R/W	Contrast adjustment range is 0 to 2 by 1/256 step.

SATURATION CONTROL REGISTER (R / W) [SUB ADDRESS : 0x14]

This register controls Saturation adjustments.
Default value (0x80) corresponds to un-adjusted condition.

Sub Address 0x14 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

Saturation Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SAT0 ~ SAT7	Saturation Control bit	R/W	Saturation adjustment range is 0 to 2 by 1/256 step. It corresponds to the range between -∞ to 6dB.

HUE CONTROL REGISTER (R / W) [SUB ADDRESS : 0x15]

This register controls HUE adjustments.
Default value (0x00) corresponds to un-adjusted condition.
This register set is valid only when the Composite signal and YC signal are input (it is invalid with Component input signasl).

Sub Address 0x15 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HUE0 ~ HUE7	HUE Control bit	R/W	The range of Hue adjustment can be set form -90deg. to 90deg. by 1/256 Step Set with 2's complement value.

POWER SAVE REGISTER (R / W) [SUB ADDRESS : 0x1C]

Controls the transition to Power Save mode. Recovery from the Power Save mode is done by writing " 0 " to PS-bit.

Sub Address 0x1C **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	PLLRST	ADC3	ADC2	ADC1	PS
Default Value							
0	0	0	0	0	0	0	0

Power Save Register Definition

BIT	Register Name		R/W	Definition
bit 0	PS	Power Save bit	R/W	Power Save Mode setting register bit 0 : Switch to the Active mode from the Power Save Mode 1 : Switch to the Power Save Mode
bit 1	ADC1	AD1 Save bit	R/W	Power save mode for ADC1 0 : Switch to the Active mode 1 : Switch to the Power save mode
bit 2	ADC2	ADC2 Save bit	R/W	Power save mode for ADC2 0 : Switch to the Active mode 1 : Switch to the Power save mode
bit 3	ADC3	ADC3 Save bit		Power save mode for ADC3 0 : Switch to the Active mode 1 : Switch to the Power save mode
bit 4	PLLRST	PLL Reset bit	R/W	Reset the PLL control Circuit. Set to "1 " and set to "0" after setting "1".
bit 5 □ bit 7	Reserved	Reserved bit	R/W	Reserved

REQUEST VBI INFO REGISTER (W) [SUB ADDRESS : 0x1F]

This register controls VBI operations, including Closed- Caption, Extended data, VBID and WSS.
The AK8850 is put into a wait condition for each data when " 1 " is written into each bit.
When the decoding is completed, " 1" is written into each bit of the [STATUS 2 REGISTER] and the decoded data are stored in the Closed-Caption Data1 / Data2,CCEXTENDED Data1 / Data2,VBID Data1 / Data2 and WSS Data1 / Data2 registers respectively.

Sub Address 0x1F

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ	ASPECTRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Info Register Definition

BIT	Register Name		R/W	Definition
bit 0	ASPECTRQ	ASPECT Request bit	W	Request to decode ASPECT Signal 0 : 1 : Request
bit 1	CCRQ	Closed Caption Request bit	W	Request to decode Closed Caption data 0 : 1 : Request
bit 2	EXTRQ	Extended Data Request bit	W	Request to decode Extended data 0 : 1 : Request
bit 3	VBIDRQ	VBID Request bit	W	Request to decode VBID data 0 : 1 : Request
bit 4	WSSRQ	WSS Request bit	W	Request to decode WSS data 0 : 1 : Request
bit 5 □ bit 7	Reserved	Reserved bit	W	Reserved bit

STATUS 1 REGISTER (R) [SUB ADDRESS 0x20]

This register shows the internal status of the AK8850.

Sub Address 0x20

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COLKIL	FIELD	SCLKMODE1	SCLKMODE0	VSQLY	FRMSTD	VLOCK	NOSIG

Status 1 Register Definition

BIT	Register Name			Definition
bit 0	NOSIG	No Signal Indicates bit	R	No signal indicates This data also output from NSIG pin. 0 : Signal is input 1 : No signal is input
bit 1	VLOCK	Vsync Lock Indicates bit	R	Shows synchronization states of the input signal. 0 : Unsynchronaized to the input signal. 1 : Synchronaized to the input signal.
bit 2	FRMSTD	Frame Standard Indicates bit	R	Showing the Input video signal quality. 0 : Not 525/625 interlace video signal. 1 : 525/625 is interlace video signal.
bit 3	NSTD	Non Standard Signal Indicates bit	R	Showing the input video signal quality. This bit reflects the SCH status. For component video signal input, this bit depends on FRMSTD-bit. (This bit becomes 0 at FRMSTD-bit is 1) The data of this bit is also output from NSTD pin 0 : Standard signal is input. 1 : Non-standard signal is input.
bit 4 □ bit 5	SCLKMODE0 □ SCLKMODE1	Status Current Clock mode bit	R	Showing the clock-mode. [CLKMODE1:CLKMODE0] = 00 : Working with Fixed clock mode. 01 : Working with Line-Locked Clock mode 10 : Reserved 11 : Working with Frame-Locked Clock mode
bit 6	FIELD	Field Status bit		Showing the Field status 0 : ODD Field 1 : EVEN Field
bit 7	COLKIL	Color Killer Active bit	R	Showing the Color Killer Status 0 : Color Killer is not active 1 : Color Killer is active

STATUS 2 REGISTER (R) [SUB ADDRESS 0x21]

This register indicates the internal status of the AK8850.

Sub Address 0x21

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
APS1	APS0	Reserved	WSS	VBID	EXT	CC	ASPECT

Status 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	ASPECT	ASPECT Detect bit	R	Status of APSECT signal. 0 : Low (Normal) 1 : High (Wide)
bit 1	CC	Closed Caption detect bit	R	Closed Caption Data detect bit 0 : Closed Caption is not detected. 1 : Closed Caption is found.
bit 2	EXT	Extended Renewal bit	R	Extended Data detect bit 0 : Extended data is not detected. 1 : Extended data is found.
bit 3	VBID	VBID Renewal bit	R	VBID data detect bit 0 : VBID data is not detected. 1 : VBID data is found.
bit 4	WSS	WSS Renewal bit	R	WSS Data detect bit. 0 : WSS data is not detected. 1 : WSS data is found.
bit 5 □ bit 7	Reserved	Reserved bit	R	Reserved

CLOSED-CAPTION 1 REGISTER / CLOSED-CAPTION 2 REGISTER (R) [SUB ADDRESS 0x22 / 0x23]

These registers show the Closed-Caption information which is encoded on Line 21 / 22 (525 system / 625 system).

Sub Address 0x22

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Sub Address 0x23

bit 7	bit 6	bit 5		bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

Closed Caption 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CC0 ~ CC7	Closed Caption Data bit	R	Closed Caption Data

Closed Caption 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CC8 ~ CC15	Closed Caption Data bit	R	Closed Caption Data

EXTENDED DATA 1 REGISTER / EXTENDED DATA 2 REGISTER (R) [SUB ADDRESS 0x24 /0x25]

These registers show the EXTENDED DATA information which is encoded on Line 284 / 335 (525 system / 625 system).

Sub Address 0x24

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Sub Address 0x25

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

Extended Data 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	EXT0 ~ EXT7	Extended Data bit	R	Extended Data

Extended Data 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	EXT8 ~ EXT15	Extended Data bit	R	Extended Data

VBID 1 REGISTER / VBID 2 REGISTER (R) [SUB ADDRESS 0x26 / 0x27].

These registers show the VBID information which is encoded on Line 20 / 20 and Line 283 / 333 (525 system / 625 system).

Sub Address 0x26

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

Sub Address 0x27

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

VBID 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	VBID14 ~ VBID7	VBID Data bit	R	VBID Data

VBID 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	VBID6 ~ VBID1	VBID Data bit	R	VBID Data
bit 6 □ bit 7	Reserved	Reserved bit	R	Reserved bit

WSS 1 REGISTER / WSS 2 & ASPECT DATA REGISTER (R)[SUB ADDRESS 0x28 / 0x29]

These registers show WSS information encoded on Line 23.

Sub Address 0x28

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

Sub Address 0x29

bit 7	bit 6	bit 5	bit 4		bit 2	bit 1	bit 0
ASPDAT	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

WSS 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	G1-0 ~ G1-3	Group1 Data bit	R	WSS Group 1 data (Aspect ration)
bit 4 □ bit7	G2-4 □ G2-7	Group2 Data bit	R	WSS Group 2 data (Enhanced services)

WSS 2 & Aspect Data Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	G3-8 ~ G3-10	Group3 Data bit	R	WSS Group 3 data (Subtitles)
bit 3 □ bit 5	G4-11 □ G4-13	Group4 Data bit	R	WSS Group 4data (Reserved)
bit 6	Reserved	Reserved bit	R	Reserved bit
bit 7	ASPDAT	Aspect Data bit	R	Video aspect data

DEVICE & REVISION ID REGISTER (R) [SUB ADDRESS 0x2E]

This register indicates the device ID and Revision number of the AK8850.
The Device ID is 0x00. The initial Revision number is 0x00.
Revision number is renewed only when the control software needs to be modified.

Sub Address 0x2E

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DID3	DID2	DID1	DID0	REV3	REV2	REV1	REV0

Revision Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	REV0 ~ REV3	Revision bit	R	Indicates Revision data REV3□REV0 0x00
bit 4 □ bit 7	DID0 □ DID3	Device ID	R	Indicates Device ID AK8850 is 0x00

CLOCK CONTROL-1 REGISTER (R /W) [SUB ADDRESS 0x36]

This register controls the Clock transition time in Auto Clock mode which is set by [bit 7 : bit 6] of the Auto Select (CONTROL 2 REGISTER (0x09))

Sub Address 0x36 **Default Value : 0x84**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TTC1	TTC0	SKEWTH5	SKEWTH4	SKEWTH3	SKEWTH2	SKEWTH1	SKEWTH0
Default Value							
1	0	0	0	0	1	0	0

Clock Control-1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	SKEWTH0 □ SKEWTH5	Skew Detection Threshold	R/W	Set the threshold value for VTR Skew detection. Threshold value = [SKEWTH5:SKEWTH0]
bit 6 □ bit 7	TTC0 □ TTC1	Clock Transition Time Constant		Time Constant for clock mode transition. 0 : slowest 3 : fastest

CLOCK CONTROL-2 REGISTER (R / W) [SUB ADDRESS 0x37]

This register controls the Clock Transition time in Auto Clock mode which is set by [bit 7 : bit 6] of the Auto Select Control 2 Register (0x09).

Sub Address 0x37 **Default Value : 0x7C**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LNFRTH7	LNFRTH6	LNFRTH5	LNFRTH4	LNFRTH3	LNFRTH2	LNFRTH1	LNFRTH0
Default Value							
0	1	1	1	1	1	0	0

Clock Control-2 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	LNFRTH0 □ LNFRTH7	Lint to Frame Threshold Level Control bit	R/W	The threshold parameter from Line-Lock clock mode to Frame-Lock clock mode.

CLOCK CONTROL- 3 REGISTER (R / W) [SUB ADDRESS 0x38]

This register controls the Clock Transition time in Auto Clock mode which is set by [bit 7 : bit 6] of the Auto Select Control 2 Register (0x09).

Sub Address 0x38 **Default Value : 0x3C**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FRLNTH7	FRLNTH6	FRLNTH5	FRLNTH4	FRLNTH3	FRLNTH2	FRLNTH1	FRLNTH0
Default Value							
0	0	1	1	1	1	0	0

Clock Control 3 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	FRLNTH0 ~ FRLNTH7	Frame to Line Threshold Level Control bit	R/W	The threshold parameter from Frame-Lock clock mode to Line-Lock clock mode.

CLOCK CONTROL-4 REGISTER (R / W) [SUB ADDRESS : 0x39]

This register controls the Clock Transition time in Auto Clock mode which is set by [bit 7 : bit 6] of the Auto Select Control 2 Register (0x09).

Sub Address 0x39 **Default Value : 0xDC**

bit 7	bit 6	bit 5		bit 3	bit 2	bit 1	bit 0
FRFXTH7	FRFXTH6	FRFXTH5	FRFXTH4	FRFXTH3	FRFXTH2	FRFXTH1	FRFXTH0
Default Value							
1	1	0	1	1	1	0	0

Clock Control 4 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	FRFXTH0 ~ FRFXTH7	Frame to Fix Clock Threshold Level Control bit	R/W	The threshold parameter from Frame-Lock clock mode to Fixed clock mode.

CLOCK CONTROL-5 REGISTER (R / W) [SUB ADDRESS 0x3A]

This register controls the Clock Transition time in clock Auto Mode set by (bit 7 : bit 6) of the Auto Select Control 2 Register (0x09).

Sub Address 0x3A **Default Value : 0x04**

bit 7	bit 6	bit 5		bit 3	bit 2	bit 1	bit 0
FXLNTH7	FXLNTH6	FXLNTH5	FXLNTH4	FXLNTH3	FXLNTH2	FXLNTH1	FXLNTH0
Default Value							
0	0	0	0	0	1	0	0

Clock Control 5 Register Definition

BIT	Register Name			Definition
bit 0 ~ bit 7	FXLNTH0 ~ FXLNTH7	Fix Clock to Line Threshold Level Control bit	R/W	The threshold parameter for switching between the Fixed clock and Line-Lock clock modes.

PLL CONTROL REGISTER (R / W) [SUB ADDRESS 0x46]

PLL control register.

Sub Address 0x46 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	LPGAUTO	LPG3	LPG2	LPG1	LPG0	LPGM1	LPGM2
Default Value							
0	0	0	0	0	0	0	0

PLL Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 □ bit 1	LPGM2:LPGM1	Loop Gain Control bit	R/W	FRAME LOCK Mode EC gain LPGM[1:2] = 00 : x 1 (Default□ 01 : x 2 10 : x 4 11 : x 8
bit 2 □ bit 5	LPG0:LPG3	Loop Gain Control bit	R/W	LPG[1:0] Line Lock mode EC gain[1:0] 00 : x 1 (Default□ 01 : x 1/2 10 : x 4 11 : x 2 LPG[2] CP gain 0 : x 1 (Default□ 1 : x 2 LPG[3] GM gain 0 : x 1 (Default) 1 : x 2
bit 6	LPGAUTO	Loop Gain Auto bit	R/W	0 : Manual□Default□ 1 : Auto In case of Auto mode setting, LPG2 and LPG3 settings are ignored and the CP and GM gains are switched automatically depending on the PLL mode. Line-Lock mode: CP□x 1 (Low), GM : x1 (Low) Frame-Lock mode : CP : x 2 (High) , GM : x 2 (High)
bit 7	Reserved	Reserved bit	R/W	Reserved

PLL DAC SET REGISTER (R / W) [SUB ADDRESS 0x47]

PLL control register.

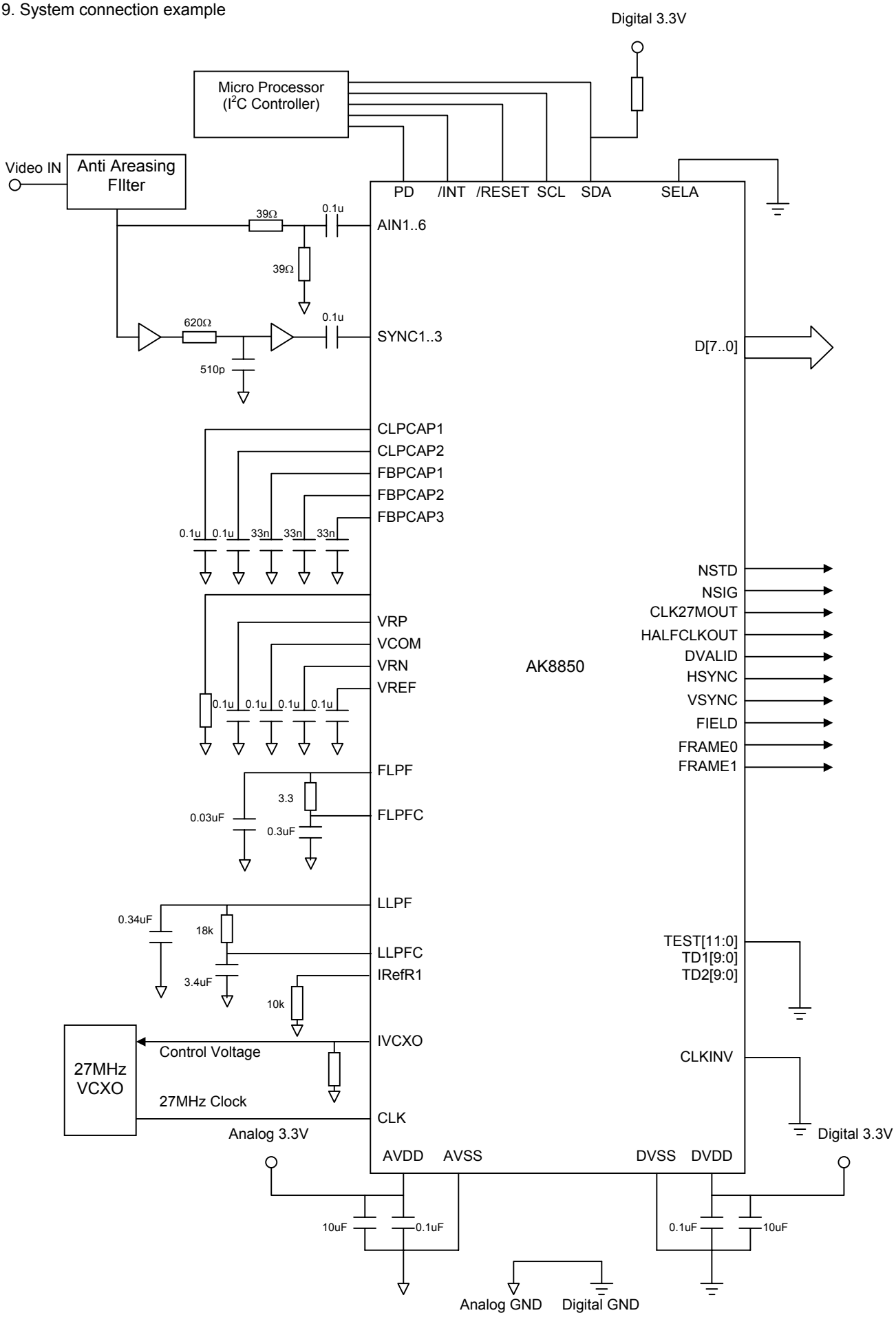
Sub Address 0x47 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PLLDACI7	PLLDACI6	PLLDACI5	PLLDACI4	PLLDACI3	PLLDACI2	PLLDACI1	PLLDACI0
Default Value							
1	0	0	0	0	0	0	0

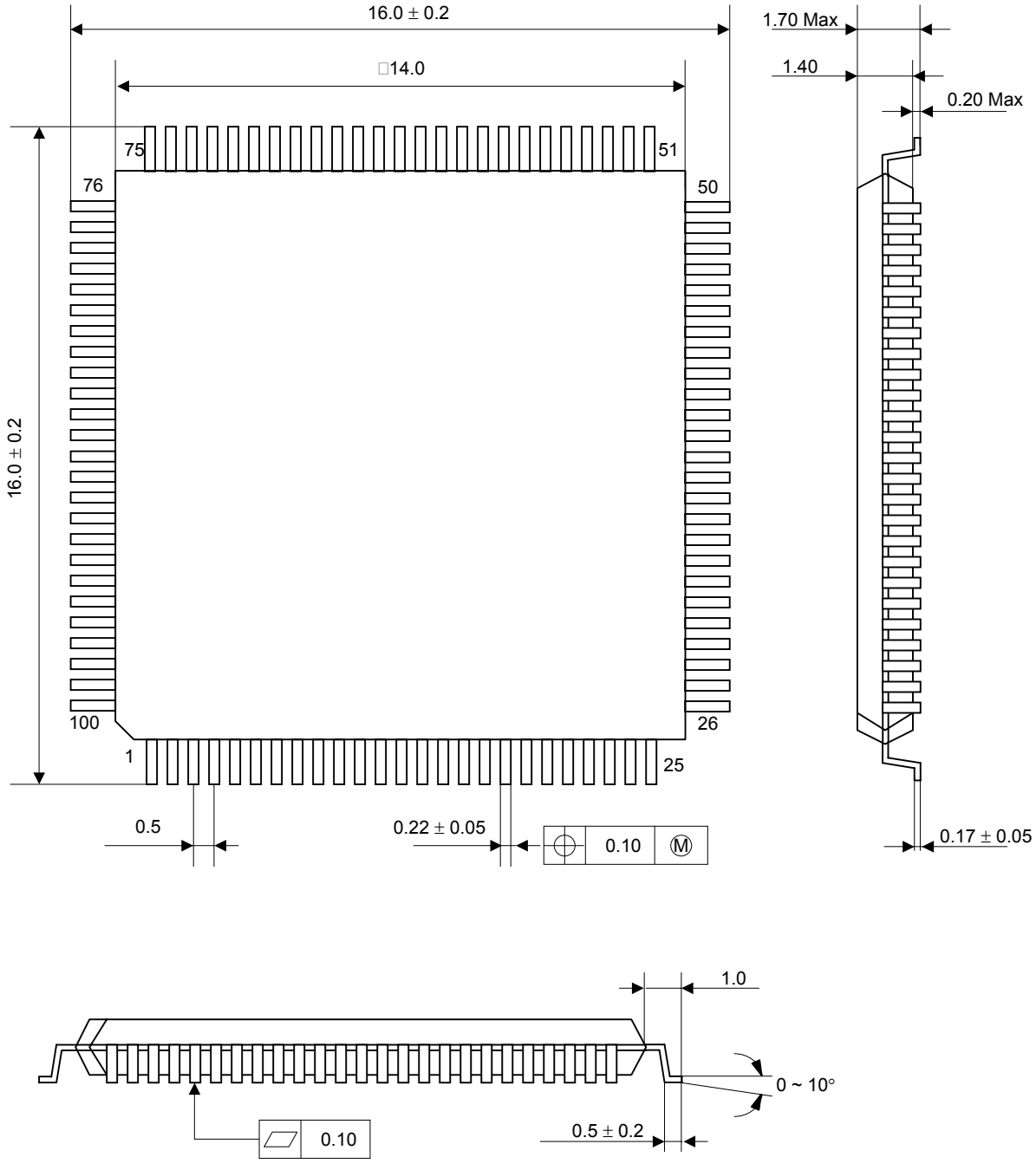
PLL DAC Set Register Definition

BIT	Register Name		R/W	
bit 0 □ bit 7	PLLDACI0 □ PLLDACI7	PLL DAC INPUT bit	R/W	Adjust the External VCXO center frequency with this register. LSB is always disabled.

9. System connection example



10. Package 100pin LQFP



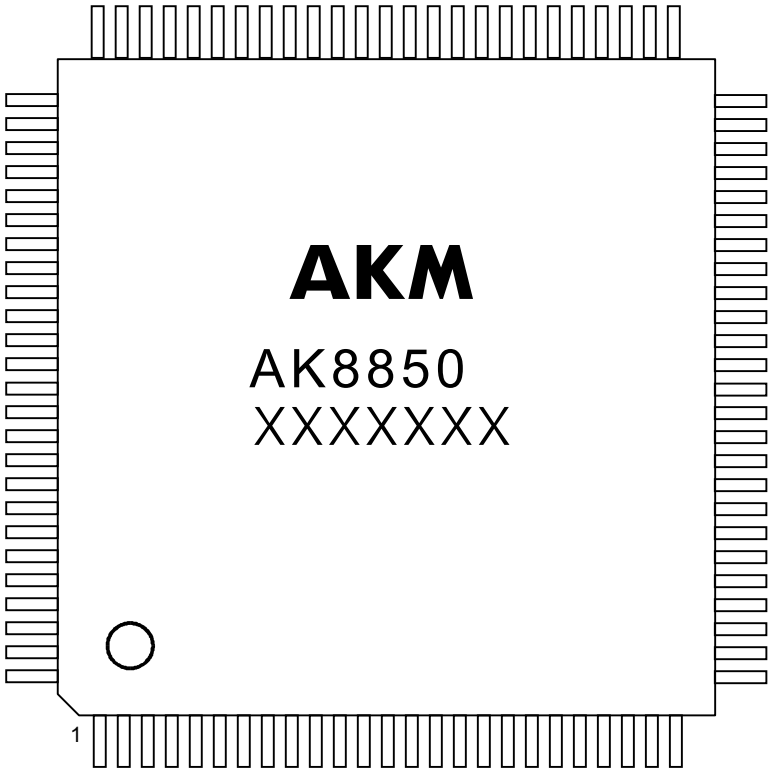
Package & Lead frame material

Package molding compound□ Epoxy

Lead frame material□ Cu

Lead frame surface treatment: Solder plate

11. Marking



1) AKM : AKM Logo

2) AK8850 : Marketing Code

3) XXXXXXX (7digits) : Date Code

4) ○□Pin #1 indication

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