AK9822/24

2K / 4Kbit EEPROM with 2ch 8bit D/A Converter

General Description

The AK9822/24 includes 2 channel, 8 bit D/A converters with on-chip output buffer amps and it is capable to store the input digital data of each D/A converter by on-chip non-volatile CMOS EEPROM. The AK9822/24 is optimally designed for various circuit adjustments for consumer and industrial equipments and it is ideally suited for replacing mechanical trimmers.

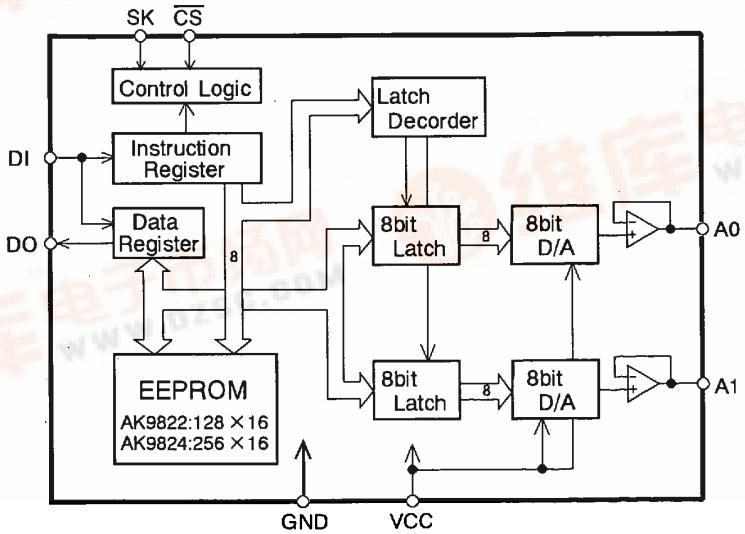
Feature

☐ EEPROM section
- AK9822・・・128 words × 16bit
- AK9824・・・256 words × 16bit
- One chip microcomputer interface
- Sequential register read

☐ D/A Converter section
- 2 channel
- Resolution : 8bit
- Differential Non-Linearity : ±1.0 LSB
- Linearity Error : ±1.5 LSB
- Output Voltage Range : GND ~ VCC

☐ Wide VCC operation
- • EEPROM section : 1.8V~5.5V
- • D/A Converter Section : 2.7V~5.5V

☐ Power Down Function

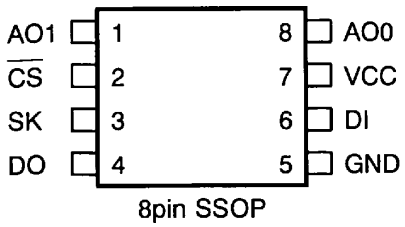


Block Diagram

■ Ordering Guide

AK9822M	-40°C~+85°C	8pin SSOP
AK9824M	-40°C~+85°C	8pin SSOP

■ Pin Layout



■ Pin Description

No.	Pin Name	I/O	Function
1	AO1	O	Analog Output Pin
2	$\overline{CS}$	I	Chip Select Pin (Schmitt-trigger input)
3	SK	I	Serial Clock Pin (Schmitt-trigger input)
4	DO	O	Serial Data Output Pin
5	GND	-	Ground Pin
6	DI	I	Serial Data Input Pin
7	VCC	-	Power Supply
8	AO0	O	Analog Output Pin

Functional Description

The AK9822/24 is composed of EEPROM and the 8bit D/A converter of two channels with the output buffer amplifier.
The AK9822/24 can connect to the serial communication port of popular one chip microcomputer directly (3 line negative clock synchronous interface).
The AK9822/24 takes the data of the DI pin by the rising edge of the SK pin and outputs the data from the DO pin by the falling edge of the SK pin.
The AK9822/24 has 7 instructions such as READ, WRITE, WREN, WRDS, PDEN, PDDS and CALL. The AK9822/24 is operated by inputting these instructions from the serial interface. Each instruction is organized by op-code block (8bits), address block (8bits) and data (8bits×2).
The DO pin is "Hi-Z" state except that the DO pin outputs the data of the internal register and the status of Ready/$\overline{\text{Busy}}$.

■ WRITE protection function

There are two states such as the WRITE enable state and the WRITE disable state in the AK9822/24. In the WRITE disable state the WRITE instruction becomes invalid and is not executed. When Vcc is applied to the part, the part powers up in the WRITE disable state and the part becomes the WRITE enable state by inputting the WREN instruction. The WRITE enable state continues until the WRDS instruction is executed or Vcc is removed from the part.
Execution of a READ instruction is independent of both WREN and WRDS instructions.

■ Power down function

There are two modes such as the power down mode and the normal mode in the AK9822/24. When the AK9822/24 is in the power down mode, the D/A converter section is in the standby state. At this time, the outputs of the D/A converters become "Hi-Z".

When Vcc is applied to the part, the AK9822/24 is in the power down mode. When a AUTO READ function is executed, the part becomes the normal mode. After the AUTO READ function is executed, the mode of the part can be switched by the PDEN and PDDS instructions. The AK9822/24 becomes the power down mode by inputting the PDEN instruction. The part is in the power down mode until the PDDS instruction is executed. When the PDDS instruction is executed, the part becomes the normal mode.
When returning to the normal mode from the power down mode, the D/A converters output the voltage value set before entering the power down mode. The relation between the D/A converter state and the mode are shown in the table 1.

Mode	State of D/A converter
Power down mode	standby
Normal mode	normal

Table 1. The relation between the state of D/A converter and the mode

■ **Output of D/A converter**

The output of the D/A converters can be set by the WRITE and the CALL instructions.
Upper 8bit data (D15~D8) of the first address of the internal EEPROM (the address "0") corresponds to "AO" of the D/A converter output. Lower 8bit data (D7~D0) of the address "0" corresponds to "A1". The internal composition of EEPROM is shown in the table2.

Address	D15~D8	D7~D0
0	Set data of A0	Set data of A1
1	General purpose memory	
〉	〉	
127(AK9822) /255(AK9824)	General purpose memory	

Table2. Internal composition of EEPROM

If the WRITE instruction by which the address "0" is specified is executed at the normal mode, the outputs of the D/A converter of A0 and A1 are set by the specified data.
When the WRITE instruction by which the address "0" is specified is executed at the WRITE enable state and the normal mode, the data is written in the address "0" of EEPROM and the outputs of the D/A converter are set. When the WRITE instruction by which the address "0" is specified is executed at the WRITE disable state and the normal mode, the data is not written in EEPROM and the outputs of the D/A converter are set. Table3 shows the relation between EEPROM, D/A converter and WRITE instruction.

State of AK9822/24		State of address"0"	Output of A0 and A1
Power down mode	WRITE enable	The data change to the specified data.	The DAC outputs are "Hi-Z".
	WRITE disable	The data does not change.	
Normal mode	WRITE enable	The data change to the specified data.	The DAC outputs change to the specified data.
	WRITE disable	The data does not change.	

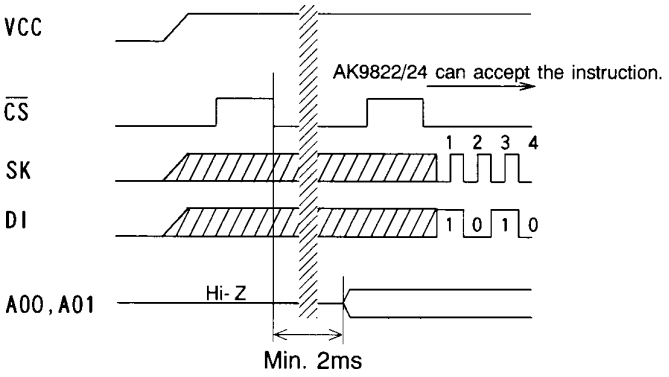
Table3. Relation between EEPROM, D/A converter and WRITE instruction

If the CALL instruction is executed, the outputs of the D/A converter are set by the data of the general purpose memory (AK9822:address "1" -"127", AK9824:address "1" -"255"). The CALL instruction is composed by the op-code and the address.
When the CALL instruction is executed at the normal mode, the D/A converter output of A0 is set by the upper 8bit data (D15~D8) of the specified address and the output of A1 is set by the lower 8bit data (D7~D0). The CALL instruction is not executed at the power down mode.

■ AUTO READ function

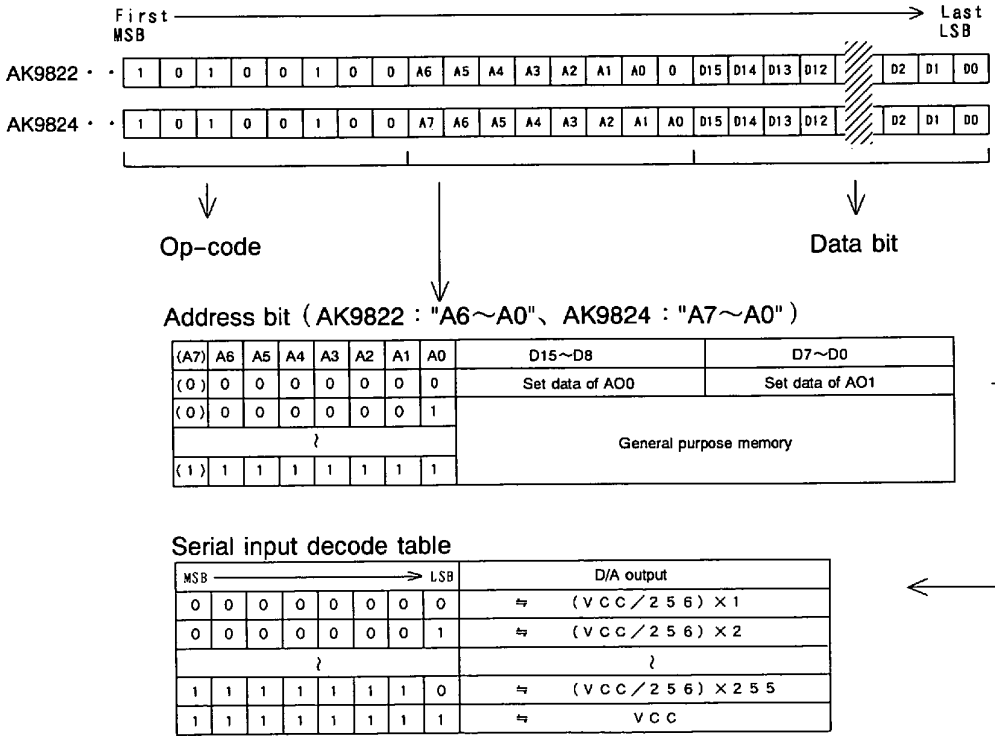
AUTO READ function automatically reads the content of EEPROM and sets the output of the D/A converter of two channels, when Vcc is applied to the part.
When Vcc is applied to the part in $\overline{CS}$="L", the AUTO READ function starts by falling $\overline{CS}$ pin first. After the $\overline{CS}$ pin is made a low level, the output of AO0 and AO1 is set within 2ms. At this time, the input pins (SK, DI) other than the $\overline{CS}$ pin are not accepted, and the serial data is not output from the DO pin. If the WREN instruction is executed after the AUTO READ function finished, AK9822/24 becomes the WRITE enable state.
After Vcc is applied to the part, the AUTO READ function is executed only once.
AUTO READ function is executed when Vcc is applied to the part in $\overline{CS}$="L".

(note) Because AK9822/24 always executes the AUTO READ function first after Vcc is applied to the part, AK9822/24 is not able to accept the instruction for the first period of "L" of the $\overline{CS}$.



■ Instruction and Composition of the data

Each instruction consist of op-code, address, and data (8bit×2) composed in each 8bit. The composition of the WRITE instruction is shown as follows.



Instruction Set

The AK9822/24 has 7 instructions such as READ, WRITE, WREN, WRDS, PDEN, PDDS, CALL. Each instruction consists of Op-code, address and data. The instruction set is shown in the table4 and table5.

When the instructions are executed consecutively, the CS pin should be brought to a high level for a minimum of tCS between consecutive instruction cycle.

Instruction	Op-code	Address	Data	Comments
READ	1 0 1 0 1 0 0 0	A6 A5 A4 A3 A2 A1 A0 0	D15~D0	read memory
WRITE	1 0 1 0 0 1 0 0	A6 A5 A4 A3 A2 A1 A0 0	D15~D0	write memory
WREN	1 0 1 0 0 0 1 1	* * * * * * * *	* ~	write enable
WRDS	1 0 1 0 0 0 0 0	* * * * * * * *	* ~	write disable
PDEN	1 0 1 0 1 1 0 0	* * * * * * * *	* ~	power down enable
PDDS	1 0 1 0 0 1 1 0	* * * * * * * *	* ~	power down disable
CALL	1 0 1 0 0 0 1 0	A6 A5 A4 A3 A2 A1 A0 0	* ~	set DAC outputs
TEST	1 0 1 0 1 1 1 1	* * * * * * * *	* ~	TEST (note)

(note) User can't use this instruction. *: Don't Care

Table4. Instruction set for AK9822

Instruction	Op-code	Address	Data	Comments
READ	1 0 1 0 1 0 0 0	A7 A6 A5 A4 A3 A2 A1 A0	D15~D0	read memory
WRITE	1 0 1 0 0 1 0 0	A7 A6 A5 A4 A3 A2 A1 A0	D15~D0	write memory
WREN	1 0 1 0 0 0 1 1	* * * * * * * *	* ~	write enable
WRDS	1 0 1 0 0 0 0 0	* * * * * * * *	* ~	write disable
PDEN	1 0 1 0 1 1 0 0	* * * * * * * *	* ~	power down enable
PDDS	1 0 1 0 0 1 1 0	* * * * * * * *	* ~	power down disable
CALL	1 0 1 0 0 0 1 0	A7 A6 A5 A4 A3 A2 A1 A0	* ~	set DAC outputs
TEST	1 0 1 0 1 1 1 1	* * * * * * * *	* ~	TEST (note)

(note) User can't use this instruction. *: Don't Care

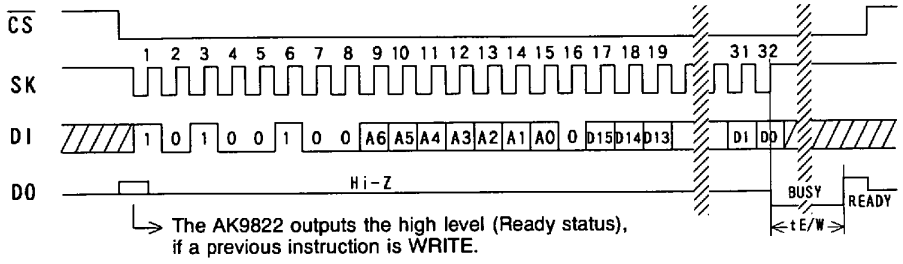
Table5. Instruction set for AK9824

■ WRITE

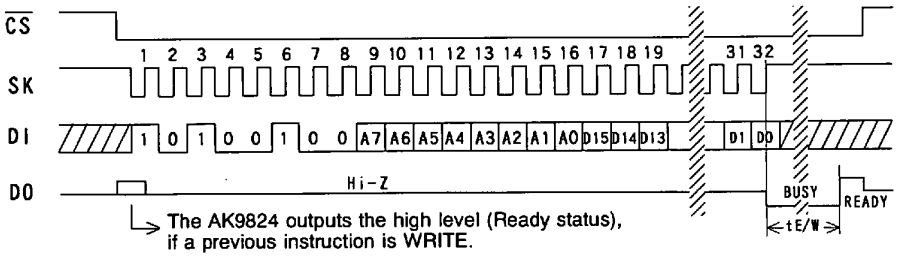
The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the 32nd rising edge of SK to read the DI pin in, the AK9822/24 will be put into the automatic write time-out period.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the EEPROM in the AK9822/24. After the 32nd rising edge of SK to read the Di pin in, the AK9822/24 will be put into the automatic write time-out period. When the automatic write time-out period starts, the DO pin outputs the Ready/$\overline{\text{Busy}}$ status. When the DO pin outputs the low level, the AK9822/24 is in the automatic write time-out and the next instruction can not be accepted. When the DO pin outputs the high level, the automatic write time-out period has ended and the AK9822/24 is ready for a next instruction.

When the $\overline{\text{CS}}$ pin is changed to high level after confirmation of Ready/$\overline{\text{Busy}}$ signal on the DO pin, the DO pin becomes "Hi-Z". The Ready/$\overline{\text{Busy}}$ signal outputs until the $\overline{\text{CS}}$ pin is changed to high level, or the initial 1 bit ("1") of the next instruction is given to the part.



WRITE (AK9822)



WRITE (AK9824)

■ READ

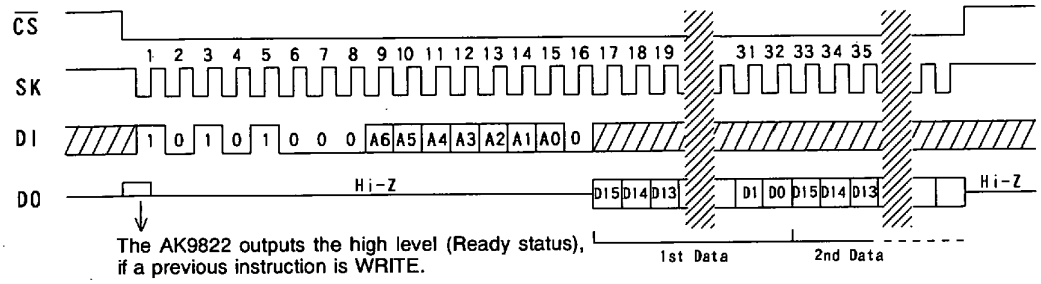
The READ instruction is the only instruction which outputs serial data on the DO pin. When the 17th falling edge of SK is received, the Do pin will come out of high impedance state and shift out the data from D15 first in descending order which is located at the address specified in the instruction.

○ Sequential READ

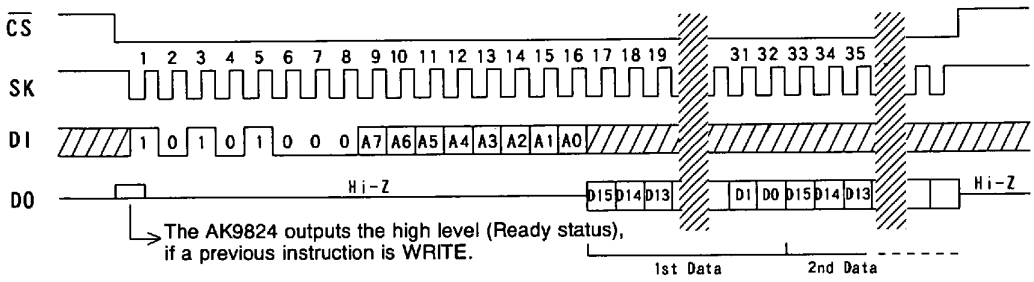
When the clock is provided on the SK pin after the data in the specified address is read, the data in the next address is read.

AK9822・・ When the clock is provided on the SK pin after the data in the address:7F (Hex) is read, the data in the address:00 (Hex) is read.

AK9824・・ When the clock is provided on the SK pin after the data in the address:FF (Hex) is read, the data in the address:00 (Hex) is read.



READ (AK9822)

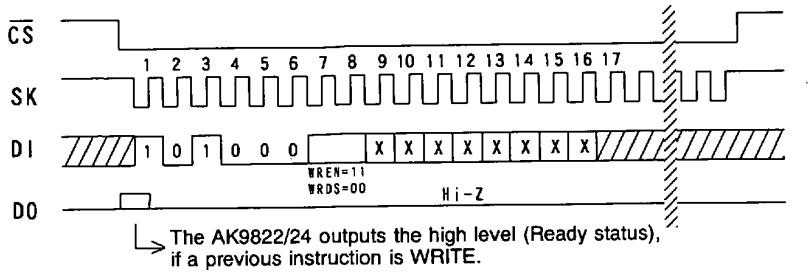


READ (AK9824)

■ **WREN/WRDS**

There are two states such as the WRITE enable state and the WRITE disable state in the AK9822/24. In the WRITE disable state the WRITE instruction becomes invalid and is not executed. When Vcc is applied to the part, it powers up in the WRITE disable state. The WRITE instruction must be preceded by a WREN instruction. This state remains enabled until a WRDS instruction is executed or Vcc is removed from the part.

Execution of a read instruction is not affected by both WREN and WRDS instruction.

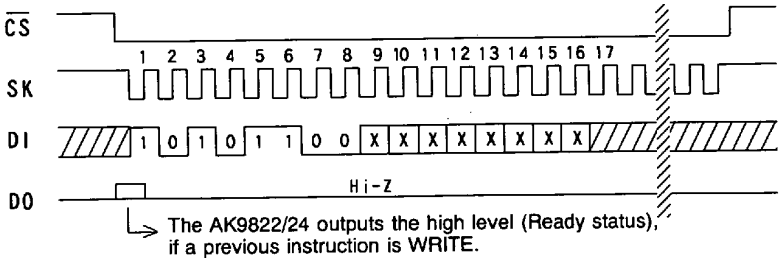


WREN/WRDS (AK9822/24)

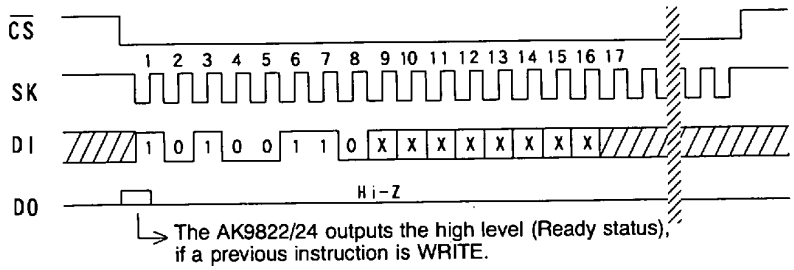
■ **PDEN/PDDS**

There are two modes such as the power down mode and the normal mode in the AK9822/24. The mode of the part can be switched by the PDEN and PDDS instructions. The AK9822/24 becomes the power down mode by inputting the PDEN instructions. When the PDDS instruction is executed, the part becomes the normal mode.

When returning to the normal mode from the power down mode, the D/A converters output the voltage value set before entering the power down mode.



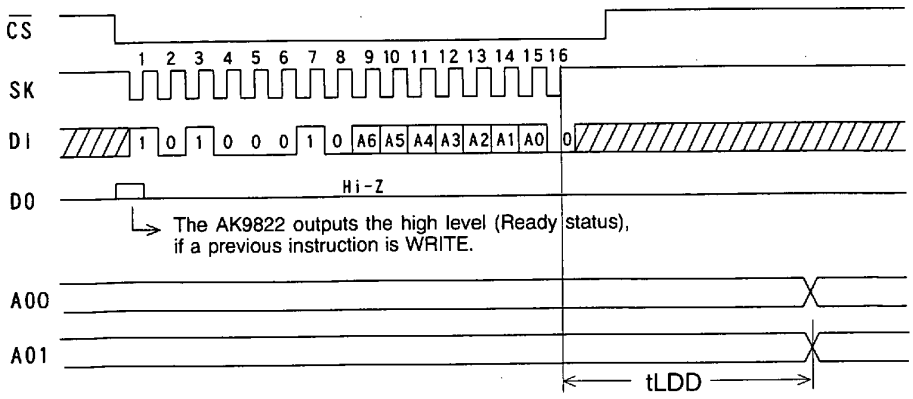
PDEN (AK9822/24)



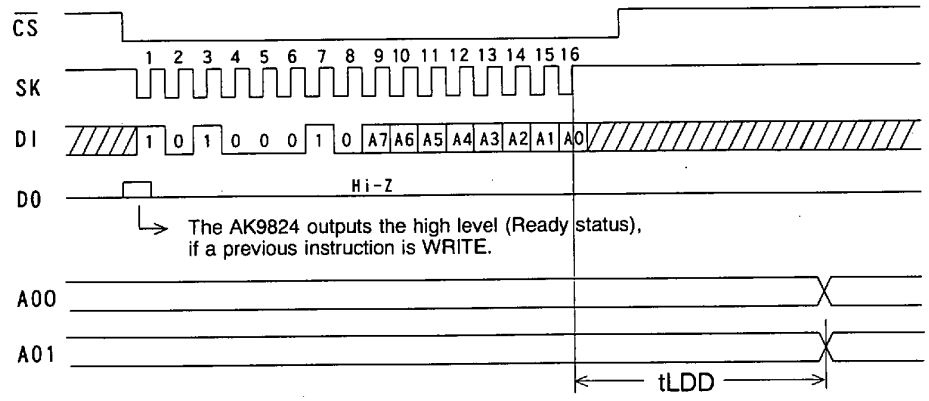
PDDS (AK9822/24)

■ CALL

The outputs of the D/A converters is set by inputting a CALL instruction. Upper 8bit data (D15~D8) of the specified address corresponds to "A0". Lower 8bit data (D7~D0) of the specified address corresponds to "A1".
The CALL instruction is not executed at the power down mode.



CALL (AK9822)



CALL (AK9824)

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Spec.	Units
Power supply	VCC	Relative to GND	-0.6~+7.0	V
Input voltage	VIO	Relative to GND	-0.6~VCC+0.6	V
Ambient temperature	Ta		-40~+85	°C
Storage temperature	TST		-65~+150	°C

Recommended Operating conditions

Parameter	Symbol	Conditions	min	typ	max	Units
Power supply	VCC1	DAC operation	2.7		5.5	V
	VCC2	EEPROM operation	1.8		5.5	V
Analog output source current1	IAL1	3.6V≤VCC ≤5.5V			1	mA
Analog output sink current1	IAH1				1	mA
Analog output source current2	IAL2	2.7V≤VCC<3.6V			500	uA
Analog output sink current2	IAH2				500	uA
Analog output load capacitance	AOC				1.0	uF

Electrical characteristics

■ DC characteristics

(VCC=+1.8V~5.5V, GND=0V, Ta=-40~+85°C unless otherwise specified)

Parameter	Symbol	Conditions	min	max	Units
Operating power consumption	IDD1	Normal mode WRITE, 1/tSKP=2MHz		5.5	mA
	IDD2	Normal mode READ, 1/tSKP=2MHz		2.3	mA
(note1),(note3)	IDD3	Power down mode READ, 1/tSKP=2MHz		0.75	mA
Standby (note2),(note3) power consumption	IDD4	Power down mode standby($\overline{CS}$="H")		1.0	uA
Input high voltage $\overline{CS}$,SK pin	VIH1 VIH2	2.5V≤VCC≤5.5V 1.8V≤VCC<2.5V	0.8×VCC 0.9×VCC		V V
Input high voltage DI pin	VIH3 VIH4	2.5V≤VCC≤5.5V 1.8V≤VCC<2.5V	0.7×VCC 0.8×VCC		V V
Input low voltage $\overline{CS}$,SK pin	VIL1 VIL2	2.5V≤VCC≤5.5V 1.8V≤VCC<2.5V		0.2×VCC 0.1×VCC	V
Input low voltage DI pin	VIL3 VIL4			0.3×VCC 0.2×VCC	V
Output high voltage	VOH1 VOH2	(note4),IOH=-50uA (note5),IOH=-50uA	VCC-0.3 VCC-0.3		V V
Output low voltage	VOL1 VOL2	(note4),IOL=1.0mA (note5),IOL=0.1mA		0.4 0.4	V V
Input leakage current	ILI	VCC=5.5V,VIN=VCC		±1.0	uA
3 state leakage current	IOZ	VCC=5.5V,DO=VCC $\overline{CS}$="H"		±1.0	uA

note1. VCC=5.5V,VIN=VIH/VIL,DO=open
note2. VCC=5.5V,SK/DI=VCC/GND,DO=open
note3. Please refer to the "Power down function" regarding the power down mode.
note4. 2.5V≤VCC≤5.5V
note5. 1.8V≤VCC<2.5V

■ AC characteristics

1)EEPROM section

(VCC=+1.8V~5.5V, GND=0V, Ta=-40~+85°C unless otherwise specified)

Parameter	Symbol	Conditions	min	max	Units
SK cycle	tSKP1 tSKP2	(note6),(note7) (note8)	500 1.5		ns us
SK pulse width	tSKW1 tSKW2	(note6),(note7) (note8)	250 750		ns ns
SK pulse high level width (note10)	tSKH1 tSKH2 tSKH3	(note6) (note7) (note8)	250 500 750		ns ns ns
$\overline{CS}$ setup time	tCSS		100		ns
$\overline{CS}$ hold time	tCSH1	READ WREN, WRDS PDEN, PDDS	100		ns
	tCSH2	CALL WRITE (note9)	2		us
SK setup time	tSKS		100		ns
Data setup time	tDIS1 tDIS2 tDIS3	(note6) (note7) (note8)	100 150 200		ns ns ns
data hold time	tDIH1 tDIH2 tDIH3	(note6) (note7) (note8)	100 150 200		ns ns ns
DO pin output delay (note11), (note13)	tPD1 tPD2 tPD3	(note6) (note7) (note8)		150 250 500	ns ns ns
Selftimed program time	tE/W			10	ms
Write recovery time	tRC		100		ns
Min. $\overline{CS}$ high time (note12)	tCS		250		ns
DO pin high-Z time	tOZ			500	ns

note6. 4.0V≤VCC≤5.5V

note7. 2.5V≤VCC<4.0V

note8. 1.8V≤VCC<2.5V

note9. In case of the following case, tCSH is min.100ns.

- The WRITE instruction by which the address "0" is specified is executed at the WRITE enable state.
- The WRITE instruction by which the address "1~127/255" is specified is executed.

note10. The tSKH is the high pulse width of 16th SK pulse in READ operation. When the data in the next address are read sequentially by continuing to provide clock, tSKH are applied to the high pulse width of 32nd and 48th (multiple of 16) SK pulse in READ operation.

note11. In case that Ready/$\overline{Busy}$ signal output, tPD is min.1us.

note12. The first $\overline{CS}$ high time is the tACS after Vcc is applied to the part.

note13. CL=100pF

2)D/A converter section

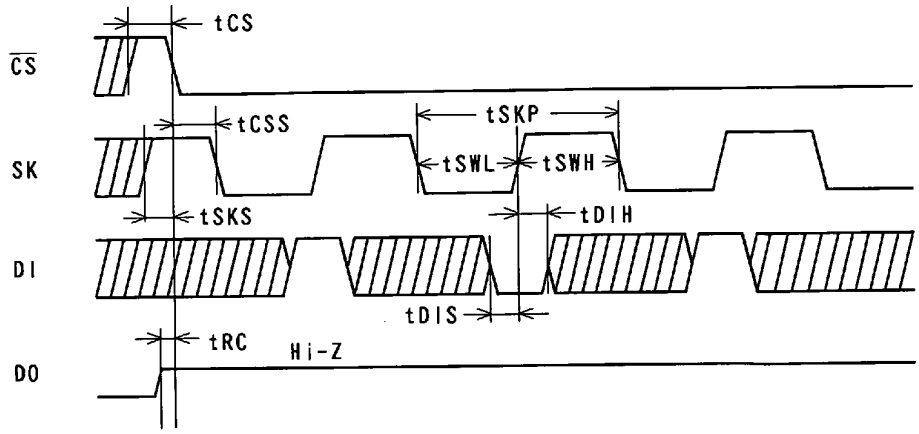
(2.7V≤VCC≤5.5V, GND=0V, Ta=-40~+85°C unless otherwise specified)

Parameter	Symbol	Conditions	min	typ	max	Units
Resolution		Monotonic			8	bit
Differential non-linearity	DNL	AO=OPEN 0.1≤AO ≤VCC-0.1	-1.0	0	+1.0	LSB
linearity error (note14)	NL		-1.5	0	+1.5	LSB
Buffer amp output voltage range 3.6V≤VCC≤5.5V	VAO1	|IAO|= 0uA	0.1		VCC-0.1	V
	VAO2	|IAO|≤1mA	0.3		VCC-0.3	V
Buffer amp output voltage range 2.7V≤VCC<3.6V	VAO3	|IAO|= 0uA	0.1		VCC-0.1	V
	VAO4	|IAO|≤500μA	0.3		VCC-0.3	V
$\overline{CS}$ setup time when VCC is applied to the part	tCSA		5.0			us
$\overline{CS}$ hold time in AUTOREAD	tACS		5.0			us
DAC setting time (note15)	tLDD1 tLDD2	3.6V≤VCC≤5.5V 2.7V≤VCC<3.6V		100	200 400	us us

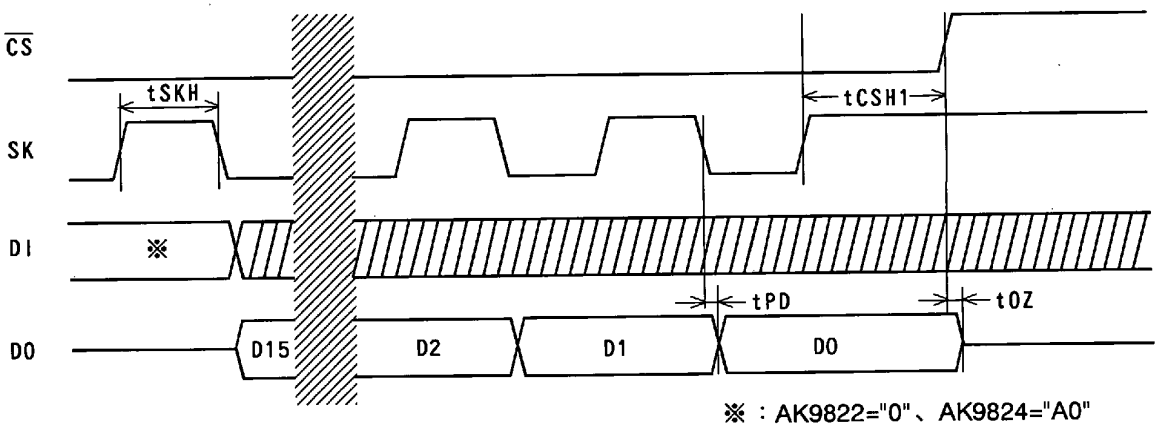
note14. Integral non-linearity is the error between the actual line and the ideal line. The ideal line exhibits a perfect linear D/A converter output characteristics between the input digital data "00" and the input digital data "FF".

note15. CL=100pF

■ **Timing waveform**

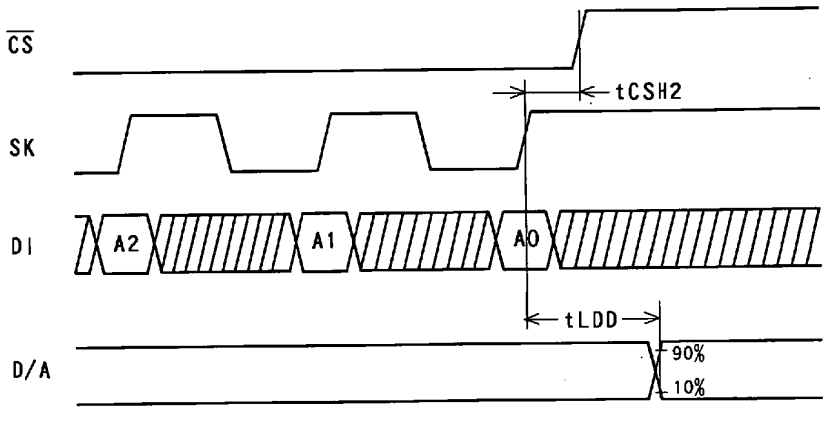


Instruction input timing

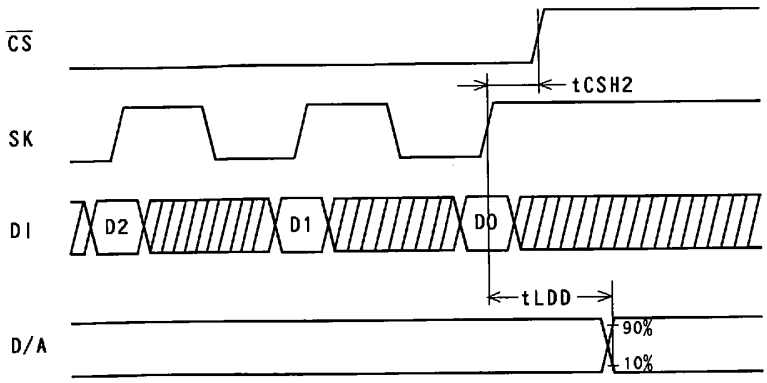


※ : AK9822="0"、AK9824="A0"

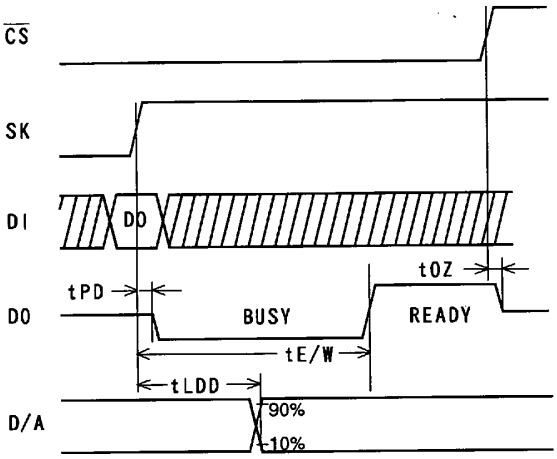
Data latch timing in READ operation



D/A converter output timing in CALL instruction

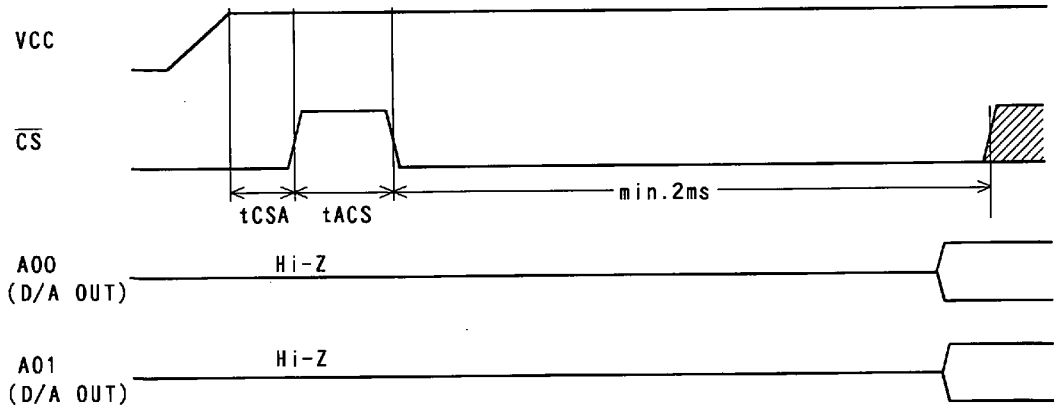


Programming timing in WRITE instruction



READY/$\overline{\text{BUSY}}$ signal output timing

note : READY/$\overline{\text{BUSY}}$ signal does not output when WRITE instruction is executed in WRITE disable state.



AUTO READ timing

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