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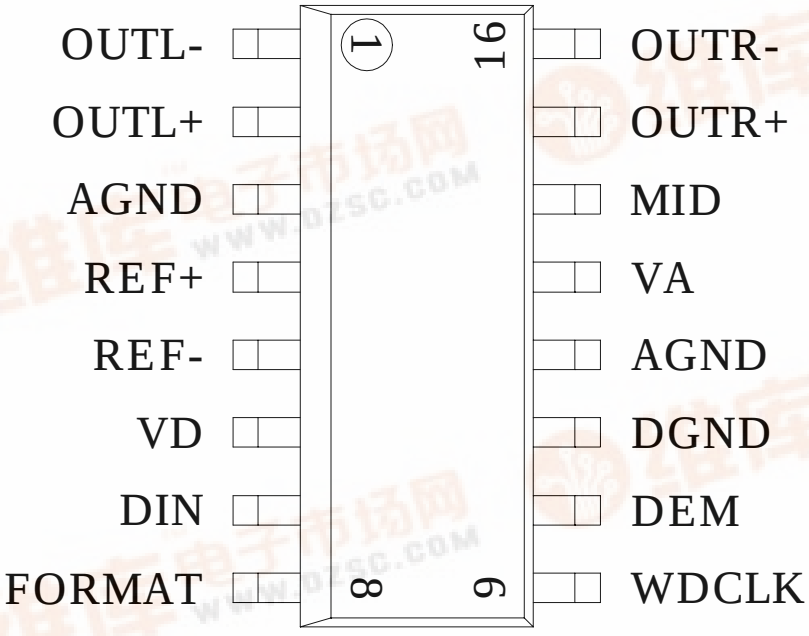
DAC AL1201 Converter

General Description

The AL1201 stereo DAC is a high performance 24-bit digital to analog audio converter. Dynamic range is 107dB (A-weighted). The sensible pinout and easy user interface are unprecedented. The part contains an internal high quality phase-locked loop that eliminates the need for external high frequency clocks.

Features

- 24 bit conversion
- 107dB dynamic range (A-wt)
- .003% THD at full scale output
- linear phase analog outputs
- 128x over sampling, 5th order 1 bit Δ-Σ modulator
- 2nd order switched cap filter and 2nd order continuous-time filter on chip
- sample rate variable 24kHz-55kHz
- selectable deemphasis (15us/50µs at Fs=44.1kHz)
- total power consumption 170mW (Fs=48kHz)
- internal PLL derives all necessary timing signals from external Fs clock
- serial input bit-rate, selectable 32/24 bits/frame
- full scale differential output = +/-4V ([OUT+]-[OUT-])
- 5V operation

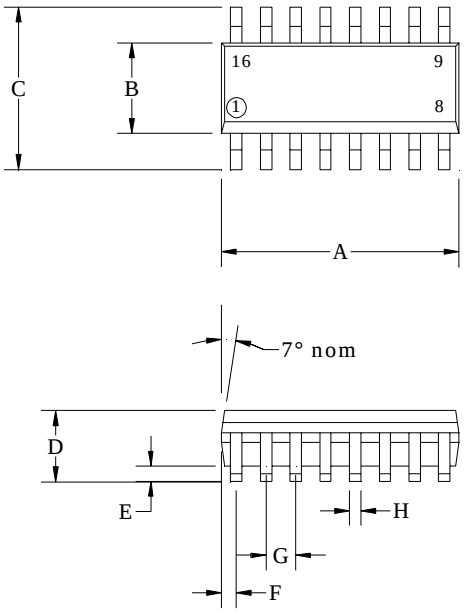


16 pin SOIC
150 mils wide

Alesis Semiconductor
12555 Jefferson Blvd., Suite 285
Los Angeles, CA 90066
Phone (310) 301-0780 Fax (310) 306-1551 www.alesis-semi.com

Pin Description

Pin #	Name	Pin Type	Description
1	OUTL-	OUTPUT	negative analog output, left channel
2	OUTL+	OUTPUT	positive analog output, left channel
3	AGND	GND	analog ground
4	REF+	PWR	positive reference, 5V, connect .1µ bypass cap to REF-
5	REF-	GND	negative reference, connect to GND
6	VD	PWR	digital supply, 5V, connect .1µ bypass cap to GND
7	DIN	INPUT	serial data input
8	FORMAT	INPUT	format select, 0=32 bits/frame, 1=24bits/frame
9	WDCLK	INPUT	sample frequency wordclock
10	DEM	INPUT	deemphasis select, 0=no deem, 1=deem
11	DGND	GND	digital ground
12	AGND	GND	analog ground
13	VA	PWR	analog supply, 5V, input, connect .1µ bypass cap to GND
14	MID	OUTPUT	MID reference output, connect .1µ cap to GND
15	OUTR+	OUTPUT	positive analog output, right channel
16	OUTR-	OUTPUT	negative analog output, right channel



Dimensions (Typical)	Inches	Millimeters
A	.389”	9.88
B	.154”	3.91
C	.236”	5.99
D	.100”	2.50
E	.008”	0.20
F	.025”	0.64
G	.050”	1.27
H	.017”	0.42
J	.011”	0.27
K	.170”	4.32
L	.033”	0.83

Notes:
Dimension “A” does not include mold flash, protrusions or gate burrs.

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Analog Characteristics

(Ta=25°C, VA=VD=V_{REF}=5V, Fs=48kHz, input=1kHz 24 bit data, measurement bandwidth=20Hz-20kHz, unless otherwise specified)

Parameter	Comments	Min	Typ	Max	Units
Dynamic Range	output=-60dBFS (A-wt)		107		dB
THD+N	output= 0dBFS output=-20dBFS output=-60dBFS		-90 -84 -44		dB dB dB
Crosstalk	output= 0dBFS		-118		dB
Output voltage	[OUT+]-[OUT-][1] Fullscale interchannel match differential dc offset common mode dc bias		+/-4.0 .05 1 2.5		V dB mV V
Max. output current			+/-0.4		mA
Output impedance	differential		3		Ohm
Power supply current	analog (I_A) digital (I_D)		28 6		mA mA
REF current	I_{REF}[2]		190		µA
Power consumption			170		mW
Gain Error	REF+ held at 5V			+/-.69	%
PSRR	REF+ held at 5V		70		dB

Note 1: Output voltage scales linearly with reference potential ([REF+]-[REF-])
Note 2: REF current scales with Fs.

Combined Digital and Analog Filter Characteristics

(Ta=25°C, VA=VD=V_{REF}=5V, Fs48kHz)

Parameter	Comments	Min	Typ	Max	Units
Passband	+/-0.1dB BW[1]	0		21.77K	Hz
	Ripple			+/-.007	dB
Stopband	Frequency[1] Attenuation	26.23k -70			Hz dB
Group delay			28.5		1/Fs
Deemphasis Filter	Fs=44.1kHz 'pole' time constant 'zero' time constant		 50 15		 µs µs

Note 1: passband, stopband, and deemphasis frequencies scale with Fs.

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Recommended Operating Conditions

(GNDA=GNDD=0V)

Parameter	Comments	Min	Typ	Max	Units
VA	analog supply voltage	4.5	5.0	5.5	V
VD	digital supply voltage	4.5	5.0	5.5	V
T_a	ambient temperature	0	25	70	°C
Fs	sample frequency	24	48	55	kHz
rl	differential load resistance	12K			Ohm

Electrical Characteristics – Digital Pins

(T_a=25°C)

Parameter	Comments	Min	Typ	Max	Units
INPUTS (WDCLK, DIN, DEM, FORMAT)					
V_{ih}	Logical “1” input voltage	0.55VD			V
V_{oh}	Logical “0” input voltage			.1VD	V
I_{in}	input leakage current			1	µA
C_{in}	input capacitance		5		pF

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System Description

Serial Interface and Timing

The AL1201 receives its 2's complement serial data in a standard MSB-first format. Two bit-rates are allowed for. The 32 bits/frame (FORMAT low) is suitable for use in systems where a 256Fs master clock is present. The 24 bits/frame (FORMAT high) is convenient when interfacing with systems where a 384Fs clock is present.

The input sample period is defined between rising edges of wordclock (WDCLK) input. Nominally, this is a 50% duty-cycle clock at frequency Fs, but it can be a pulse with Ts/256 < pulse-width < Ts (255/256); Ts=1/Fs. Left channel data is presented to the AL1201 with rising edge of WDCLK, and right channel data is presented Ts/2 seconds later (when WDCLK falls if 50% duty cycle).

The serial bits are clocked into the AL1201 input registers on the falling edge of an internally generated bit clock (rising edge aligned with rising edge of WDCLK) that runs at 64Fs when FORMAT is low (32 bits/frame), or 48Fs when FORMAT is high (24 bits/frame). The input data should be valid +/-100ns from the falling edge of this internally generated clock. See timing diagram next page.

Input Logic Levels

The AL1201 can properly receive input logical '1' voltages of .55VD. This means the AL1201 can interface directly with logic signals supplied from 3.3V systems. No special interface circuitry is required.

Internal Phase-Locked Loop (PLL)

The AL1201 contains an internal PLL that locks to the rising edge of WDCLK and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock (jitter rejection corner approx. 4kHz).

The PLL allows a simplified user interface and eliminates the need of running high frequency clocks on PCB traces to the part. This reduces unwanted RF noise and coupling problems that can occur when these clocks are required as input pins for a device.

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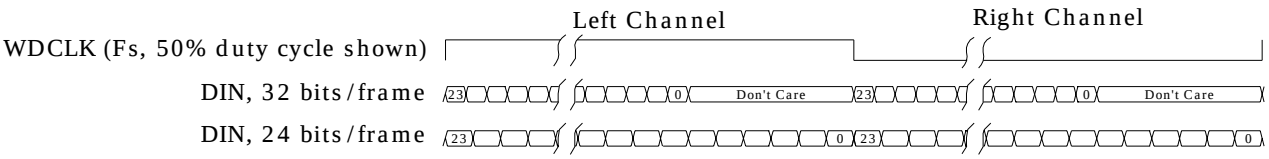
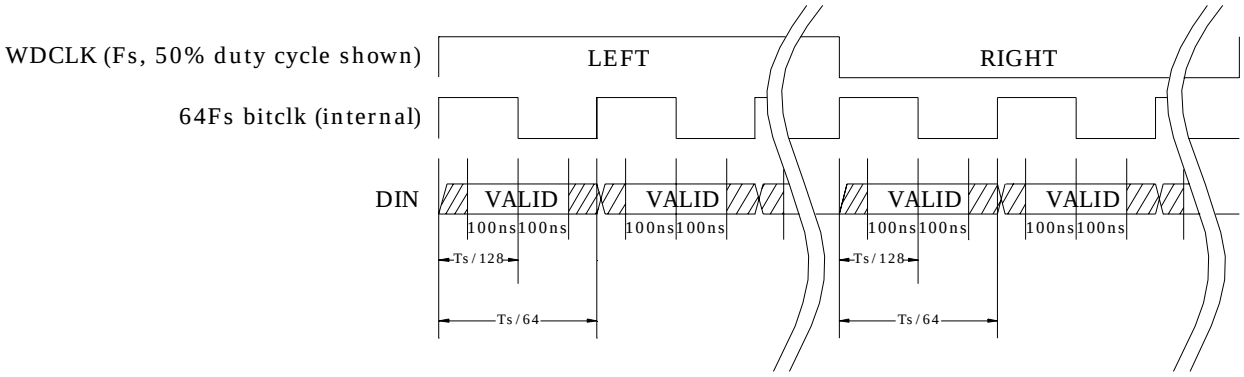
Serial Input Formats

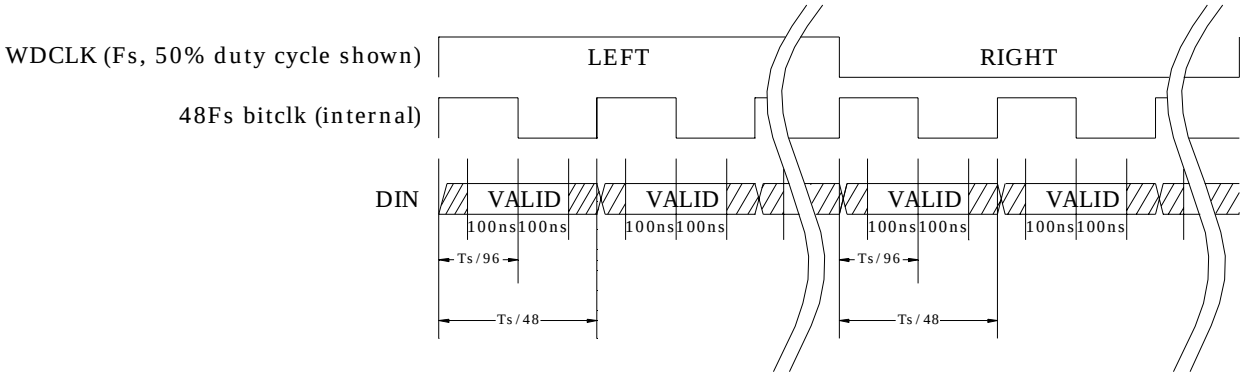


Timing Example

32 bits/frame



24 bits/frame



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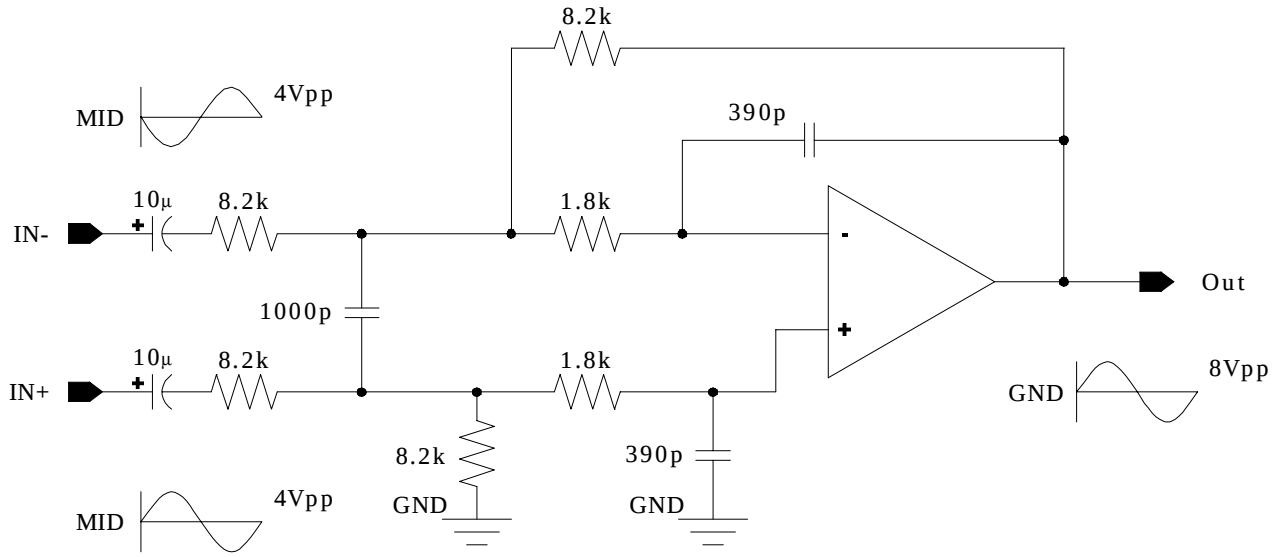
Differential Analog Outputs

The AL1201 outputs are self-biased to MID potential. Maximum differential output signal level is +/-4V. The outputs have been internally filtered to reduce out-of-band noise, and further filtering is suggested where this is considered critical. The differential-to-single-ended filter shown is a two-pole 48kHz lowpass filter whose frequency response is flat from dc to 20kHz +/-.03dB. Its group delay deviation from flat is 1.3µs at 20kHz. High quality ceramic or film capacitors suggested.



Differential to Single-ended Converter and 2-pole 48kHz lowpass filter

Reference and Mid

The differential potential between the REF+ and REF- pins (connected to VA and GND respectively) determines the amount of charge that is added to or removed from the switched-capacitor filter input for each Δ-Σ modulator output (128Fs). It is very important that REF+ is well bypassed to REF- (.1µF ceramic as close as possible to pins) to remove the unwanted effects of high frequency noise.

The MID potential is developed on chip (VA/2 volts) and is used to bias the internal amplifiers in the switched-capacitor and continuous-time filters. It requires a .1µF bypass to GND at the pin. No load current should be taken from the MID pin.

Power Supplies and Ground

A single low-impedance 5V supply is all that is required to achieve specified performance. A 5V supply plane is recommended if possible. VA and VD can be directly connected to 5V, and REF+ should be isolated with a 220-ohm resistor to 5V.

A single low impedance ground plane can be used for all GND connections, simplifying PCB layout. Each supply pin should be bypassed to GND with a .1µF ceramic cap positioned as close to the pin as possible.

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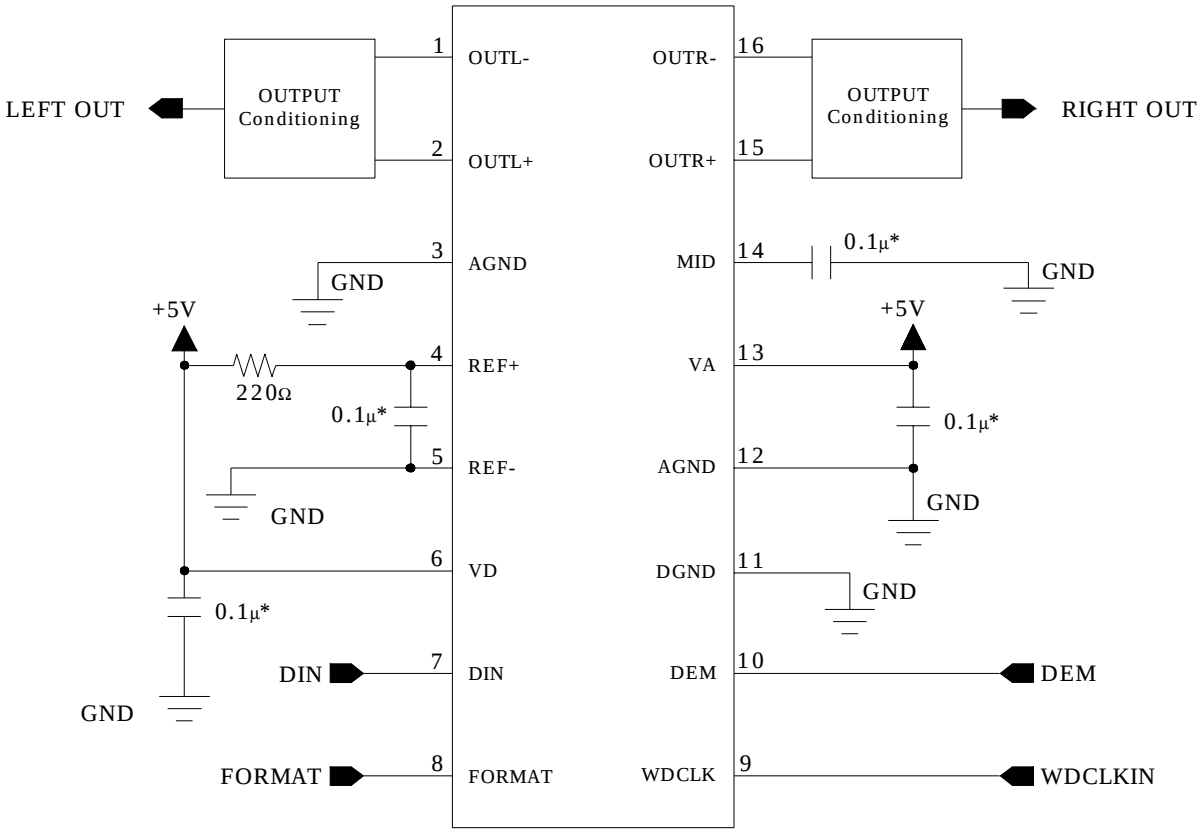

24-bit DAC

Suggested Connections

* Position caps as close to pins as possible

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Contact Information:

Alesis Semiconductor
12555 Jefferson Blvd., Suite 285
Los Angeles, CA 90066
Phone: (310) 301-0780
Fax: (310) 306-1551

Email: sales@alesis-semi.com