SN74ALB16244
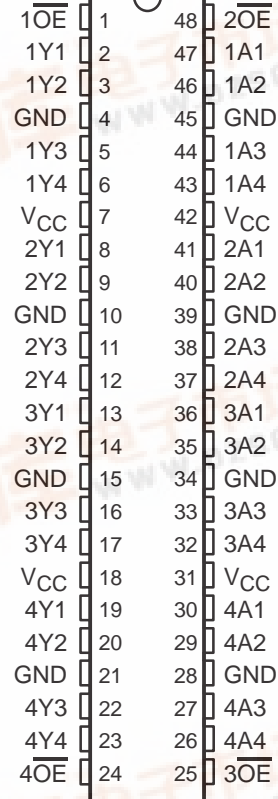## 16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS647C – AUGUST 1995 – REVISED JULY 1997

- **Member of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation**
- **Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot**
- **Industry Standard '16244 Pinout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74ALB16244 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	2$\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{OE}$	24	25	3$\overline{OE}$

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

TEXAS INSTRUMENTS

SN74ALB16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

logic symbol†

1OE	1	EN1
2OE	48	EN2
3OE	25	EN3
4OE	24	EN4

Input	Pin			Pin	Output
1A1	47	1	1 ▽	2	1Y1
1A2	46			3	1Y2
1A3	44			5	1Y3
1A4	43			6	1Y4
2A1	41	1	2 ▽	8	2Y1
2A2	40			9	2Y2
2A3	38			11	2Y3
2A4	37			12	2Y4
3A1	36	1	3 ▽	13	3Y1
3A2	35			14	3Y2
3A3	33			16	3Y3
3A4	32			17	3Y4
4A1	30	1	4 ▽	19	4Y1
4A2	29			20	4Y2
4A3	27			22	4Y3
4A4	26			23	4Y4

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
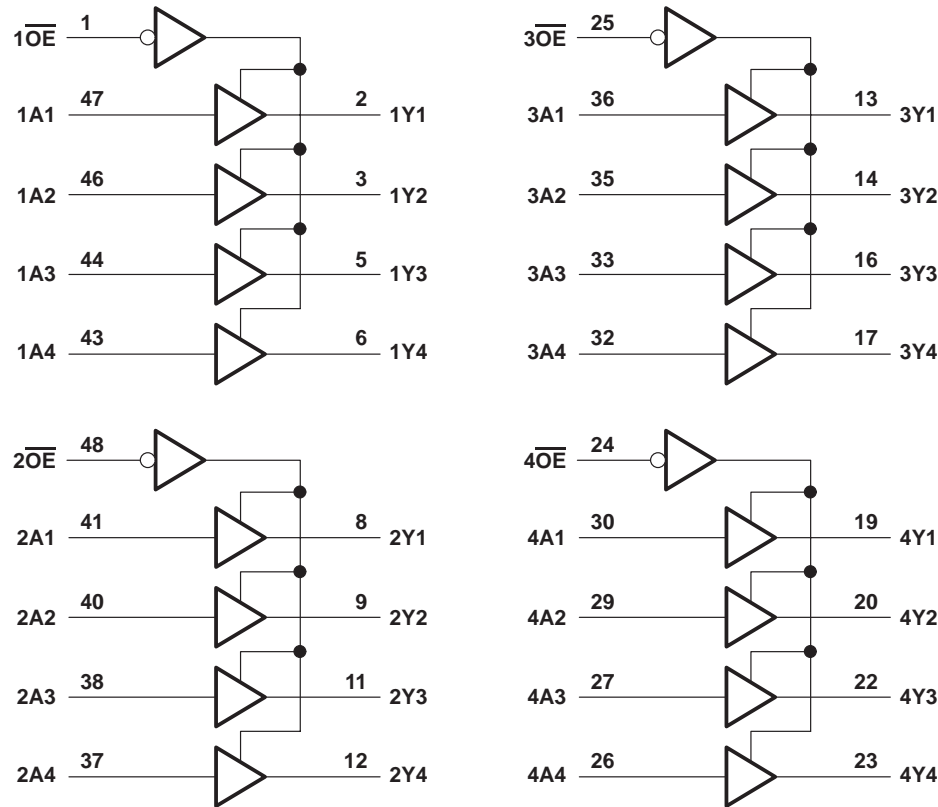
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) .... –0.5 V to 4.6 V
                    I/O ports (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through each V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package .... 89°C/W
                                         DL package .... 94°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
         2. This value is limited to 4.6 V maximum.
         3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
I_{OH}[†]	High-level output current			−25	mA
I_{OL}[†]	Low-level output current			25	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	Outputs enabled		5	ns/V
T_A	Operating free-air temperature		−40	85	°C

[†] Refer to Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}	Data inputs	V_{CC} = 3 V	I_I = 18 mA			3.6	V_{CC}−1.2	V
			I_I = −18 mA			−0.9	−1.2	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±10	µA
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}	$\overline{OE}$ low		0.4	0.6	mA
				$\overline{OE}$ high			25	µA
			V_I = 0	$\overline{OE}$ low		−0.8	−1	mA
				$\overline{OE}$ high			−60	µA
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			0.6	20	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			−0.1	−50	µA
I_{CC}/buffer		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND		3.7	5.6	mA
I_{CCZ}		V_{CC} = 3.6 V,	Control inputs = V_{CC} or GND				0.8	mA
ΔI_{CC}[§]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					600	µA
C_i		V_I = 3 V or 0					4.5	pF
C_o		V_O = 3 V or 0					5.5	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP[‡]	MAX	
t_{pd}	A	Y	0.6	1.3	2	ns
t_{en}	$\overline{OE}$	Y	1.3	2.5	4.7	ns
t_{dis}	$\overline{OE}$	Y	1.8	2.8	4.2	ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

OUTPUT VOLTAGE HIGH
vs
INPUT VOLTAGE
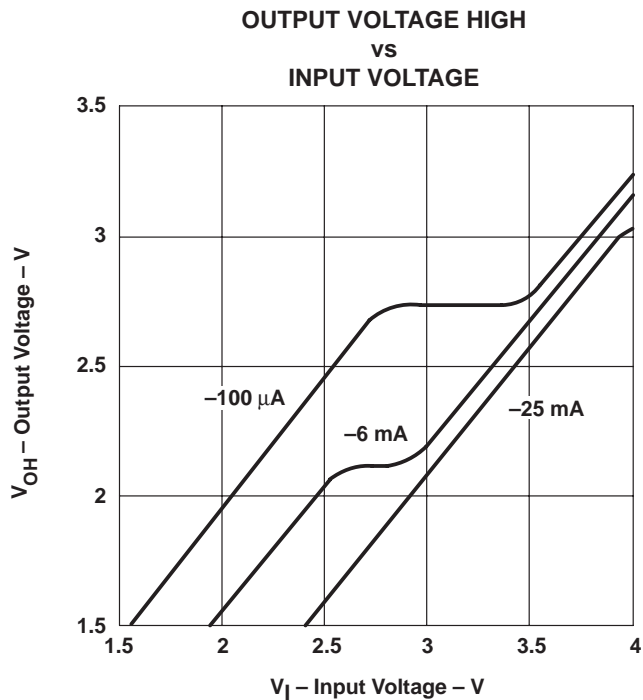
Figure 1. V_{OH} Over Recommended Free-Air Temperature Range

OUTPUT VOLTAGE LOW
vs
INPUT VOLTAGE
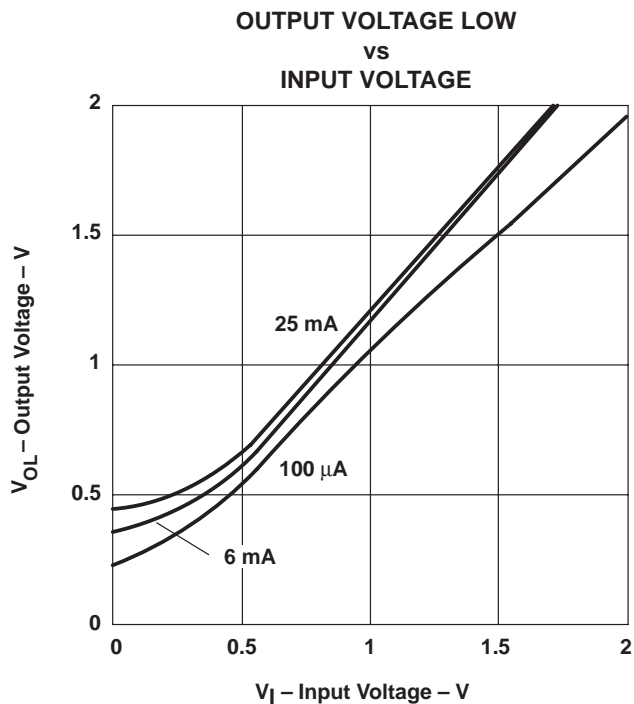
Figure 2. V_{OL} Over Recommended Free-Air Temperature Range

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
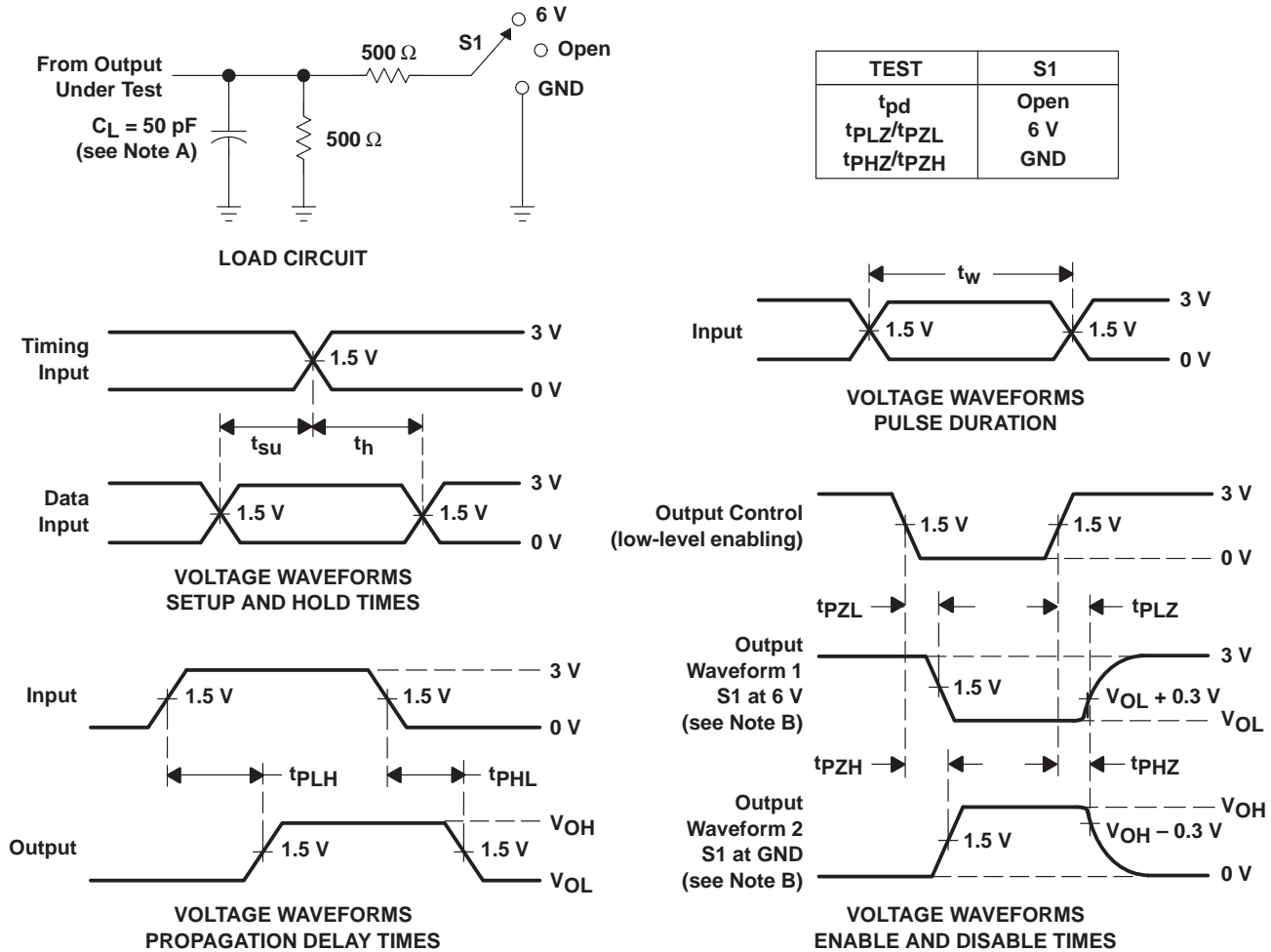
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50\,\Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

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