AnaChip

AM24LC21
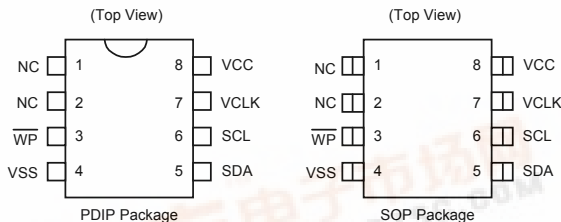(Preliminary)

Dual Mode, 1K-bits (128 x 8) 2-Wire Serial EEPROM

■ Features

- Single supply with operation down to 2.5V
- Completely implements DDC1/DDC2 interface for monitor identification, including recovery to DDC1
- Low power CMOS technology
- 1 mA typical active current
- 10 uA standby current typical at 5.5V
- 2-wire serial interface bus, I^2C compatible
- 100Khz (2.5V) and 400Khz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Hardware write-protect pin
- Page-write buffer for up to eight bytes
- 1,000,000 erase/write cycles
- Data retention > 40 years
- 8-pin PDIP and SOP packages
- Available for extended temperature ranges
  Commercial (C): 0°C to +70°C
  Industrial (I): -40°C to +85°C

■ General Description

The AM24LC21 is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: transmit only mode and bi-directional mode. Upon power-up, the device will be in the transmit only mode, sending a serial bit stream of the memory array contents, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the bi-directional mode, with byte selectable read/write capability of the memory array. The AM24LC21 is available in a standard 8-pin PDIP and SOP package in both commercial and industrial temperature ranges.
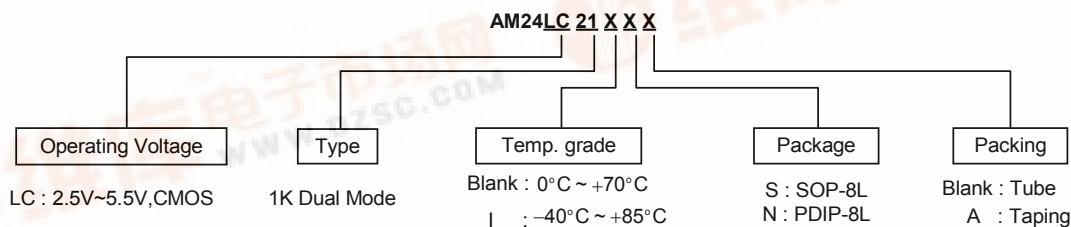
■ Pin Assignments

(Top View)

PDIP Package

NC	1		8	VCC
NC	2		7	VCLK
WP	3		6	SCL
VSS	4		5	SDA

(Top View)

SOP Package

NC	1		8	VCC
NC	2		7	VCLK
WP	3		6	SCL
VSS	4		5	SDA

■ Pin Descriptions

Name	Description
NC	No connection
VSS	Ground
SDA	Serial address/data I/O
VCLK	Serial clock (transmit only mode)
VCC	Power supply
SCL	Serial clock (bi-directional mode)
WP	Write protect (active low)

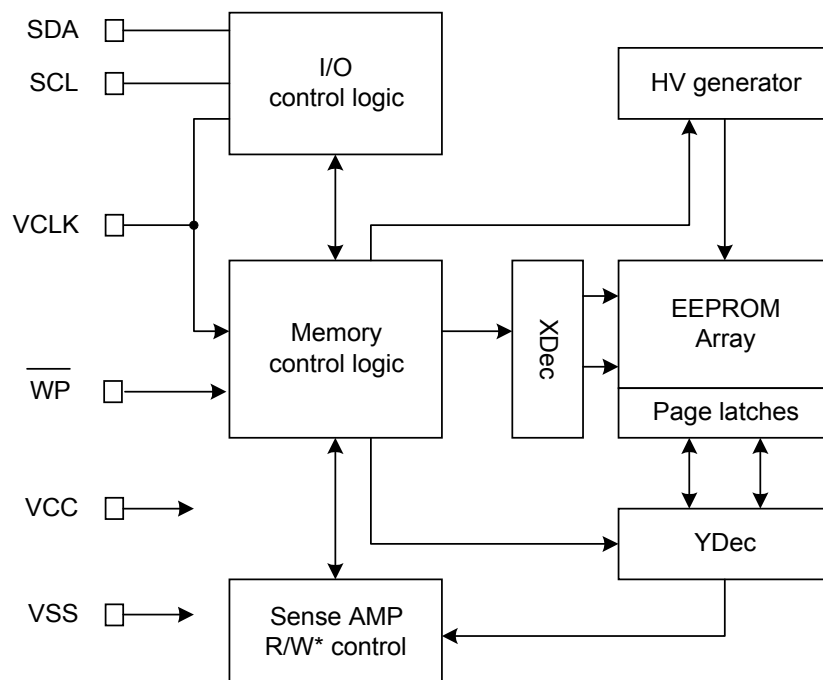**Note.** See pin description (continued) for more detailed

■ Ordering Information

AM24LC 21 X X X

Operating Voltage	Type	Temp. grade	Package	Packing
LC : 2.5V~5.5V,CMOS	1K Dual Mode	Blank : 0°C ~ +70°C I : −40°C ~ +85°C	S : SOP-8L N : PDIP-8L	Blank : Tube A : Taping

Rev. 0.0   Aug 10, 2002

Dual Mode, 1K-bits (128 x 8) 2-Wire Serial EEPROM

■ Block Diagram

■ Absolute Maximum Ratings [(Note)]

Symbol	Parameter	Rating	Unit
V_{CC}	Voltage with respect to ground	7	V
V_{SS}	All inputs and outputs w.r.t.	-0.6V to Vcc+1	V
T_{OP}	Operating temperature	0 to + 70 (commercial) -40 to +85 (industrial)	°C
T_{STG}	Storage temperature	-65 to +125	°C

■ DC Electrical Characteristics (Vcc=2.5V to 5.5V, T_{AC}=0°C ~ +70°C, T_{AI}= -40°C ~ +85°C)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IH}	SCL and SDA pins: High level input voltage	–	0.7Vcc	–	V
V_{IL}	SCL and SDA pins: Low level input voltage	–	–	0.3Vcc	V
V_{IH}	VCLK pin input level: High level input voltage	$V_{CC} \geq 2.7V$ (Note)	2	–	V
V_{IL}	VCLK pin input levels: Low level input voltage	$V_{CC} <2.7V$ (Note)	–	0.2Vcc	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	(Note)	0.05Vcc	–	V
V_{OL1}	Low level output voltage	I_{OL}=3mA, V_{CC}=2.5V (Note)	–	0.4	V
V_{OL2}	Low level output voltage	I_{OL}=6mA, V_{CC}=2.5V	–	0.6	V
I_{LI}	Input leakage current	V_{IN} = 0.1V to V_{CC}	-10	10	uA
I_{LO}	Output leakage current	V_{OUT} = 0.1V to V_{CC}	-10	10	uA
$I_{CC(Write)}$	Operating current	V_{CC} = 5.5V, SCL=400Khz	–	3	mA
$I_{CC(Read)}$	Operating current	V_{CC} = 5.5V, SCL=400Khz	–	1	mA
I_{CCS}	standby current	V_{CC} = 3V, SDA=SCL= V_{CC} V_{CC} = 5.5V, SDA=SCL= $V_{CC,}$ VCLK=V_{SS}	– –	30 100	uA

Note : This parameter is periodically sampled and not 100% tested

■ AC Electrical Characteristics

Symbol	Parameter	Standard Mode		Vcc=4.5V~5.5V Fast mode		Unit	Remarks
		Min	Max	Min	Max		
F_{CLK}	Clock frequency	–	100	–	400	Khz	–
T_H	Clock high time	4	–	0.6	–	us	–
T_L	Clock low time	4.7	–	1.3	–	us	–
T_R	SDA and SCL rise time	–	1	–	0.3	us	(Note1)
T_F	SDA and SCL fall time	–	0.3	–	0.3	us	(Note1)
$T_{HD(ST)}$	Start condition hold time	4	–	0.6	–	us	After this period the first clock pulse is generated
$T_{SU(ST)}$	Start condition setup time	4.7	–	0.6	–	us	Only relevant for repeated start condition
$T_{HD(DI)}$	Data input hold time	0	–	0	–	us	(Note 2)
$T_{SU(DI)}$	Data input setup time	0.25	–	0.1	–	us	–
$T_{SU(STP)}$	Stop condition setup time	4	–	0.6	–	us	–
T_{AA}	Output valid from clock	–	3.5	–	0.9	us	(Note 2)
T_{BUF}	Bus free time	4.7	–	1.3	–	us	Time the bus must be free before a new transmission can start
T_{OF}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$	–	0.25	$20+0.1C_B$	0.25	us	(Note 1), $C_B \leq 100pF$
T_{SP}	Input filter spike suppression (SDA and SCL pins)	–	0.05	–	0.05	us	(Note 3)
T_{WR}	Write cycle time	–	10	–	10	ms	Byte or page mode
T_{VAA}	Output valid from V_{CLK}	–	2	–	1		–
T_{VH}	VCLK high time	4	–	0.6	–		–
T_{VL}	VCLK low time	4.7	–	1.3	–		–
T_{VHZ}	Mode transition time	–	0.5	–	0.5		–
T_{VPU}	Transmit only power up time	0	–	0	–		–
–	Endurance	1M	–	1M	–	cycles	25^0C, V_{CC}=5V, Block mode (Note 4)

Note 1. Not 100% tested. C_B=total capacitance of one bus line in pF.
Note 2. As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300ns) of the falling edge of SCL to avoid unitended generation of start or stop conditions
Note 3. The combined T_{SP} and V_{hys} specifications are due to new schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a T_I specification for standard operation.
Note 4. This parameter is not tested but ensured by characterization.

■ Functional description

1.0 Overview
The AM24LC21 operates in two modes, the transmit-only mode and the bi-directional mode. There is a separate two wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bi-directional mode. The only way to switch the device back to the transmit-only mode is to remove power from the device.

2.1 Transmit-only mode
The device will power up in the transmit-only mode. This mode supports a unidirectional two wire protocol for trans-mission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the transmit-only mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8 bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the transmit-only mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The bi-directional mode clock (SCL) pin must be held high for the device to remain in the transmit-only mode.

2.2 Initialization procedure
After VCC has stabilized, the device will be in the transmit-only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address. (Figure 2-2).
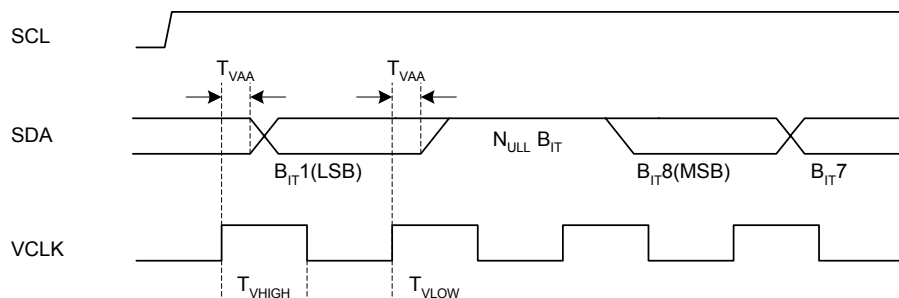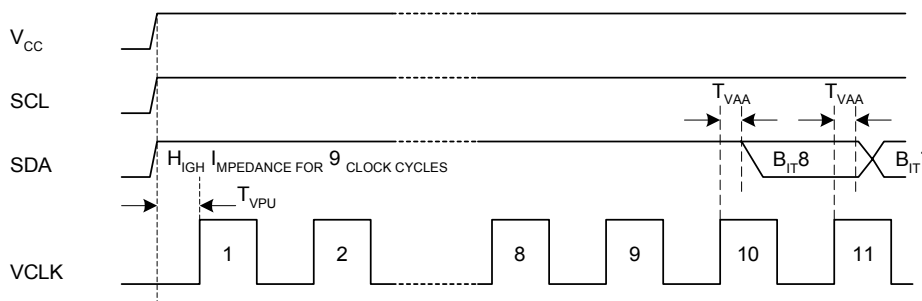

Figure 2-1. Transmit only mode

Figure 2-2. Device initialization

3.0 Bi-directional mode

The AM24LC21 can be switched into the bi-directional mode (see Figure 3-1) by applying a valid high to low transition on the bi-directional mode clock (SCL). When the device has been switched into the bi-directional mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two wire bi-directional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be con-trolled by a master device that generates the bi-directional mode clock (SCL), controls access to the bus and generates the START and STOP conditions, while the AM24LC21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Any high to low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h.(see Figure 3-1, 3-2)

3.1 Bi-directional mode bus characteristics

The following bus protocol has been defined:
- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition. Accordingly, the following bus conditions have been defined (see Figure 3-3).

3.1.1 Bus not busy (A)

Both data and clock lines remain HIGH.

3.1.2 Start data transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP data transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
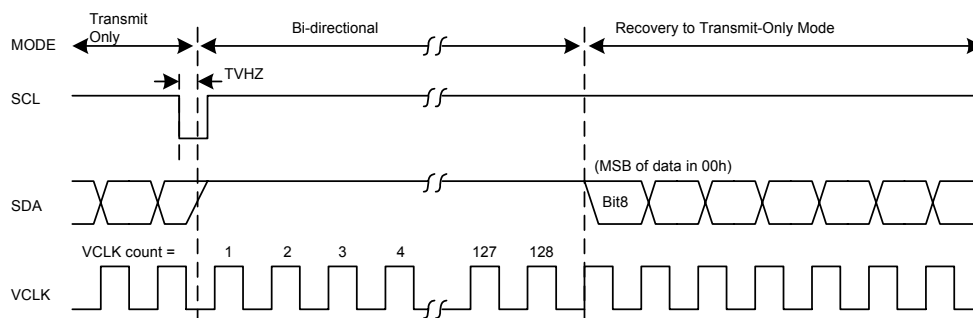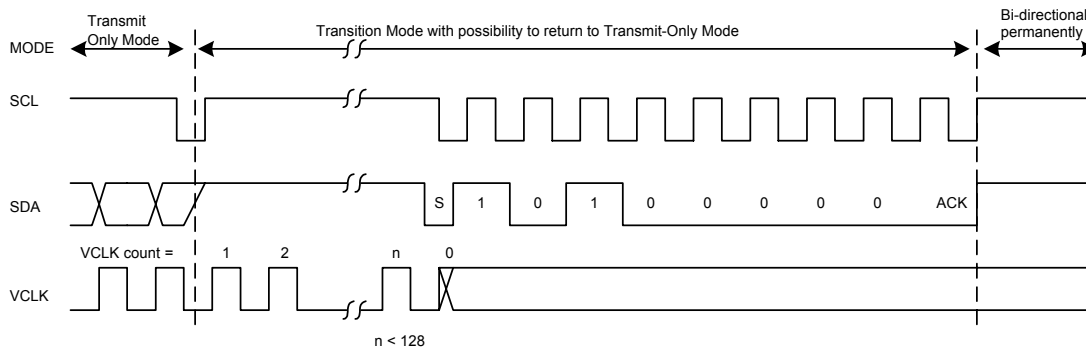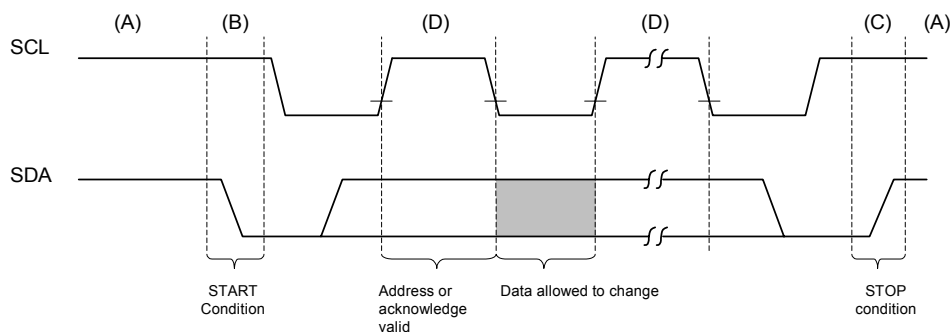

Figure 3-1. Mode transition

Figure 3-2. Successful Mode transition

Rev. 0.0   Aug 10, 2002

Dual Mode, 1K-bits (128 x 8) 2-Wire Serial EEPROM

Figure 3-3. Data transfer sequence on the serial bus

3.1.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

3.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:
The AM24LC21 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
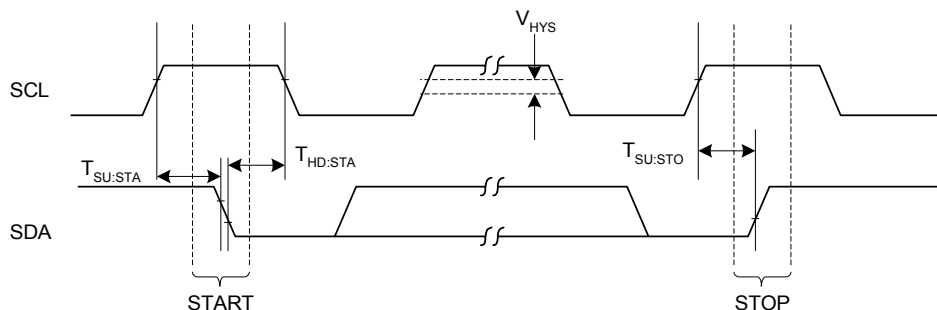

Figure 3-4. Bus timing start/stop
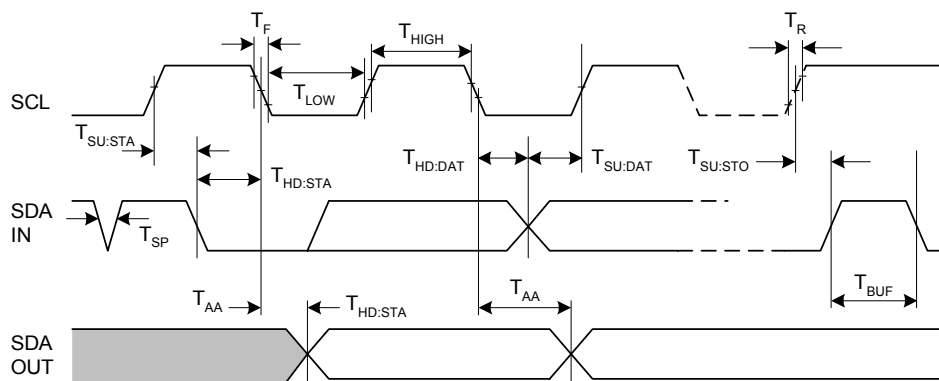
Figure 3-5. Bus timing data

3.1.6 Slave address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010) for the AM24LC21, followed by three 000 3 bits. The eighth bit of slave address determines if the master device wants to read or write to the AM24LC21 (Figure 3-6). The AM24LC21 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control code	Chip select	R / $\overline{\text{W}}$
Read	1010	000	1
Write	1010	000	0
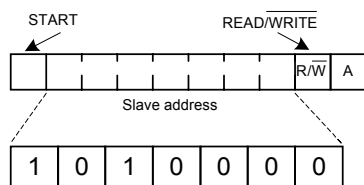
Figure 3-6. Control byte allocation

4.1 Byte Write

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the AM24LC21 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the AM24LC21 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant.

Following the start signal from the master, the slave address (4 bits), 000 (3 bits) and the R/W bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will fol-low after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmit-ted by the master is the word address and will be written into the address pointer of the AM24LC21. After receiving another acknowledge signal from the AM24LC21 the master device will transmit the data word to be writ-ten into the addressed memory location. The AM24LC21 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the AM24LC21 will not generate acknowledge signals (Figure 4-1). It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

If the

master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2). It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

Note:
Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.
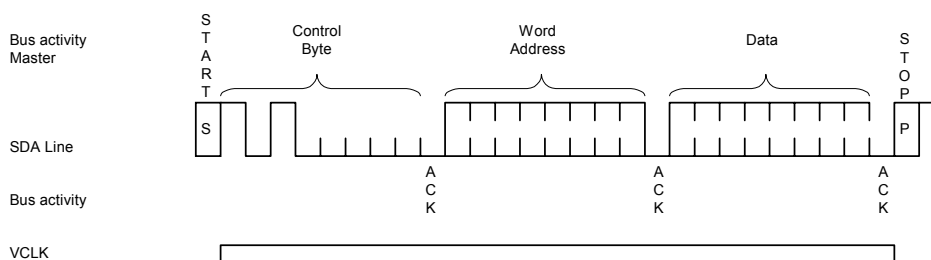
Figure 4-1. Byte write
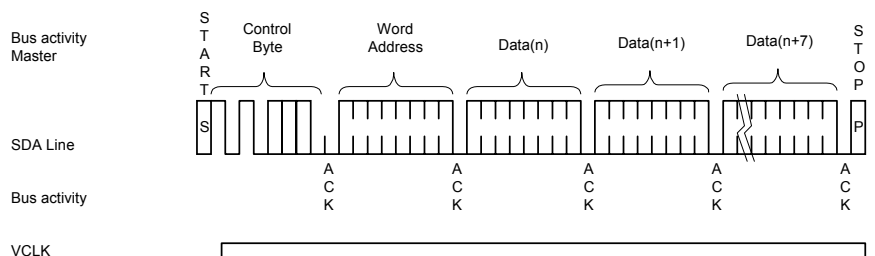

Figure 4-2. Page write

5.0 Acknowledge polling
Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

6.0 Write protection
When using the AM24LC21 in the bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the AM24LC21 to operate as a serial ROM, although this configuration would prevent using the device in the transmit-only mode.
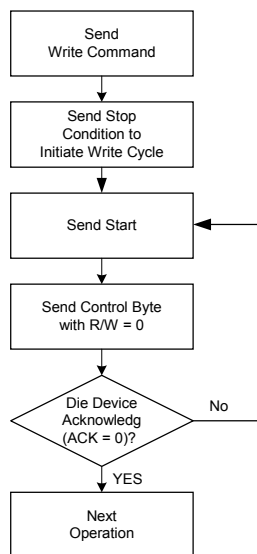
Figure 5-1: Acknowledge polling flow

7.0 Read operation

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current address read

The AM24LC21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to '1', the AM24LC21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the AM24LC21 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the AM24LC21 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a '1'. The AM24LC21 will then issue an acknowledge and transmits the eight bit data word.The master will not acknowledge the transfer but does generate a stop condition and the AM24LC21 discontinues transmission (Figure 7-2).
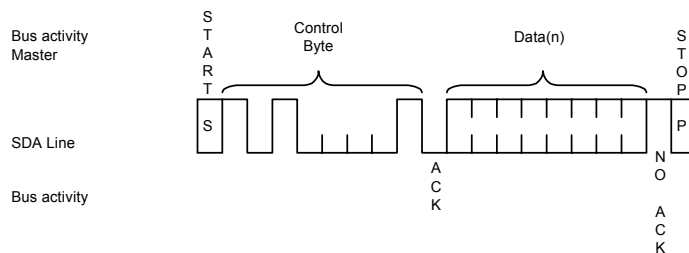
7.3 Sequential Read

Sequential reads are initiated in the same way as a ran-dom read except that after the AM24LC21 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the AM24LC21 to transmit the next sequentially addressed 8-bit word (see Figure 7-3).
To provide sequential reads the AM24LC21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise protection

The AM24LC21 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.
The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

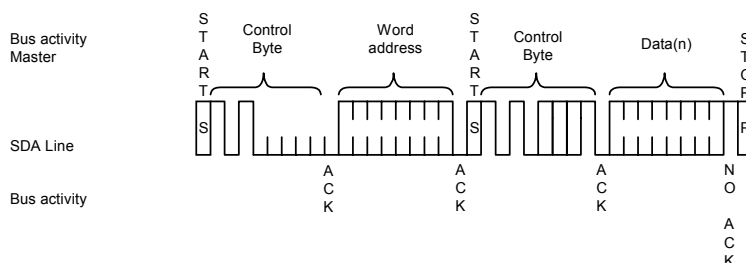
Figure 7-1. Current address read

Dual Mode, 1K-bits (128 x 8) 2-Wire Serial EEPROM

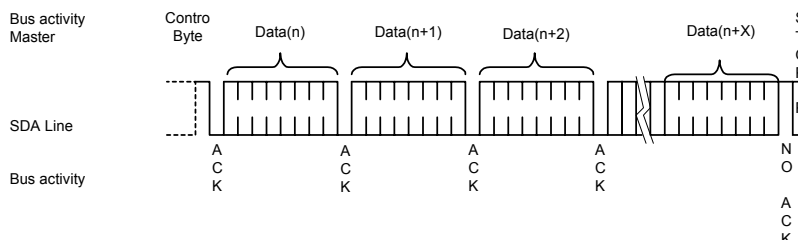

Figure 7-2. Random read

Figure 7-3. Sequential read

■ Pin Descriptions (Continued)

SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the bi-directional mode. In the transmit-only mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10k for 100 Khz, 1k for 400 Khz).

For normal data transfer in the bi-directional mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL

This pin is the clock input for the bi-directional mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the transmit only mode to the bi-directional mode. It must remain high for the chip to continue operation in the transmit only mode.

VCLK

This pin is the clock input for the transmit only mode. In the transmit only mode, each bit is clocked out on the rising edge of this signal. In the bi-directional mode, a high logic level is required on this pin to enable write capability.

$\overline{WP}$

When using the AM24LC21 in the bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the AM24LC21 to operate as a serial ROM, although this configuration would prevent using the device in the transmit-only mode. If WP is connected to GND, PROGRAM operation onto the whole memory will not be executed. READ operation are possible. If WP is connected to Vcc, normal memory operation is enabled, READ/$\overline{WRITE}$ over the entire memory is possible.
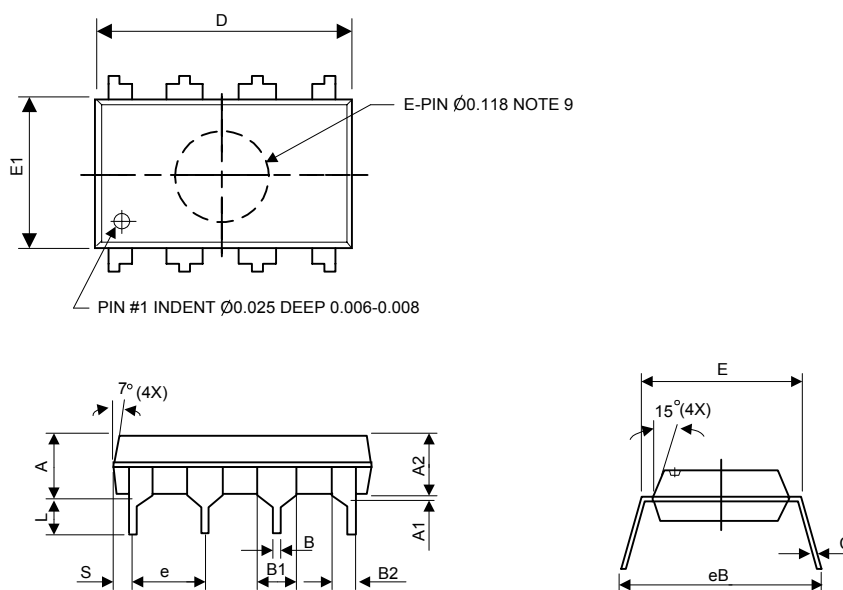
■ Package Information

(1) Package Type: PDIP-8L

E-PIN Ø0.118 NOTE 9

PIN #1 INDENT Ø0.025 DEEP 0.006-0.008

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	5.33	—	—	0.210
A1	0.38	—	—	0.015	—	—
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.27	1.52	0.045	0.050	0.060
B2	0.18	0.99	1.17	0.032	0.039	0.046
C	0.20	0.25	0.33	0.008	0.010	0.013
D	9.12	9.30	9.53	0.359	0.366	0.375
E	7.62	—	8.26	0.300	—	0.325
E1	6.20	6.35	6.60	0.244	0.250	0.260
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.40	0.330	—	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

Dual Mode, 1K-bits (128 x 8) 2-Wire Serial EEPROM

(2) Package Type: SOP-8L

VIEW "A"

VIEW "A"
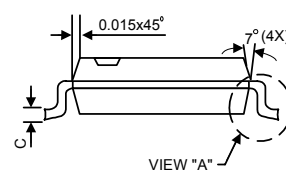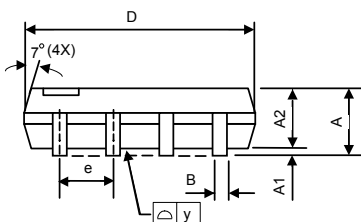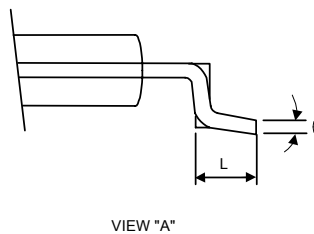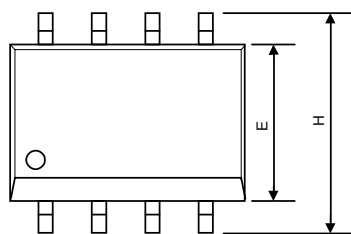
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

■ **Marking Information**

Logo

Part Number & grade
X=Blank   (0^0C to $+70^0$C)
X=I   (-40^0C to $+85^0$C)

AC
24LC21X
YYWWX

Date Code
YY: Year
WW: Nth week
X: Internal code

PDIP/SOP/ Package